SGM41286
LNB Supply W/Tone Repeater/Synthesizer W/Programmable Cable Drop Correction

GENERAL DESCRIPTION

This device is a high efficiency boost power supply which converts 12V nominal input to 14V/19V nominal output, plus a linear regulation stage for tone signal transmission. It could repeat the external 22kHz tone input symmetrically or synthesize a 22kHz tone signal upon external on/off control.

Pulsing on its EN initials -1V/+0.4V drop correction, makes it suitable for using external surge absorbing devices and for long cable installation.

The SGM41286 is available in Green TDFN-3×3-8L and SOIC-8 (Exposed Pad) packages. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **7V to 14V Input Voltage**
- **14V/19V 500mA Output**
- **DiSEqC 1.X Compatible**
- **Programmable -1V/+0.4V Drop Correction**
- **High Efficiency Low Head Room Architecture**
- **Acoustic Noise Free Low Power Operation**
- **Automatic Tone Repeater or Tone Synthesizer**
- **LDO Output and Low Out-of-Band Noise**
- **Internal Short-Safe Over-Current Protection**
- **Internal Over-Temperature Protection**
- **200ms Current Limit Loading Surge Window**
- **Available in Green TDFN-3×3-8L and SOIC-8 (Exposed Pad) Packages**
- **-40℃ to +85℃ Operating Temperature Range**

APPLICATIONS

STB Satellite Receiver
TV Satellite Receiver
PC Card Satellite Receiver

TYPICAL APPLICATION

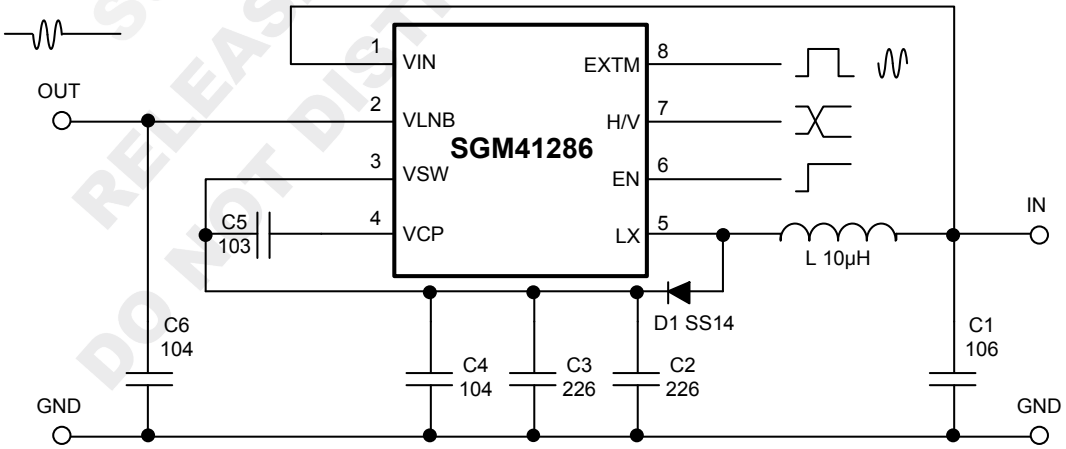


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41286	TDFN-3×3-8L	-40℃ to +85℃	SGM41286YTDB8G/TR	SGM 41286DB XXXXX	Tape and Reel, 4000
	SOIC-8 (Exposed Pad)	-40℃ to +85℃	SGM41286YPS8G/TR	SGM 41286YPS8 XXXXX	Tape and Reel, 2500

NOTE: XXXXX = Date Code and Vendor Code.

Green (RoHS& HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

V_{IN} ..... -0.3V to 22.5V
LX, VCP, VSW ..... -0.3V to 22.5V
EN, H/V, EXTM ..... -0.3V to 6V
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
VLNB to GND, HBM 8000V
All Rest Pins to GND, HBM 4000V
Pin to Pin, MM 400V
Surge Immunity, 10μs/700μs, ±Impulse 40V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage Range ..... 7V to 14V
Operating Temperature Range ..... -40℃ to +85℃
Operating Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

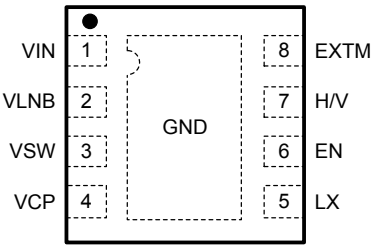
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

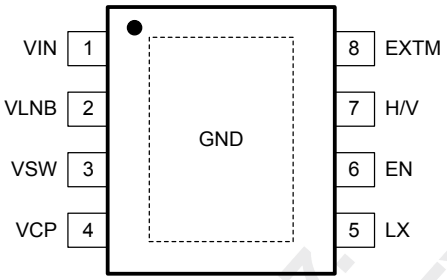
PIN CONFIGURATIONS

(TOP VIEW)



TDFN-3×3-8L

(TOP VIEW)



SOIC-8 (Exposed Pad)

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
TDFN-3×3-8L/ SOIC-8 (Exposed Pad)			
1	VIN	P	Power Input for Internal Circuit.
2	VLNB	O	Output for LNB Powering. Connect with a 100nF decoupling capacitor.
3	VSW	O	Input for Powering Output Stage.
4	VCP	O	Charge Pump Storage Output for Internal Use. Connect with a 10nF storage capacitor.
5	LX	O	Switch Node of Boost. Connect with one end of a power inductor.
6	EN	I	Enable Input. Pull to 1.2V~6V logic high to enable chip function.
7	H/V	I	VLNB Output Voltage Selection Input. Pull to 1.2V~6V logic high for 19V nominal output, pull to low or leave it open for 14V nominal output.
8	EXTM	I	External 22kHz Tone Input and Internal Tone Synthesizer Enable Input. If a 22kHz ± 20% pulse string applied, symmetric pulse string is sent to VLNB to superpose over its output after first pulse in the string; If input stays high for over 46μs, an internal 22kHz is sent for output.
Exposed Pad	GND	G	Ground of Chip Internal Circuit.

NOTE：1. P: power, I: input, O: output, G: ground.

ELECTRICAL CHARACTERISTICS

(V_{IN} = 12V, V_{EN} = 3V, C_{IN} = 10μF, C_{VSW} = 22μF × 2, L = 10μH and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OPERATION CHARACTERISTIC						
Supply Voltage	V_{OPM}		7	12	14	V
Under-Voltage Lockout Release Voltage	UVLOr	V_{IN} rising		4.5		V
Shutdown Supply Current	I_Q	EN = 0		60		μA
Operation Supply Current	I_{OP}	EN = 1, H/V = 0, I_{OUT} = 0mA		4		mA
Boost Switching Frequency	fswm	No load		22		kHz
Boost Switching Frequency	fsw_1			1.4		MHz
VLNB Output Voltage	V14	H/V = 0, I_{OUT} = 500mA		14		V
	V19	H/V = 1, I_{OUT} = 500mA		19		
Power Supply Rejection Ratio	14PSRR1k	1kHz, H/V = 0, V_{PP} = 200mV		-58		dB
	19PSRR1k	1kHz, H/V = 1, V_{PP} = 200mV		-50		
Line Regulation	$14V_{LINEREG}$	V_{IN} = 11V to12V, I_{OUT} = 500mA, H/V = 0		0.01		%/V
	$19V_{LINEREG}$	V_{IN} = 11V to12V, I_{OUT} = 500mA, H/V = 1		0.01		
Linear Regulator Dropout Voltage	V_{RRM}			600		mV
Short Circuit Current Limit	I_{SHRT}			3		A
Over-Current Limit	I_{OC}			750		mA
Output Current	I_{OUT}			500		mA
Over-Current Blanking Time	t_{OCBLK}			187		ms
Over-Current Retry Time	t_{RETRY}			748		ms
Count of Over-Current Retry Times	C_{RETRY}			8		–
Line Drop Correction Voltage	DCV	3 negative EN pulses		-1		V
		4 negative EN pulses		+0.4		V
Efficiency (No Tone)	η	H/V = low, load current = 500mA		89.5		%
		H/V = high, load current = 500mA		89		
Efficiency (Tone)	$η_T$	H/V = low, load current = 500mA		87.7		%
		H/V = high, load current = 500mA		87.5		
OVER-TEMPERATURE PROTECTION						
Over-Temperature Shutdown	T_{OT}			160		℃
Over-Temperature Protection Hysteresis	T_{OTHYS}			30		℃
LOGIC SIGNALS						
Logic High Threshold Level	V_{TL}	EN, H/V, EXTM			0.4	V
	V_{TH}		1.2			
Logic Input Current	I_{IN}				1	μA
TIMING						
Power Blanking Time	t_{PONBLK}			93.5		ms
Delay Time for Tone Starting after Enable	t_{ENDLY}			2.9		ms
Delay Time for Output Starting after Enable	t_{ONDLY}			23.5		ms
Delay Time for Line Drop Out Correction after End of EN Pulses	$t_{PROGDLY}$			2.9		ms
Delay Time for Output Stopping after Disable	t_{OFFDLY}			23.5		ms

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN} = 12V, V_{EN} = 3V, C_{IN} = 10μF, C_{VSW} = 22μF × 2, L = 10μH and T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Detection time for Internal Synthesized Tone Signal	t_{SYNDLY}			46		μs
SYNTHESIZED TONE						
Frequency of Internal Synthesized Tone Signal	f_{22k}			22		kHz
Tone Amplitude	V_{PPTONE}			600		mV
Tone Duty Cycle	D			50		%
Tone Rise Time	t_R			5		μs
Tone Fall Time	t_F			5		μs
EN NEGATIVE PULSES						
Minimum on Time between Two EN Negative Pulses	t_{SH}			30		μs
Minimum off Time of EN Negative Pulse	t_{SL}			30		μs
Delay Time for Sending EN Negative Pulses after Enable	t_{E2S}			2.9		ms
Detection Time for end of EN Pulses	t_{EOS}			2.9		ms

FUNCTIONAL BLOCK DIAGRAM

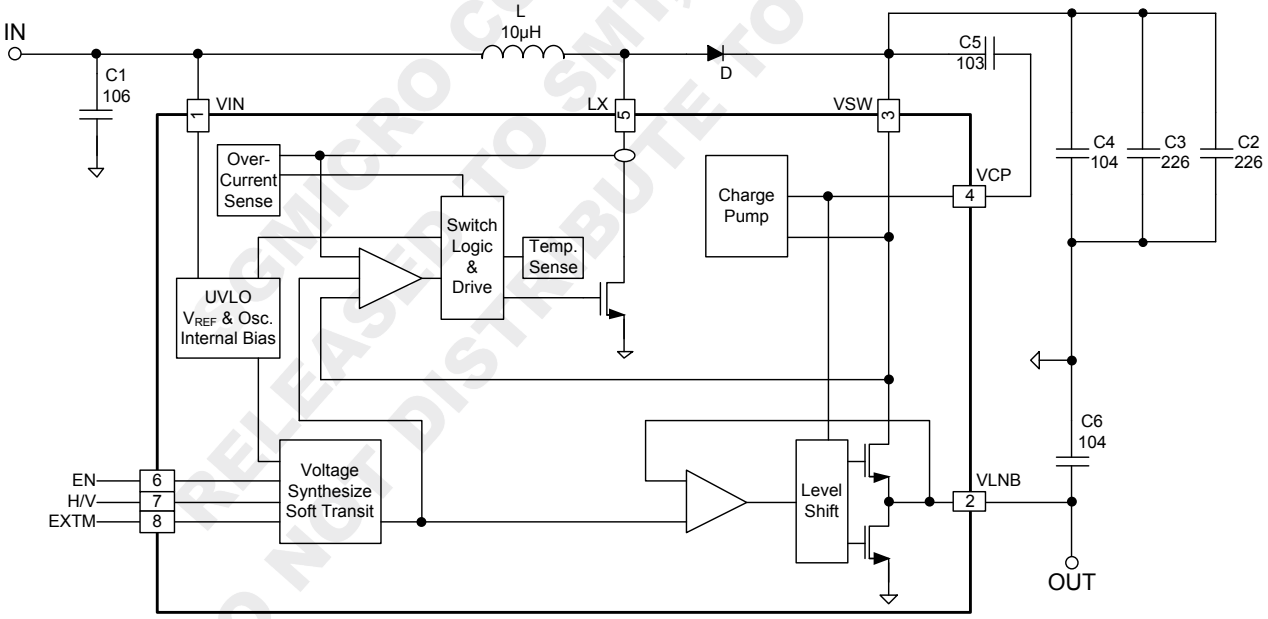


Figure 2. Block Diagram

ESSENTIAL SEQUENCE

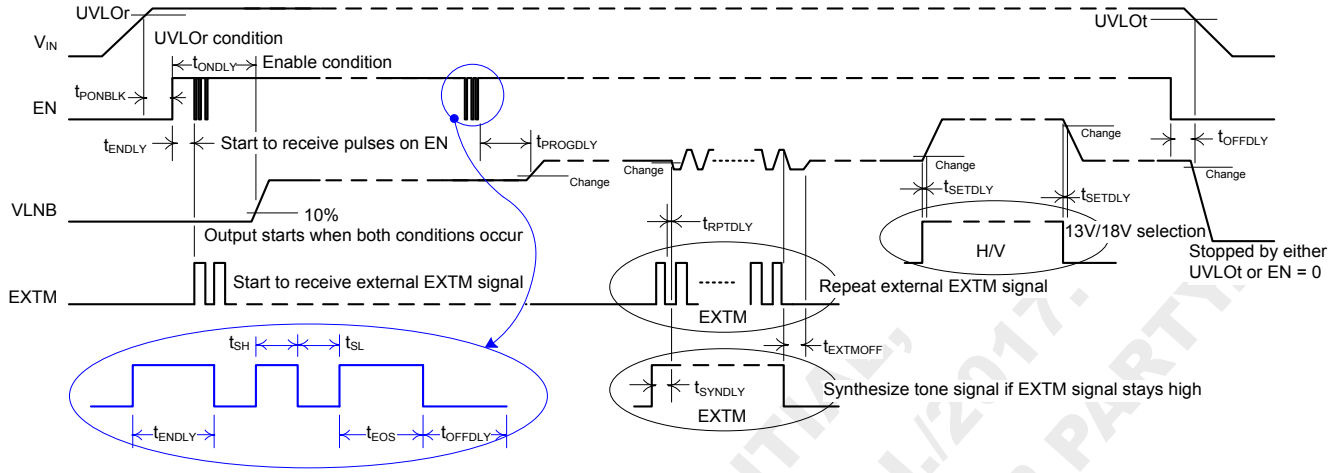
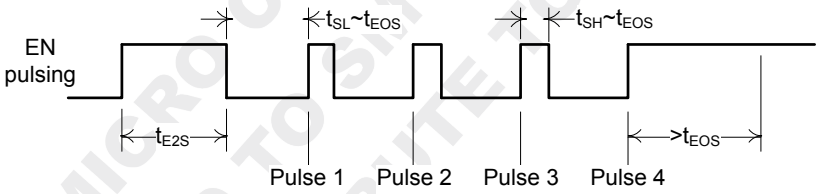


Figure 3. Essential Sequence Timings

CONTROLS and LOGIC DIAGRAMS

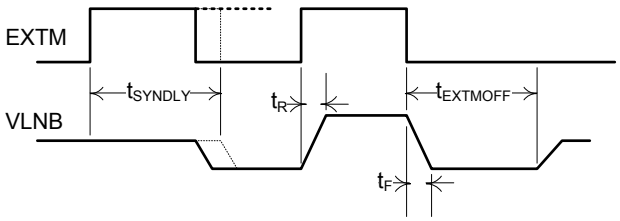
EN Pulsing and Counting



Pulse Counts to Output Status

COUNTS	DESCRIPTION
0	Ignore, keep its original output status.
1	Ignore, keep its original status.
2	Reset to no drop correction status.
3	Apply -1V drop correction superposing its normal output voltage.
4	Apply +0.4V drop correction superposing its normal output voltage.
>4	Ignore, keep its original status. Counting overflow is kept until $t_{PROGDLY}$ times out.

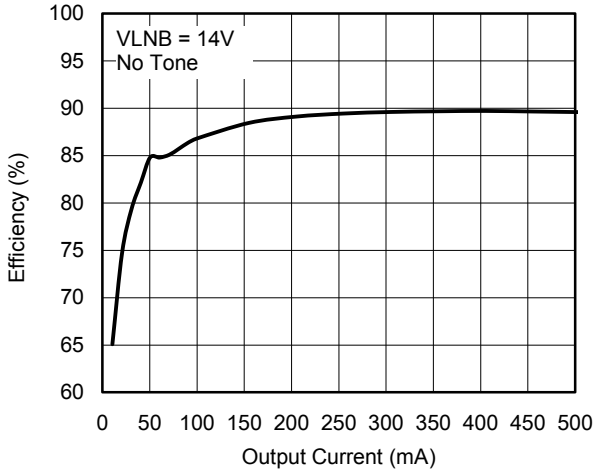
EXTM Signal Timing



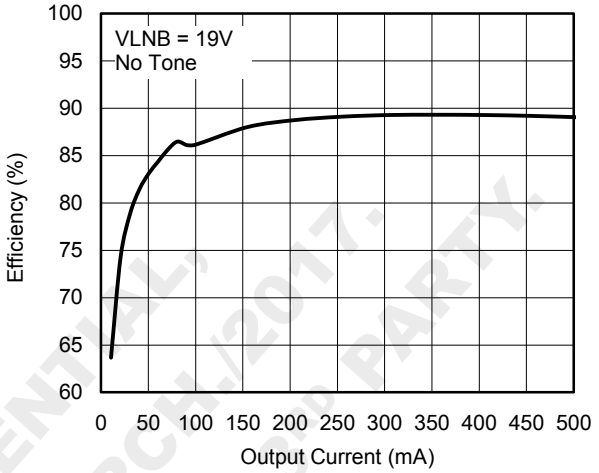
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, C_{IN} = 10μF, C_{VSW} = 22μF × 2, L = 10μH and T_A = +25℃, unless otherwise noted.

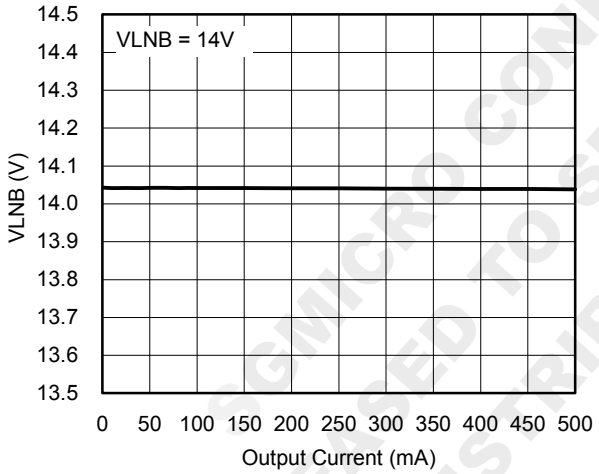
Efficiency vs. Output Current



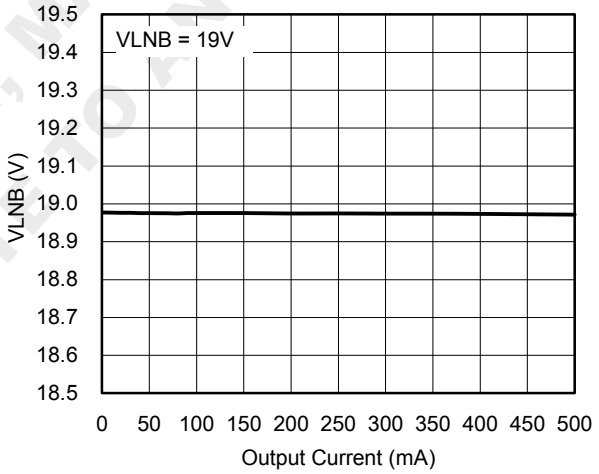
Efficiency vs. Output Current



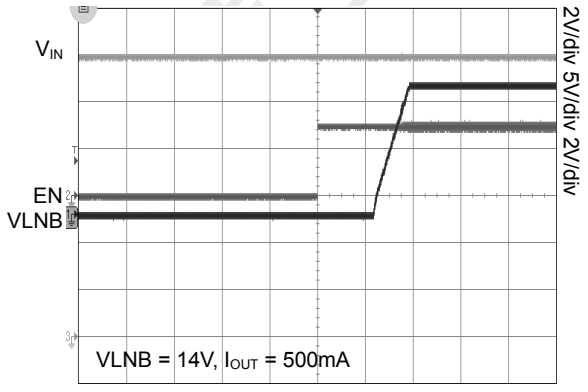
Load Regulation



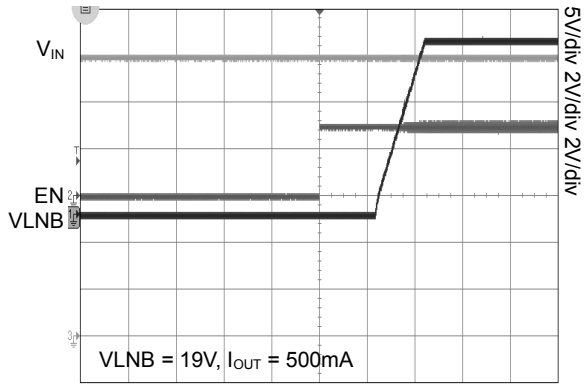
Load Regulation



Power On



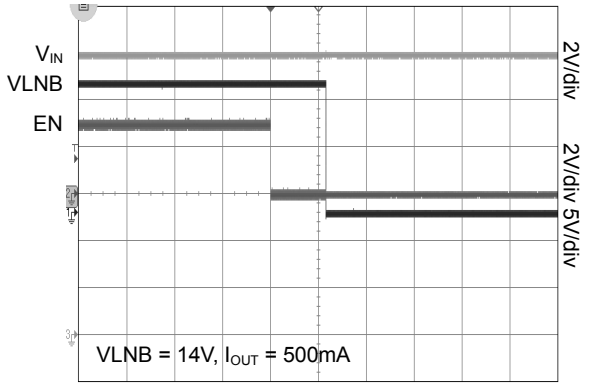
Power On



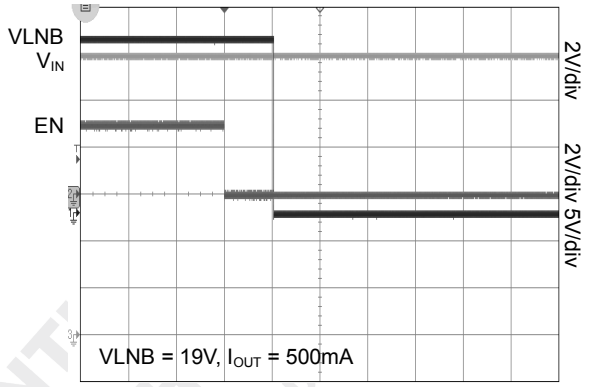
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

V_{IN} = 12V, C_{IN} = 10μF, C_{VSW} = 22μF × 2, L = 10μH and T_A = +25℃, unless otherwise noted.

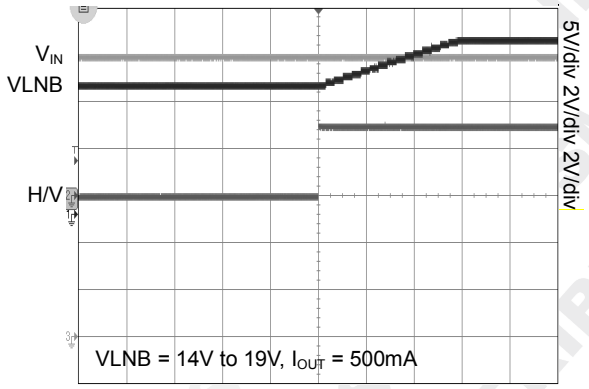
Power Off



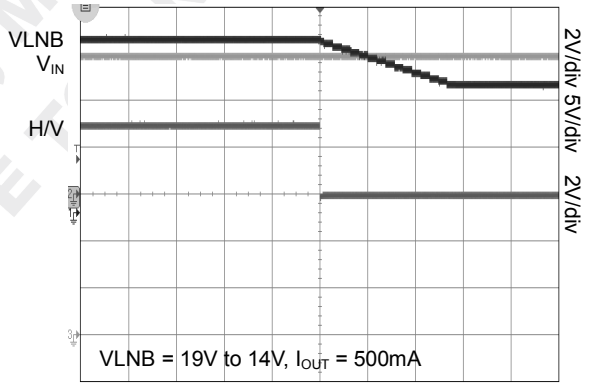
Power Off



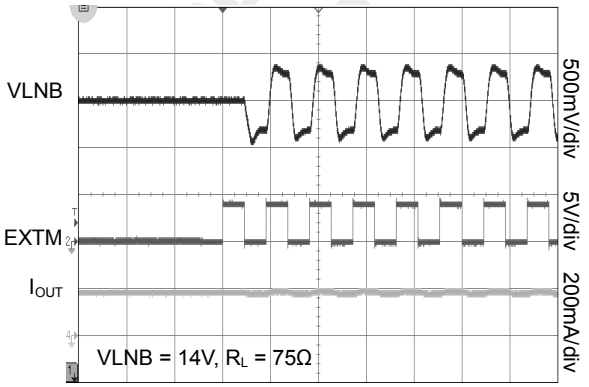
Power Change



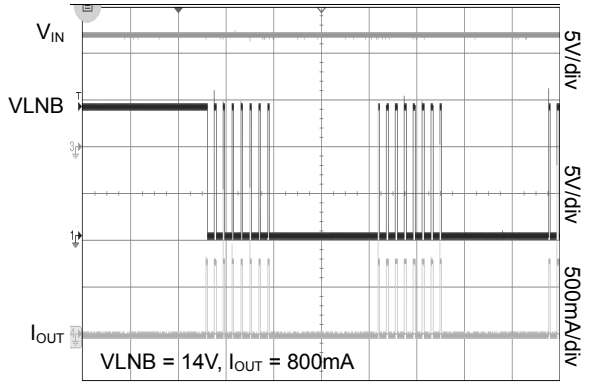
Power Change



22kHz Tone On



Over Load



FUNCTION, OPERATION AND APPLICATION

The SGM41286 cascades a high efficient boost and a linear regulator for generating 2 selectable 14V/19V output, for powering and controlling the antenna unit. With an internal synthesizer and an embedded controller, the SGM41286 modulates its output voltage, transmits control signal over the cable, in compliance with the specifications defined in the DiSEqC, the Digital Satellite Equipment Control Bus, in either repeater mode or synthesizer mode.

Charge Pump

Generates a supply voltage above the internal tracking regulator output to drive the linear regulator control.

Overload Handling

If the LNB output current >750mA and lasting for 200ms, or output current >3A and lasting for 30μs, the converter will shut down for 800ms and then retry to start. If retry for 8 times, the converter will shut down for 12s and then retry again.

Thermal Protection

When the junction temperature exceeds +160℃, the part will be shut down. Once the junction temperature is cooled enough, typically +130℃, the part will re-start automatically.

The DiSEqC Levels

A 22kHz tone signal is superimposed at the LNB output voltage as a carrier for DiSEqC command. This tone signal can be generated by feeding an external 22kHz clock at the EXTM pin. It can also be generated with its internal tone generator gated by control logic. The output stage of the regulator facilitates a push-pull circuit, so even at zero loading the tone at the output is still clear of distortion.

The SGM41286 only has circuit for signal transmission, which satisfies the level DiSEqC 1.X and those backwards.

Repeater or Synthesizer

The synthesizer controller circuit in the SGM41286 detects the level change of the EXTM input. When a rising edge is detected, the controller counts the time for an expected falling edge of 22kHz square wave in t_{SYNDLY}. If the falling does not happen, it steps down the VLNB for about $V_{PPTONE}/2$, and then modulates the VLNB with local synthesizer's 22kHz; and the falling edge comes within t_{SYNDLY}, the controller steps down the VLNB output for about $V_{PPTONE}/2$, repeats what is seen at the EXTM input.

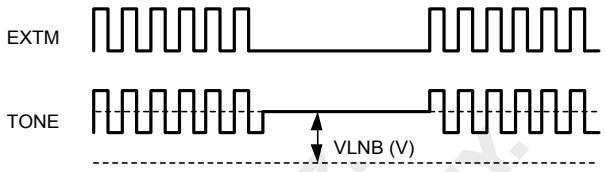


Figure 4. Tone and VLNB

Layout and Surge Absorbing Recommendations and In-rush handling

The booster works at high frequency, careful layout is helpful and even critical for assuring the stable operation, less ripple and EMC performance. See Figure 5 for a reference board layout used for the evaluation, which is proven good in the SGM41286's development test.

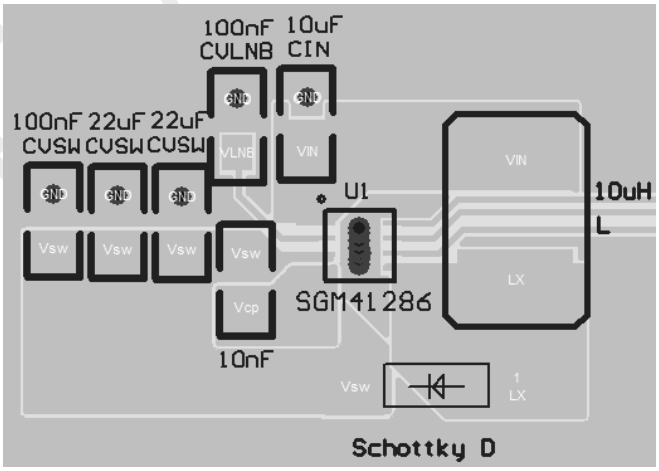


Figure 5. Reference Board Layout

Surging contributes to the operation down-time, absorbing circuit like the SGM40700 in addition to passive splitter and absorbing circuit is recommended for protection at both the in-door unit and the outdoor unit. See Figure 6 for a reference circuit with surge absorbing and splitter.

If excessive motor spin-staling current in-rush happens, the SGM41286 stops output for short while and resumes instantly for times. If the over-current does exist after times of instant retrials, the SGM41286 turns into longer interval retrial for safe concern.

FUNCTION, OPERATION AND APPLICATION (continued)

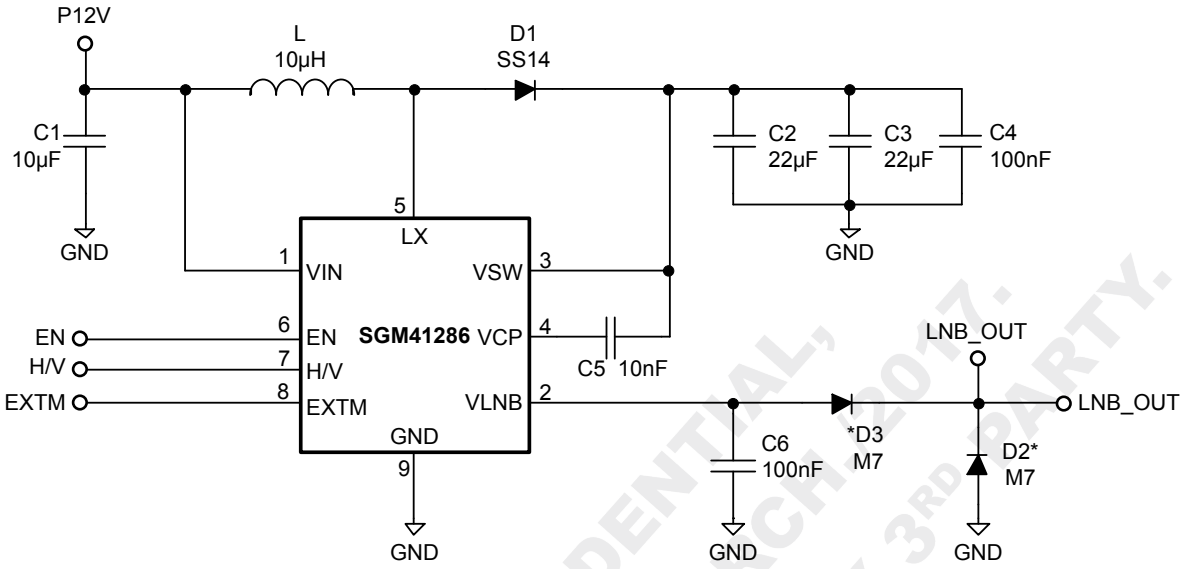
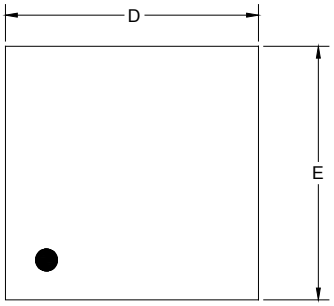


Figure 6. A Reference Circuit with Surge Absorbing Circuit and Splitter

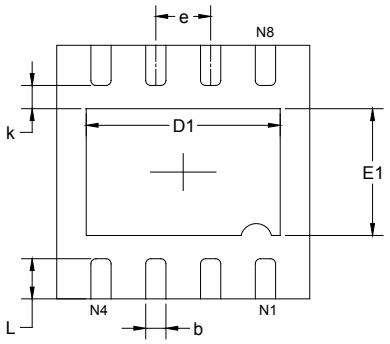
*D2, D3 for high voltage surge test

PACKAGE OUTLINE DIMENSIONS

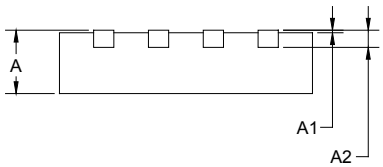
TDFN-3×3-8L



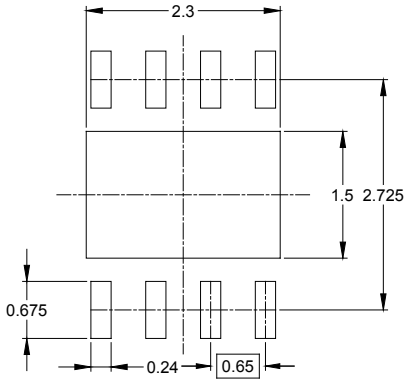
TOP VIEW



BOTTOM VIEW



SIDE VIEW

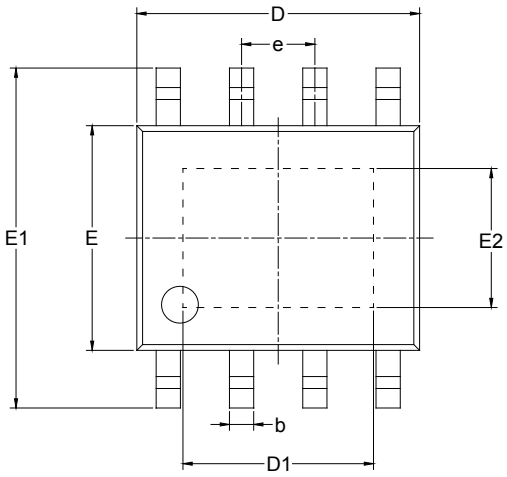


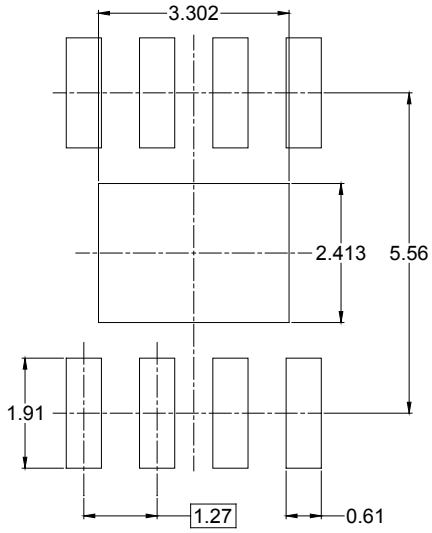
RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.200	2.400	0.087	0.094
E	2.900	3.100	0.114	0.122
E1	1.400	1.600	0.055	0.063
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.650 TYP		0.026 TYP	
L	0.375	0.575	0.015	0.023

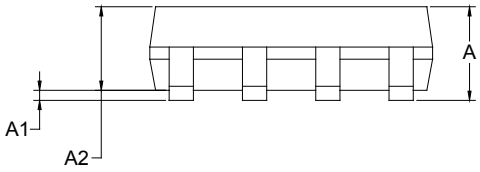
PACKAGE OUTLINE DIMENSIONS

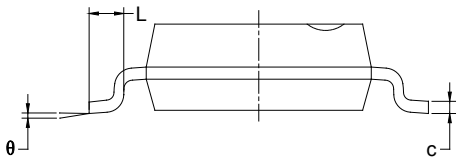
SOIC-8 (Exposed Pad)





RECOMMENDED LAND PATTERN (Unit: mm)

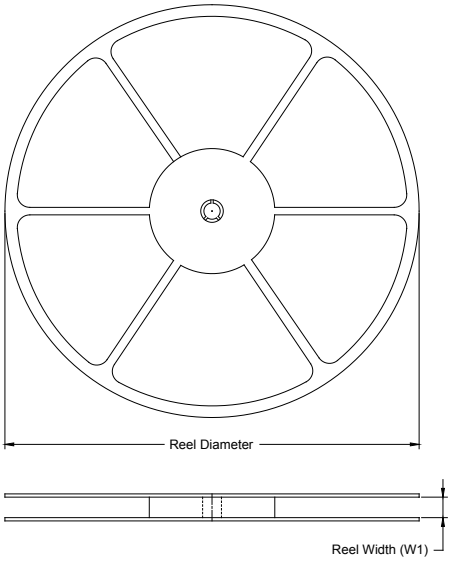




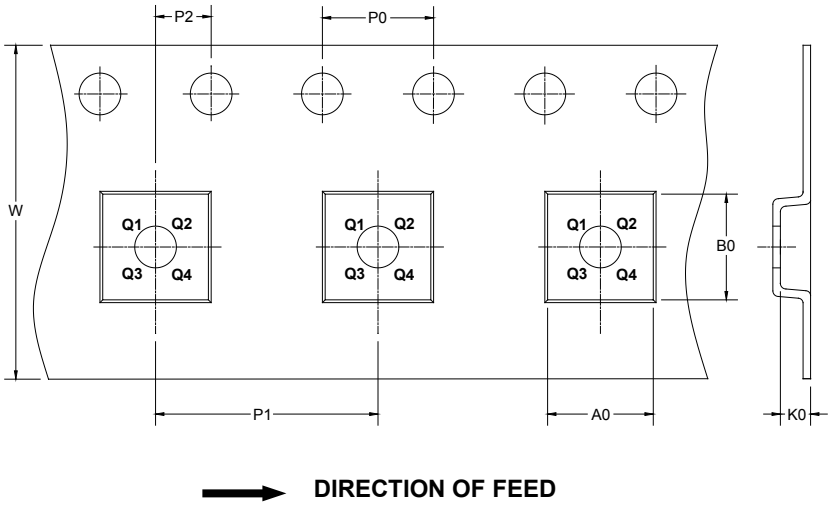
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A		1.700		0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

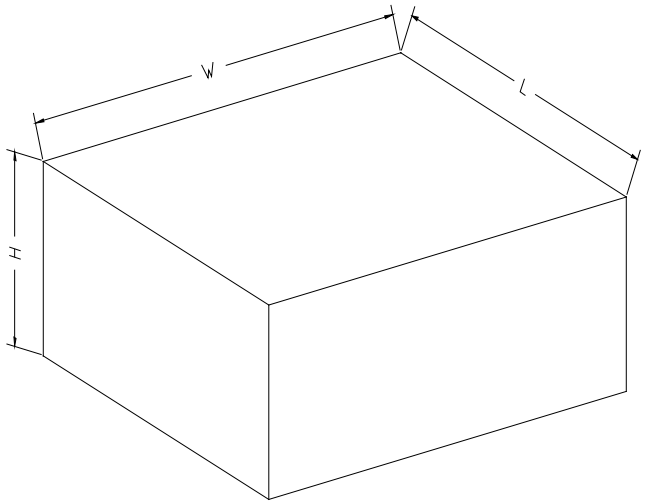
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-8L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1
SOIC-8 (Exposed Pad)	13″	12.4	6.40	5.40	2.10	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002