A product Line of
Diodes Incorporated

PI2EQX6804-A

6.5Gbps 4-Lane SAS2/SATA/XAUI ReDriver with Equalization & De-Emphasis

Features

- Up to 6.5Gbps SAS2/SATA/XAUI ReDriver
- Supporting 8 differential channels or 4 ports
- Pin strapped and I2C configuration controls (3.3V Tolerant)
- Adjustable receiver equalization
- Adjustable transmitter amplitude and de-emphasis
- 50-Ohm input/output termination
- Mux/Demux feature
- Channel loop-back
- OOB fully supported
- Single supply voltage, 1.2V ± 5%
- Power down modes
- Industrial temperature range: -40°C to 85°C
- Packaging (Pb-free & Green):
  - 100-contact LBGA

Description

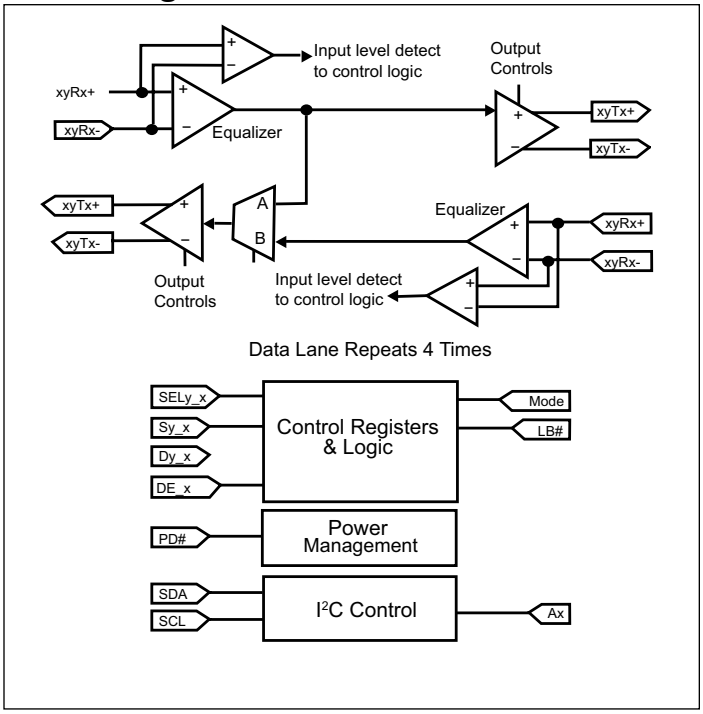
Diodes' PI2EQX6804-A is a low power, SAS2, SATA, XAUI signal ReDriver™. The device provides programmable equalization, amplification, and de-emphasis by either pin strapping option or I^2C control to optimize performance over a variety of physical mediums by reducing Inter-symbol interference.

PI2EQX6804-A supports eight 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or extends the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the ReDriver, whereas the integrated de-emphasis circuitry provides flexibility with signal integrity of the signal after the ReDriver.

In addition to providing signal re-conditioning, Diodes' PI2EQX6804-A also provides power management Stand-by mode operated by a Power Down pin, or through I^2C register.

Block Diagram



Pin Configuration (Top-Side View)

	1	2	3	4	5	6	7	8	9	10
A	VDD	B0TX-	B0TX+	VDD	SCL	SDA	VDD	B0RX+	B0RX-	VDD
B	A1RX+	GND	GND	A0RX-	DE_A	VDD	A0TX-	GND	GND	A1TX+
C	A1RX-	GND	GND	A0RX+	NC	PD#	A0TX+	GND	GND	A1TX-
D	VDD	B1TX+	B1TX-	VDD	D2_A	NC	VDD	B1RX-	B1RX+	VDD
E	SEL0_A	SEL1_A	SEL2_A	D0_A	D1_A	S0_A	NC	S1_A	SIG_A	NC
F	NC	SIG_B	S1_B	NC	S0_B	A1	SEL2_B	LB#	SEL1_B	SEL0_B
G	VDD	A2RX-	A2RX+	VDD	MODE	D0_B	VDD	A2TX+	A2TX-	VDD
H	B2TX+	GND	GND	B3TX-	DE_B	A0	B3RX-	GND	GND	B2RX+
J	B2TX-	GND	GND	B3TX+	NC	D1_B	B3RX+	GND	GND	B2RX-
K	VDD	A3RX+	A3RX-	VDD	D2_B	A4	VDD	A3TX-	A3TX+	VDD

Pin Description

Pin #	Pin Name	Type	Description
Data Signals			
C4 B4	A0RX+, A0RX-	I I	CML inputs for Channel A0, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0).
C7 B7	A0TX+, A0TX-	O O	CML outputs for Channel A0, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).
B1 C1	A1RX+, A1RX-	I I	CML inputs for Channel A1, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0).
B10 C10	A1TX+, A1TX-	O O	CML outputs for Channel A1, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).
G3 G2	A2RX+, A2RX-	I I	CML inputs for Channel A2, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0).
G8 G9	A2TX+, A2TX-	O O	CML outputs for Channel A2, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).
K2 K3	A3RX+, A3RX-	I I	CML inputs for Channel A3 with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0).
K9 K8	A3TX+, A3TX-	O O	CML outputs for Channel A3, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).
A8 A9	B0RX+, B0RX-	I I	CML inputs for Channel B0, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0).
A3 A2	B0TX+, B0TX-	O O	CML outputs for Channel B0, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).
D9 D8	B1RX+, B1RX-	I I	CML inputs for Channel B1, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0).
D2 D3	B1TX+, B1TX-	O O	CML outputs for Channel B1, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).
H10 J10	B2RX+, B2RX-	I I	CML inputs for Channel B2, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0).
H1 J1	B2TX+, B2TX-	O O	CML outputs for Channel B2, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).
J7 H7	B3RX+, B3RX-	I I	CML inputs for Channel B3, with internal 50-Ohm pull-down. Goes to high-impedance during power-down (PD#=0).
J4 H4	B3TX+, B3TX-	O O	CML outputs for Channel B3, with internal 50-Ohm pull-up. Goes to high-impedance during power-down (PD#=0).

Pin Description Cont.

Pin #	Pin Name	Type	Description
Control Signals			
H6, F6, K6	A0, A1, A4	I	I^2C programmable address bit A0, A1 and A4 with 100K-Ohm internal pull up
E4 E5 D5	D0_A D1_A D2_A	I	Selection pins for Channel Ax de-emphasis (See de-emphasis Configuration Table) with100K-Ohm internal pull up
G6 J6 K5	D0_B D1_B D2_B	I	Selection pins for Channel Bx de-emphasis (See De-emphasis Configuration Table) with100K-Ohm internal pull up
B5	DE_A	I	De-emphasis enable input for Channel A0, A1, A2 and A3 with internal 100K-Ohm pull-up resistor. Set high selects output half-bit-de-emphasis and set low selects output full-bit-de-emphasis.
H5	DE_B	I	De-emphasis enable input for Channel B0, B1, B2 and B3 with internal 100K-Ohm pull-up resistor. Set high selects output half-bit-de-emphasis and set low selects output full-bit-de-emphasis.
F8	LB#	I	Input with internal 100K-Ohm pull-up resistor. LB# = High or open for normal operation. LB# = Low for loopback connection of A_RX to A_TX and B_TX.
G5	MODE	I	Input switch between pin control and I^2C control with internal 100K-Ohm pull-up resistor. A LVCMOS high level selects input pin control, and disables I^2C operation. Note, during startup, input status of the control pin (LB#, PD#, SEL0-2_A/B, D0-2_A/B, S0-1_A/B, DE_A/B) will be latched to the initial state of some I^2C control bits only once.
C5, D6, E7, E10, F1, F4, J5	NC		Do Not Connect (Reserved for future use.)
C6	PD#	I	Input with internal 100K-Ohm pull-up resistor, PD# =High or open is normal operation, PD# =Low disable the IC, and set IC to power down mode, both input and output go Hi-Z.
E6 E8	S0_A S1_A	I	Selection pins for Channel Ax output level (see Output Swing Configuration Table) with100K-Ohm internal pull up
F5 F3	S0_B S1_B	I	Selection pins for Channel Bx output level (see Output Swing Configuration Table) with 100K-Ohm internal pull up
A5	SCL	I	I2C SCL clock input. Up to 3.3V input tolerance.
A6	SDA	I/O	I2C SDA data input/output. Up to 3.3V input tolerance
E1, E2, E3	SEL[0:2]_A	I	Selection pins for Channel Ax Equalization (see Equalizer Configuration Table) with 100K-Ohm internal pull up
F10, F9, F7	SEL[0:2]_B	I	Selection pins for Channel Bx Equalization (see Equalizer Configuration Table) with 100K-Ohm internal pull up
E9	SIG_A	O	Signal detect output pin for Channel A0. SIG_A=High represents a input signal > threshold at the differential inputs.
F2	SIG_B	O	Signal detect output pin for Channel B0. SIG_B=High represents a input signal > threshold at the differential inputs.

Pin Description Cont.

Pin #	Pin Name	Type	Description
Power Pins			
B2, B3, B8, B9, C2, C3, C8, C9, H2, H3, H8, H9, J2, J3, J8, J9	GND	PWR	Supply Ground
A1, A4, A7, A10, B6, D1, D4, D7, D10, G1, G4, G7, G10, K1, K4, K7, K10	VDD	PWR	1.2V Supply Voltage

DESCRIPTION of OPERATION

Configuration Modes

Device configuration can be performed in two ways depending on the state of the MODE input. MODE determines whether IC configuration is from the input pins or via I^2C control. Note that the MODE pin is not latched, and is always active to enable or disable I^2C access. When MODE is set high, the configuration input pins determine the configuration operating state aND changes to the input configuration pins will change the operating mode.

When the MODE pin is low, programming of all control registers via I^2C is allowed. During initial power-on, the value at the configuration input pins: LB#, PD#, DE_A, DE_B, SEL0_A, SEL1_A, SEL2_A, D0_A, D1_A, D2_A, S0_A, S1_A, SEL0_B, SEL1_B, SEL2_B, D0_B, D1_B, D2_B, S0_B, S1_B, will be latched to the configuration registers as initial startup states.

Equalizer Configuration

The PI2EQX6804-A input equalizer compensates for signal attenuation and Inter-Symbol Interference (ISI) resulting from long signal traces or cables, vias, signal crosstalk and other factors, by boosting the gain of high-frequency signal components. Because either too little, or too much, signal compensation may be non-optimal, eight levels are provided to adjust for any application.

Equalizer configuration is performed in two ways determined by the state of the MODE pin. When the device first powers up, the SELx_[A:B] input pins are read into the appropriate control registers to set the equalization characteristic. If the MODE pin is low, reprogramming of these control registers via I^2C is allowed.

Each group of four channels, A and B, has separate equalization control, and all four channels within the group are assigned the same configuration state. The Equalizer Selection table below describes pin strapping options and associated operation of the equalizer. Refer to the section on I^2C programming for information on software configuration of the equalizer.

Equalizer Selection

SEL2_[A:B]	SEL1_[A:B]	SEL0_[A:B]	@1.5GHz	@3.0GHz
0	0	0	0.8dB	1.5dB
0	0	1	1.0dB	1.9dB
0	1	0	1.5dB	3.2dB
0	1	1	2.5dB	5.2dB
1	0	0	3.5dB	6.9dB
1	0	1	4.4dB	8.3dB
1	1	0	5.9dB	10.4dB
1	1	1	8.7dB	13.8dB

Output Configuration

The PI2EQX6804-A provides flexible output strength and de-emphasis controls to provide the optimum signal to pre-compensate for losses across long trace or noisy environments so that the receiver gets a clean eye opening. Control of output configuration is grouped for the A and B channels, so that each channel within the group has the same setting.

Output configuration is performed in two ways depending on the state of the MODE pin. When the device first powers up, the Sx_[A:B], and Dx_[A:B] input pins are read into the appropriate control registers to set the power-on state. If the MODE pin is low, reprogramming of these control registers via I^2C is allowed.

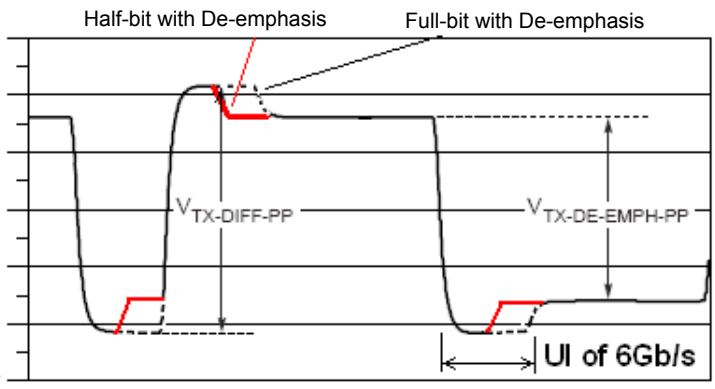
Output Swing Control

S1_[A:B]	S0_[A:B]	Swing (Differential)
0	0	1V
0	1	0.5V
1	0	0.7V
1	1	0.9V

The Output Swing Control table shows available configuration settings for output level control, as specified using the Sx_y pins and registers. Output swing settings are independant of the data rate.

Output De-emphasis Adjustment

De-emphasis settings are determined by the state of the DEx_y input pins and configuration registers, as shown in the Output De-emphasis table below. Half-bit-de-emphasis is selected as the default power-on mode, but can be changed to full-bit-de-emphasis via reprogramming the Loopback and De-emphasis Control register using the I2C interface. Output de-emphasis settings are independant of the data rate.

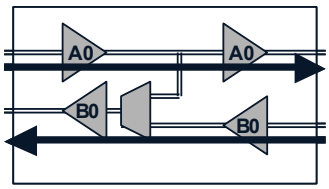
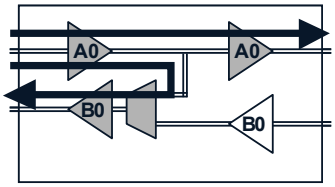
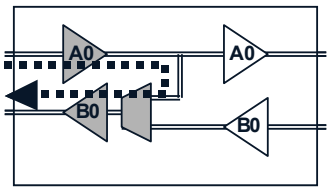
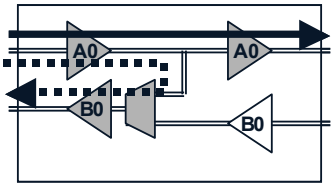
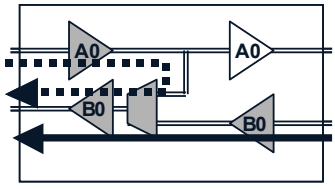


D2_[A:B]	D1_[A:B]	D0_[A:B]	De-emphasis
0	0	0	0dB
0	0	1	2.5dB
0	1	0	3.5dB
0	1	1	4.5dB
1	0	0	5.5dB
1	0	1	6.5dB
1	1	0	7.5dB
1	1	1	8.5dB

Input Level Detect

An input level detect and output squelch function is provided on each channel to eliminate re-transmission of input noise. A continuous signal level below the V_{th-} threshold causes the output driver to drive both the plus and minus signal pair to the common mode voltage.

Loopback Operation

Loopback Modes		CONDITIONS
	NORMAL MODE A0Rx to A0Tx, B0Rx to B0Tx	LB_A0B0# = 1 INDIS_A0 = 0 OUTDIS_A0 = 0 INDIS_B0 = 0 OUTDIS_B0 = 0
	BROADCAST MODE A0Rx to A0Tx and B0Tx	LB_A0B0# = 0 INDIS_A0 =0 OUTDIS_A0 = 0 INDIS_B0 = 1 OUTDIS_B0 = 0
	LOOPBACK MODE A0Rx to B0Tx	LB_A0B0# = 0 INDIS_A0 = 0 OUT_DIS_A0 = 1 INDIS_B0 = 1 OUTDIS_B0 = 0
	DEMUX MODE Solid Line A0Rx to A0Tx	LB_A0B0# = 1 INDIS_A0 = 0 OUTDIS_A0 = 0 INDIS_B0 = 1 OUTDIS_B0 =1
	DEMUX MODE Dashed Line A0Rx to B0Tx	LB_A0B0# = 0 INDIS_A0 = 0 OUTDIS_A0 = 1 INDIS_B0 = 1 OUTDIS_B0 = 0
	MUX MODE Solid Line B0Rx to B0Tx	LB_A0B0# = 1 INDIS_A0 = 1 OUTDIS_A0 = 1 INDIS_B0 = 0 OUTDIS_B0 = 0
	MUX MODE Dashed Line A0Rx to B0Tx	LB_A0B0# = 0 INDIS_A0 = 0 OUTDIS_A0 = 1 INDIS_B0 = 1 OUTDIS_B0 = 0

Each lane provides a loopback mode for test purposes which is controlled by a strapping pin and I^2C register bit. The LB# pin controls all lanes together. When this pin is high normal data mode is enabled. When LB# is low the loopback feature is enabled. The adjacent figure diagrams this operation. Loopback is not intended to be dynamically switched, and the normal system application is to initialize to one configuration or the other.

The Loopback mode can also support mux/demux operation. Using I^2C configuration, unused inputs and outputs can be disabled to minimize power and noise.

I²C Operation

The integrated I²C interface operates as a slave device, supporting standard rate operation of 100Kbps, with 7-bit addressing mode. The data byte format is 8 bit bytes, and supports the format of indexing to be compatible with other bus devices. The index, or dummy byte will have no effect on the PI2EQX6804-A operation. The bytes must be accessed in sequential order from the lowest to the highest byte with the ability to stop after any complete byte has been transferred. Address bits A4, A1 and A0 are programmable to support multiple chips environment. The Data is loaded until a Stop sequence is issued.

Note that the I²C inputs, SCL and SDA operate at 1.2V logic levels.

Configuration Register Summary

Byte	Mnemonic	Function
0	SIG	Signal Detect, indicates valid input signal level
1	RSVD	Reserved for future use
2	LBDEC	Loopback and De-emphasis Control, provides for control of the loopback function and De-emphasis mode (Half-bit or Full-bit)
3	INDIS	Channel Input Disable, controls whether s channels input buffer is enabled or disabled
4	OUTDIS	Channel Output Disable, controls whether a channel output buffer is enabled or disabled.
5	RSVD	Reserved for future use
6	PWR	Power Down Control, enables power down for each channel individually
7	RSVD	Reserved for future use
8	AEOC	A-Channels Equalizer and Output Control
9	BEOC	B-Channels Equalizer and Output Control
10	RSVD	Reserved for future use
11	RSVD	Reserved for future use

Register Description

BYTE 0 - Signal Detect (SIG)

SIG_xy=0=low input signal, SIG_xy=1=valid input signal

Bit	7	6	5	4	3	2	1	0
Name	**SIG_A0**	**SIG_B0**	**SIG_A1**	**SIG_B1**	**SIG_A2**	**SIG_B2**	**SIG_A3**	**SIG_B3**
Type	R	R	R	R	R	R	R	R
Power-on State	X	X	X	X	X	X	X	X

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Signal Detect register provides information on the instantaneous status of the channel input from the Input Level Threshold Detect circuit. If the input level falls below the V_{th-} level the relevant SIG_xy bit will be 0, indicating a low-level noise or electrical idle input, resulting in the outputs going to the high-impedance off state or squelch mode. If the input level is above V_{th-}, then SIG_xy is 1, indicating a valid input signal, and active signal recovery operation.

BYTE 1 - Reserved

Reserved Byte 1 is visible via the I^2C interface. This is a read-only byte with an undefined initial state after power-up. This byte is reserved for future use.

BYTE 2 - Loopback and De-emphasis Control Register (LBDEC)

LB_xyxy#=0=loopback mode, LB_xyxy#=1=normal mode, DE_x=0=Full-bit-de-emphasis, DE_x=1=Half-bit-de-emphasis

Bit	7	6	5	4	3	2	1	0
Name	**LB_A0B0#**	**LB_A1B1#**	**LB_A2B2#**	**LB_A3B3#**	**DE_A**	**DE_B**	**rsvd**	**rsvd**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Power-on State	LB#	LB#	LB#	LB#	DE_A	DE_B	X	X

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

Individual control for each lane is provided for the loopback function via this register.

BYTE 3 - Channel Input Disable (INDIS)

INDIS_xy=0=enable input, INDIS_xy=1=disable input

Bit	7	6	5	4	3	2	1	0
Name	**INDIS_A0**	**INDIS_B0**	**INDIS_A1**	**INDIS_B1**	**INDIS_A2**	**INDIS_B2**	**INDIS_A3**	**INDIS_B3**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	0	0	0	0	0	0	0	0

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Channel Input Disable register, provides control over the input buffer of each channel independently. When and INDIS_xy bit is logic 1, then the input buffer is switched off and the input termination is high impedance. This feature can be used for PCB testing, and when only one input is used during Loopback as a demux function. When INDIS_xy is at a logic 0 state then the input buffer is enabled (normal operating mode).

BYTE 4 - Channel Output Disable (OUTDIS)

ODIS_xy=0=enable output, ODIS_xy=1=disable output

Bit	7	6	5	4	3	2	1	0
Name	**ODIS_A0**	**ODIS_B0**	**ODIS_A1**	**ODIS_B1**	**ODIS_A2**	**ODIS_B2**	**ODIS_A3**	**ODIS_B3**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	0	0	0	0	0	0	0	0

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Channel Output Disable register, allows control over the output buffer of each channel independently. When and OUTDIS_xy bit is logic 1, then the output buffer is switched off and the termination is high impedance. This feature can be used for PCB testing, and when only one output is used during Loopback as a mux function. When INDIS_xy is at a logic 0 state then the input buffer is enabled (normal operating mode).

BYTE 5 - Reserved

Reserved Byte 5 is visible via the I^2C interface. This is a R/W byte with an undefined initial power-on state. This byte is reserved for future use. This byte must be written to all "1's" (FFh).

BYTE 6 - Power Down Control (PWR)

PD_xy# =0=channel off/power down, PD_xy# =1=normal operation, Latch from PD# input at startup

Bit	7	6	5	4	3	2	1	0
Name	**PD_A0#**	**PD_B0#**	**PD_A1#**	**PD_B1#**	**PD_A2#**	**PD_B2#**	**PD_A3#**	**PD_B3#**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	PD#	PD#	PD#	PD#	PD#	PD#	PD#	PD#

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The Power Down Control register allows for individual control over each channel for power savings. When PD_xy# is logic 0 the channel is turned off. When PD_xy# is 1 then the channel is enabled for normal operation.

BYTE 7 - Reserved

Reserved Byte 7 is visible via the I^2C interface. This is a R/W byte with an FFh initial power-on state. This byte is reserved for future use. This byte must be written to all "1's" (FFh).

BYTE 8 - A-Channels Equalizer and Output Control (AEOC)

SELx_A: Equalizer configuration, Dx_A: De-emphasis control, Sx_A: Output level control (see Configuration Table)

Bit	7	6	5	4	3	2	1	0
Name	**SEL0_A**	**SEL1_A**	**SEL2_A**	**D0_A**	**D1_A**	**D2_A**	**S0_A**	**S1_A**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	SEL0_A	SEL1_A	SEL2_A	D0_A	D1_A	D2_A	S0_A	S1_A

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The A-Channels Equalizer and Output Control register is used to control the configuration of the input equalizer and output de-emphasis and levels of the four A channels. These register bits are loaded from the input configuration pins of the same name at power-on. These bits may be changed if the MODE# input is set to allow I^2C configuration. Please refer to the tables (1) Equalizer Configuration, (2) Output Swing Configuration and (3) Output De-emphasis Configuration earlier in this document for setting information. All four A channels get the same configuration settings.

BYTE 9 - B-Channels Equalizer and Output Control (BEOC)

SELx_B: Equalizer configuration,

Dx_B: De-emphasis control,

Sx_B: Output level control (see Configuration Table)

Bit	7	6	5	4	3	2	1	0
Name	**SEL0_B**	**SEL1_B**	**SEL2_B**	**D0_B**	**D1_B**	**D2_B**	**S0_B**	**S1_B**
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Power-on State	SEL0_B	SEL1_B	SEL2_B	D0_B	D1_B	D2_B	S0_B	S1_B

Note: R=Read only, W=Write only, R/W=Read and Write, X=Undefined, rsvd=reserved for future use

The B-Channels Equalizer and Output Control register is used to control the configuration of the input equalizer and output de-emphasis and levels of the four B channels. These register bits are loaded from the input configuration pins of the same name at power-on. These bits may be changed if the MODE# input is set to allow I^2C configuration. Please refer to the tables (1) Equalizer Configuration, (2) Output Swing Configuration and (3) Output De-emphasis Configuration earlier in this document for setting information. All four B channels get the same configuration settings.

BYTE 10 - Reserved

Reserved Byte 10 is visible via the I^2C interface. This byte is R/W and is initialized to 0000 0000 at power up. It is used for IC manufacturing test purposes and should not be changed for normal operation.

BYTE 11 - Reserved

Reserved Bytes 10 is visible via the I^2C interface. This byte is R/W and is initialized to 1110 1111 at power up. It is used for IC manufacturing test purposes and should not be changed for normal operation.

Transferring Data

Every byte put on the SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first (see the I^2C Data Transfer diagram). The PI2EQX6804-A will never hold the clock line SCL LOW to force the master into a wait state.

Note: Byte-write and byte-read transfers have a fixed offset of 0x00, because of the very small number of configuration bytes. An offset byte presented by a host to the PI2EQX6804-A is not used.

Addressing

Up to eight PI2EQX6804-A devices can be connected to a single I^2C bus. The PI2EQX6804-A supports 7-bit addressing, with the LSB indicating either a read or write operation. The address for a specific device is determined by the A0, A1 and A4 input pins.

Address Assignment							
A6	**A5**	**A4**	**A3**	**A2**	**A1**	**A0**	**R/W**
1	1	Program	0	0	Programmable		1=R, 0=W

Acknowledge

Data transfer with acknowledge is required from the master. When the master releases the SDA line (HIGH) during the acknowledge clock pulse, the PI2EQX6804-A will pull down the SDA line during the acknowledge clock pulse so that it remains stable LOW during the HIGH period of this clock pulse as indicated in the I^2C Data Transfer diagram. The PI2EQX6804-A will generate an acknowledge after each byte has been received.

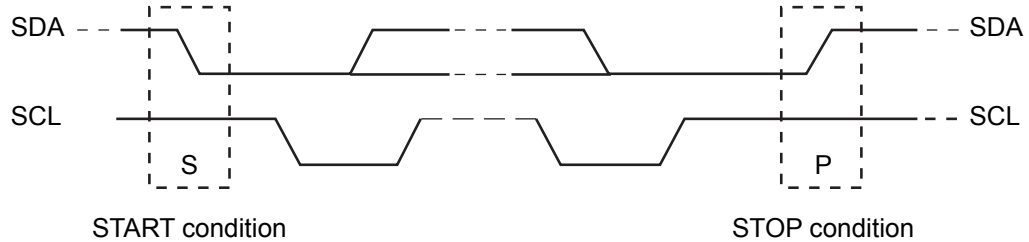
Data Transfer

A data transfer cycle begins with the master issuing a start bit. After recognizing a start bit, the PI2EQX6804-A will watch the next byte of information for a match with its address setting. When a match is found it will respond with a read or write of data on the following clocks. Each byte must be followed by an acknowledge bit, except for the last byte of a read cycle which ends with a stop bit. For a write cycle, the first data byte following the address byte is a dummy or fill byte that is not used by the PI2EQX6804-A. This byte is provided to provided compatibility with systems implementing 10-bit addressing. Data is transferred with the most significant bit (MSB) first.

I^2C Data Transfer

Start & Stop Conditions

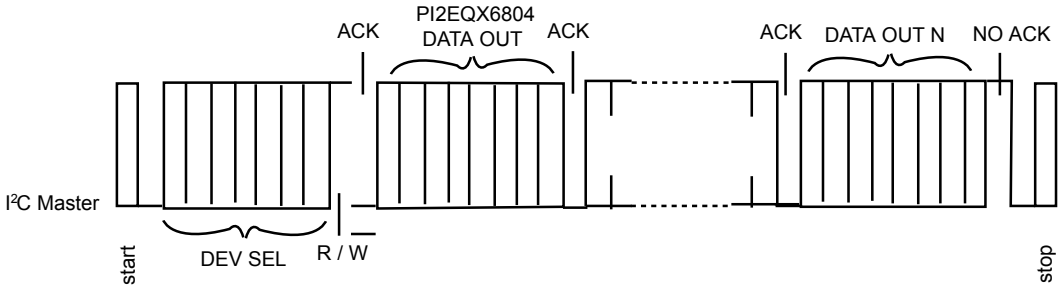
A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition, as shown in the figure below.



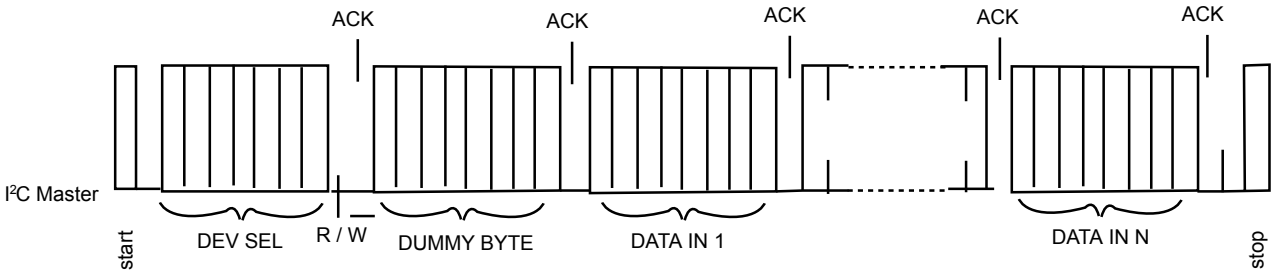
I^2C START and STOP conditions.

I²C Data Transfer

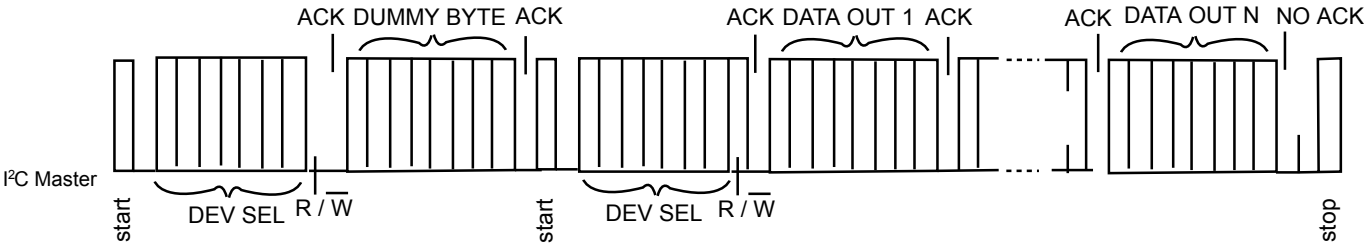
1. Read sequence



2. Write sequence



3. Combined sequence



Notes:
1. only block read and block write from the lowest byte are supported for this application.
2. for some I2C application, an offset address byte will be presented at the second byte in write command, which is called dummy byte here and will be simply ignored in this application for correct interoperation.

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature . . . . . –65°C to +150°C
Supply Voltage to Ground Potential . . . . . –0.5V to +2.5V
DC SIG Voltage . . . . . –0.5V to VDD +0.5V
Current Output . . . . . –25mA to +25mA
Power Dissipation Continuous 1W
Operating Temperature . . . . . -40 to +85°C
ESD, Human Body Model, SCL, SDA. . . . . ±2kV

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics

Power Supply Characteristics (V_{DD} = 1.2V ± 5%, T_A = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$I_{DDactive}$	Power supply current - active	All channels switching @ 6.5 Gbps			800	mA
$I_{DDstandby}$	Power supply current - standby	PD# = 0		1	5	mA

AC Performance Characteristics (V_{DD} = 1.2V ± 5%, T_A = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{pd}	Channel latency from input to output			750		ps

CML Receiver Input (V_{DD} = 1.2V ± 5%, T_A = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ZRX-DC	DC Input Impedance		40	50	60	Ohms
ZRX-DIFF-DC	DC Differential Input Impedance		80	100	120	Ohms
VRX-DIFFP-P	Differential Input Peak-to-peak Voltage		0.2		1.2	V
VRX-CM-ACP	AC Peak Common Mode Input Voltage				150	mV
V_{th-}	Signal detect threshold voltage		75	150	200	mV ppd

Equalizer

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
J_{RS-T}	Residual jitter	Total			0.3	Ulp-p
J_{RS-D}	Residual jitter	Deterministic			0.2	Ulp-p
J_{RM}	Random jitter	Note 2		1.5		psrms

Notes

1. K28.7 pattern is applied differentially at point A as shown in AC test circuit (see figure).

2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. Jitter is measured at 0V at point C of the AC test circuit (see figure).

CML Transmitter Output (V_{DD} = 1.2V ± 5%, T_A = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Z_{OUT}	Output resistance	Single ended	40	50	60	Ohms
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	Ohms
$V_{TX-DIFFP-P0}$	Differential Peak-to-Peak Ouput Voltage VTX-DIFFP-P = 2 * | VTX-D+ - VTX-D- |	S[1:0] = 00, 0dB de-emphasis	0.8	1	1.2	V
		S[1:0] = 01, 0dB de-emphasis	0.3	0.5	0.7	
		S[1:0] = 10, 0dB de-emphasis	0.5	0.7	0.9	
		S[1:0] = 11, 0dB de-emphasis	0.7	0.9	1.1	
V_{TX-C}	Common-Mode Voltage | VTX-D+ + VTX-D- | / 2			V_{DD}-0.6		V
t_F, t_R	Transition Time	20% to 80%			150	ps
C_{TX}(1)	AC Coupling Capacitor		0.3	4.7	12	nF

Notes:

1. Recommended external blocking capacitor.

Digital I/O DC Specifications (V_{DD} = 1.2V ± 5%, T_A = -40 to 85°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC input logic high		V_{DD}/2 +0.2		V_{DD}+0.3	V
V_{IL}	DC input logic low		-0.3		V_{DD}/2 -0.2	
V_{OH}	DC output logic high	I_{OH} = -4mA	V_{DD}-0.4			
V_{OL}	DC output logic low	I_{OL} = 4mA			0.4	
V_{hys}	Hysteresis of Schmitt trigger input		0.1			

Digital I/O DC Specifications Cont.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{IH} (1)	Input high current				250	µA
I_{IL1} (2)	Input low current		-250			
I_{IL2} (3)	Input low current		-250			

Notes:
1. Includes input signals A1, A2, A4, Dx_[A:B], DE_[A:B], LB#, MODE#, PD#, Sx_[A:B], SCL, SDA, SEL_x[A:B]
2. For control inputs without pullups: SCL, SDA
3. Control inputs with pull-ups include: Dx_[A:B], DE_[A:B], LB#, MODE#, PD#, Sx_[A:B], SEL_x[A:B], A1, A2, A4

SDA and SCL I/O for I²C-bus (V_{DD} = 1.2 ± 5%, T_A = -40 to 85°C)

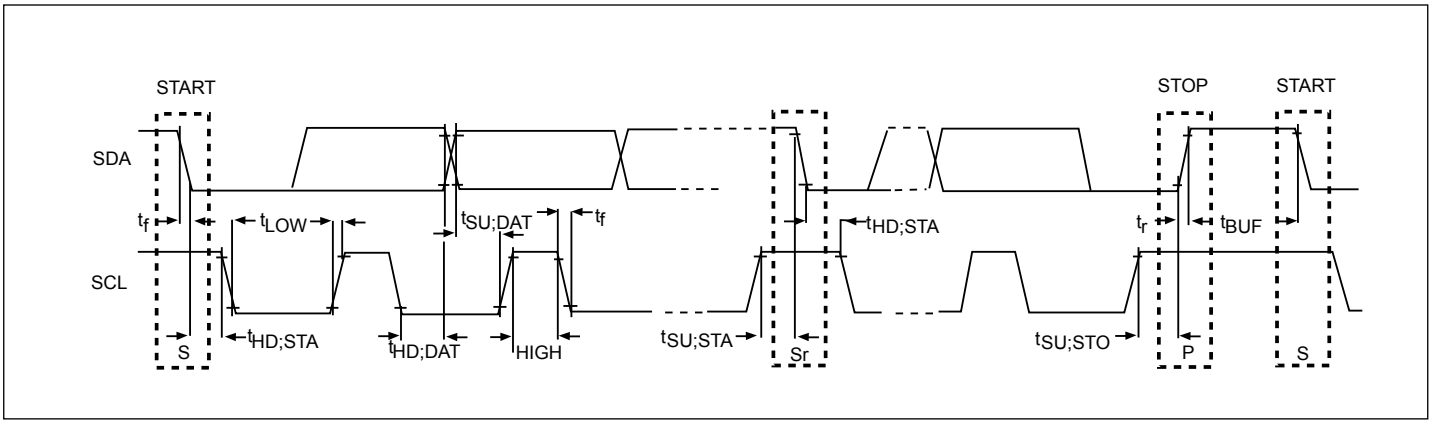
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	DC input logic high		0.85 x V_{DD}		3.6	V
V_{IL}	DC input logic low		-0.3		0.4	
V_{OL}	DC output logic low	I_{OL} = 3mA			0.4	
V_{hys}	Hysteresis of Schmitt trigger input		0.2			

Characteristics of the SDA and SCl bus lines for Standard Mode I²C-bus devices (1)

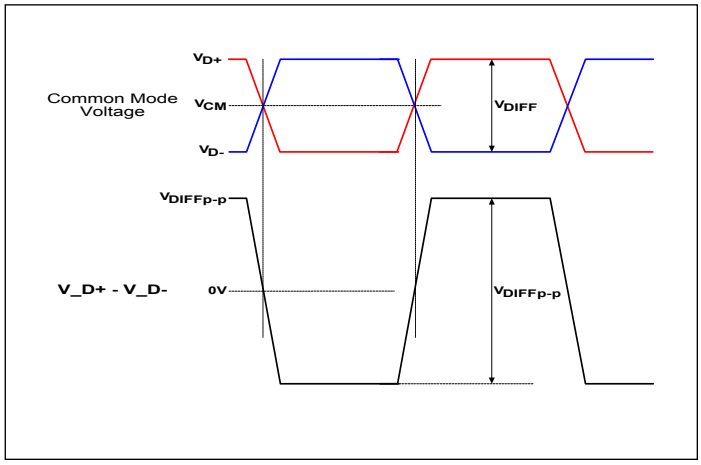
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{SCL}	SCL clock frequency		0		100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.		4.0		_	µs
t_{LOW}	LOW period of the SCL clock		4.7		_	
t_{HIGH}	HIGH period of the SCL clock		4.0		_	
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7		_	
$t_{HD;DAT}$	Data hold time		10		_	ns
$t_{SU;DAT}$	Data set-up time		250		_	ns
t_r	Rise time of both SDA and SCL signals		-		1000	
t_f	Fall time of both SDA and SCL signals				300	
$t_{SU;STO}$	Set-up time for STOP condition		4.0		_	µs
t_{BUF}	Bus free time between a STOP and STOP condition		4.7		_	
C_b	Capacitive load for each bus line		-		400	pF

Notes:

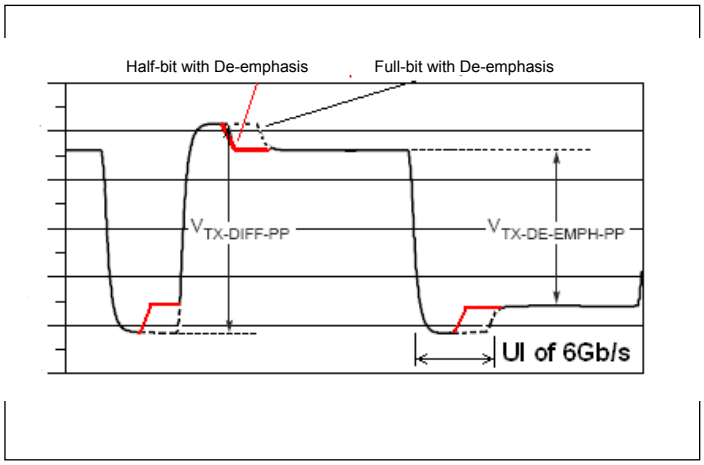
1. All values referred to VIH min and VIL max levels



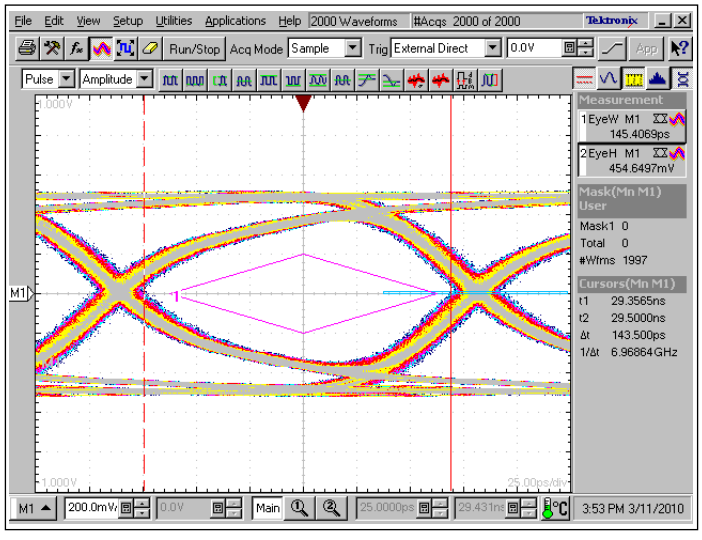
I²C Timing



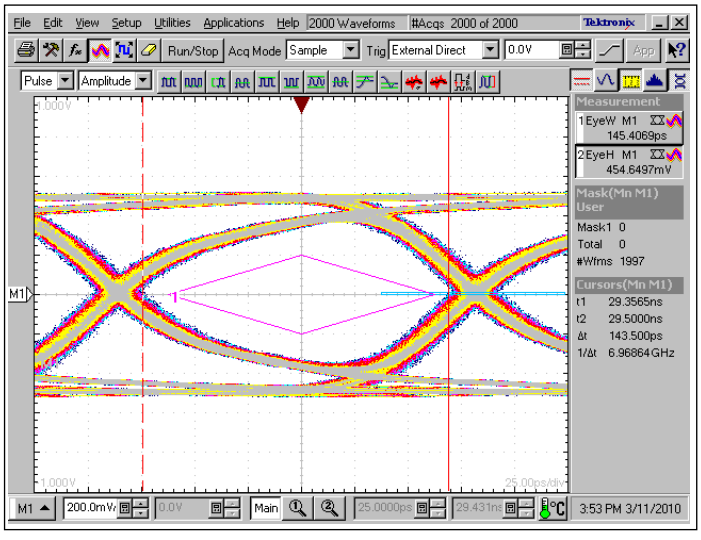
Definition of Differential Voltage and Differential Voltage Peak-to-Peak



Definition of De-emphasis

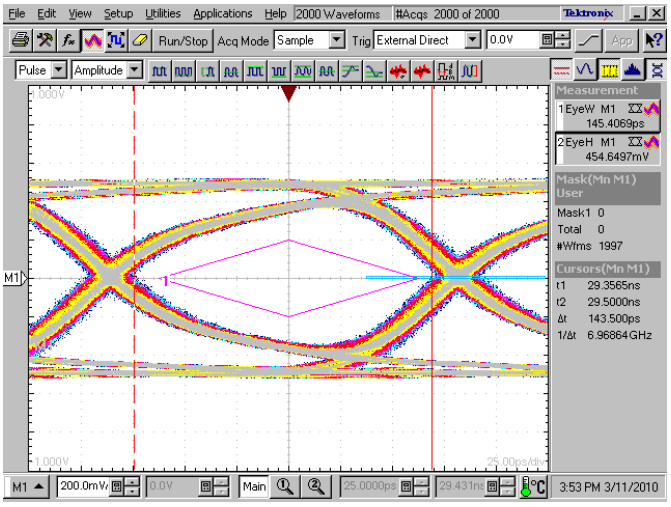


Input Eye

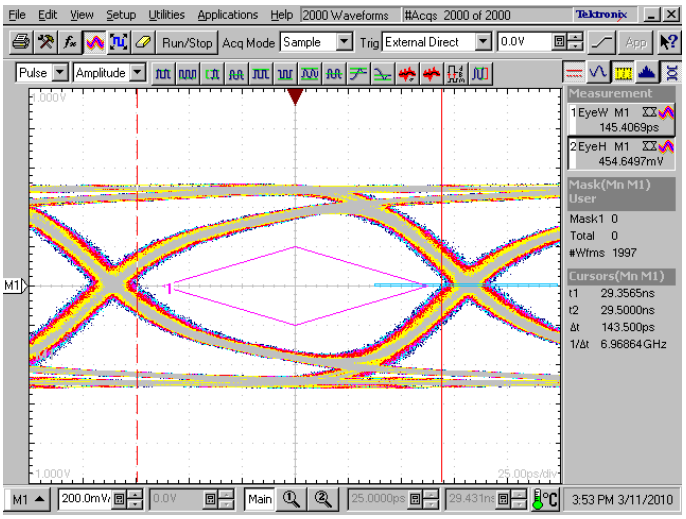


Output Eye

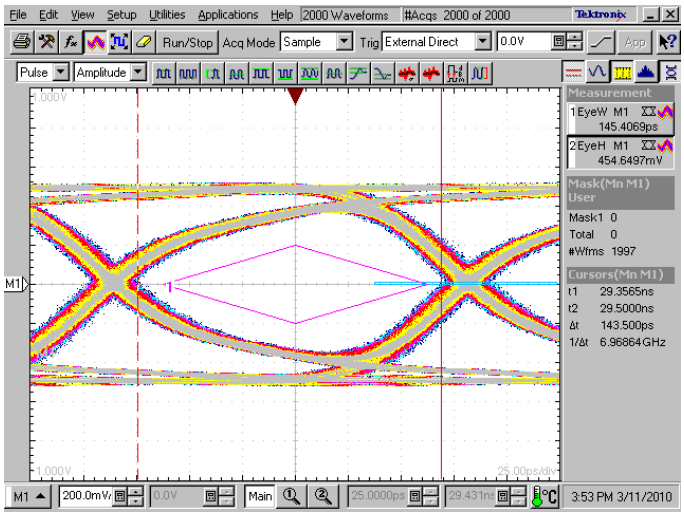
Signal Eyes @10dB input equalization, 24 inch FR4 input trace, 36 inch output cable



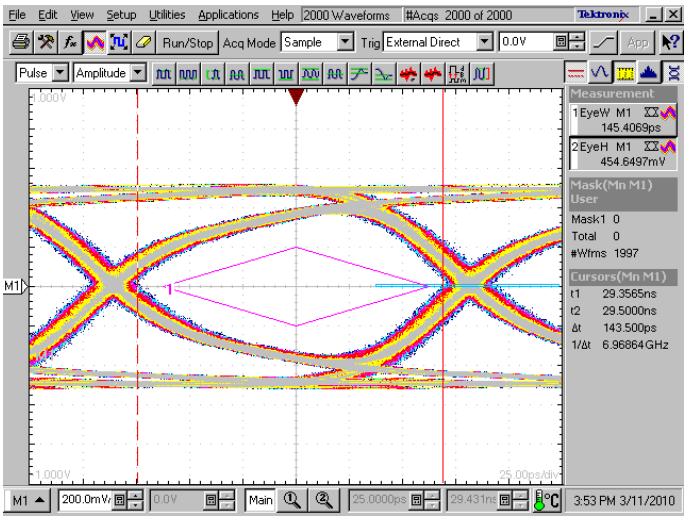
0.0 dB(Dx = 000)



3.5 dB(Dx = 010)

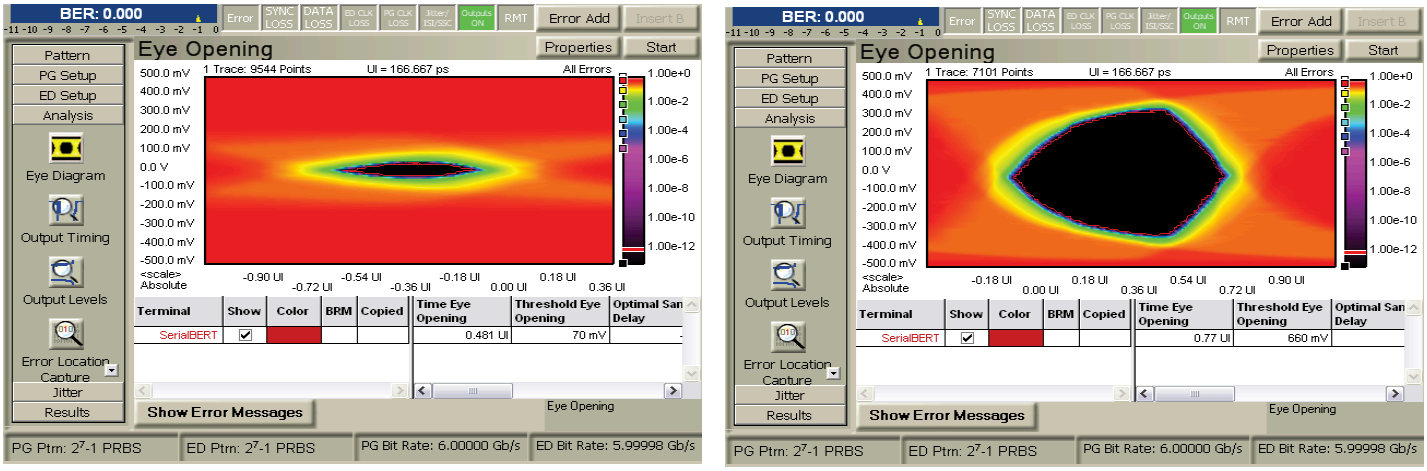


6.5 dB(Dx = 101)

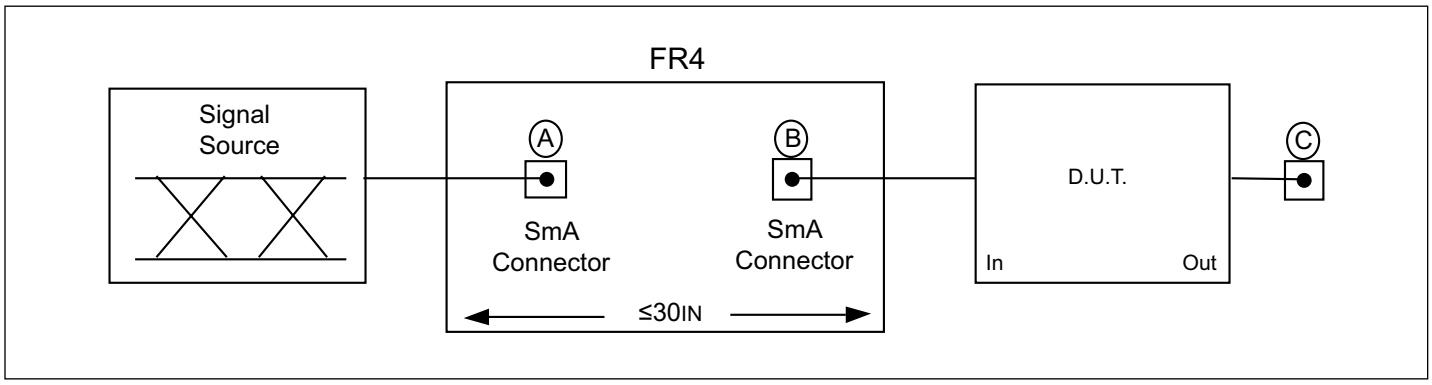


8.5 dB(Dx = 111)

Output De-emphasis Characteristics



Eye Diagrams 6.0Gbps (input left, output right)



AC Test Circuit Referenced in the Electrical Characteristic Table

Configuration Code Samples

The following examples, describe programming the PI2EQX6804-A via the I^2C interface.

Data Byte Format: HEX sequence (8 bit, MSB to LSB)

Byte Sequence Format

BYTE	Address	dummy-byte	byte0	byte1	byte2	byte3	byte4	byte5	byte6	byte7	byte8	byte9
DATA	A	d	0	1	2	3	4	5	6	7	8	9

Example 1

CHA=CHB: Equalization=1.5dB, De-emphasis=0dB, Swing=1.0V, No loopback

BYTE	A	d	0	1	2	3	4	5	6	7	8	9
DATA	C0	00	FF	FF	F0	00	00	FF	FF	FF	00	00

Example 2

Channel A: Equalization=1.5dB, De-emphasis=6.5dB, Swing=1.0V, No loopback

Channel B: Equalization=6.9dB, De-emphasis=0dB, Swing=0.7V, No loopback

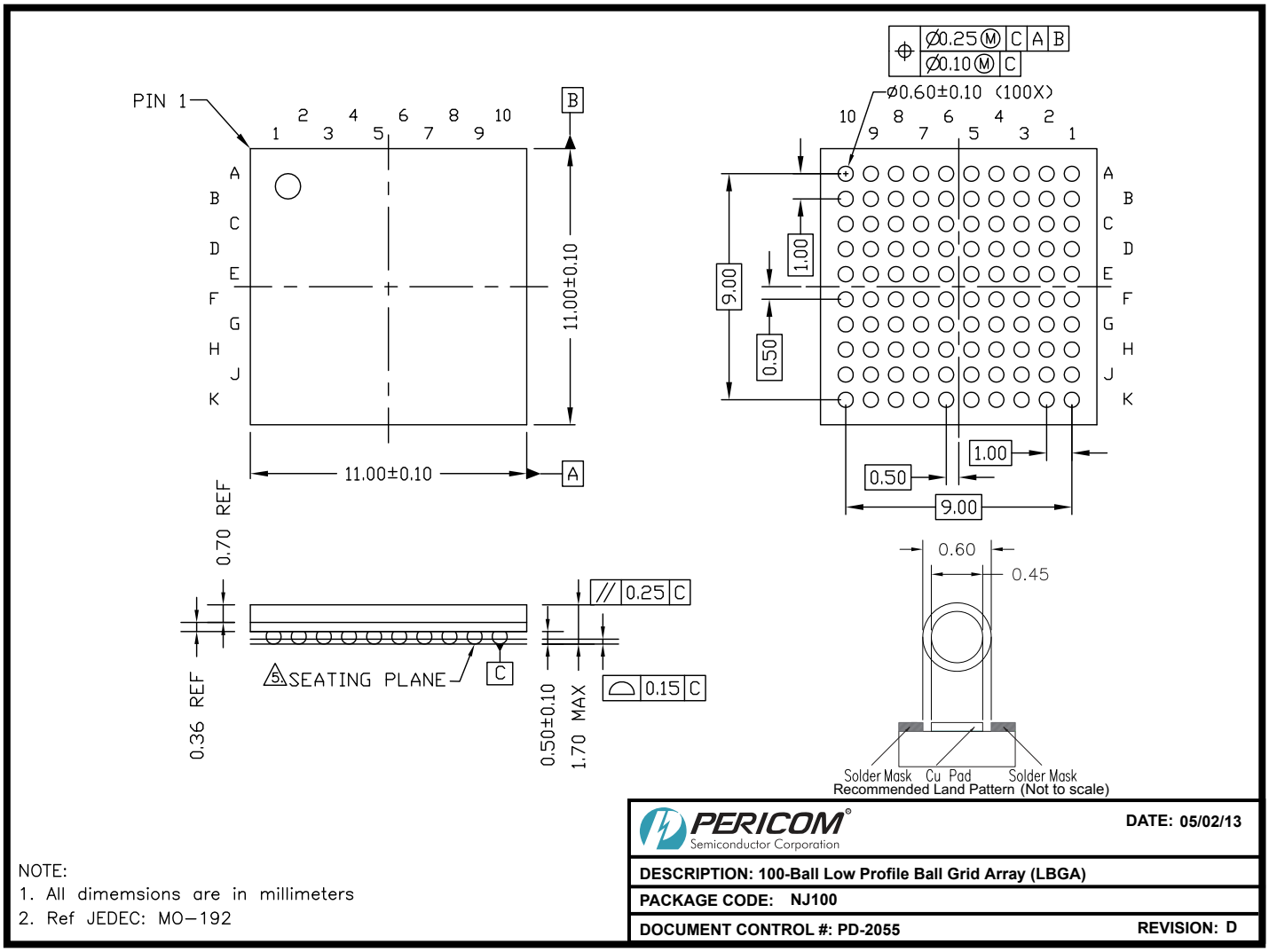
BYTE	A	d	0	1	2	3	4	5	6	7	8	9
DATA	C0	00	FF	FF	F0	00	00	FF	FF	FF	14	21

Part Marking

NJ Package

*: Porting Code
YY: Year
WW: Workweek
1st X: Assembly Code
2nd X: Fab Code

Packaging Mechanical: 100-LBGA (NJ)



13-0083

For latest package info.

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Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX6804-ANJEX	NJ	100-Ball, Low Profile Ball Grid Array (LBGA)

Notes:

1. EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant. All applicable RoHS exemptions applied.
2. See http://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free. Thermal characteristics can be found on the company web site at www.diodes.com/design/support/packaging/
3. E = Pb-free and Green
4. X suffix = Tape/Reel

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