TLV9051 / TLV9052 / TLV9054 5-MHz, 15-V/µs High Slew-Rate, RRIO Op Amp

1 Features

- High slew rate: 15 V/µs
- Low quiescent current: 330 µA
- Rail-to-rail input and output
- Low input offset voltage: ±0.33 mV
- Unity-gain bandwidth: 5 MHz
- Low broadband noise: 15 nV/√Hz
- Low input bias current: 2 pA
- Unity-gain stable
- Internal RFI and EMI filter
- Scalable family of CMOS op amps for low-cost applications
- Operational at supply voltages as low as 1.8 V
- Extended temperature range: –40°C to 125°C

2 Applications

- HVAC: heating, ventilating, and air conditioning
- Photodiode amplifier
- Current shunt monitoring for DC motor control
- White goods (refrigerators, washing machines, and so forth)
- Sensor signal conditioning
- Active filters
- Low-side current sensing

3 Description

The TLV9051, TLV9052, and TLV9054 devices are single, dual, and quad operational amplifiers, respectively. The devices are optimized for low voltage operation from 1.8 V to 5.5 V. The inputs and outputs can operate from rail to rail at a very high slew rate. These devices are perfect for cost-constrained applications where low-voltage operation, high slew rate, and low quiescent current is needed. The capacitive-load drive of the TLV905x family is 150 pF, and the resistive open-loop output impedance makes stabilization easier with much higher capacitive loads.

The TLV905xS devices include a shutdown mode that allow the amplifiers to be switched off into a standby mode with typical current consumption less than 1 µA.

The TLV905x family is easy to use due to the devices being unity-gain stable, including a RFI and EMI filter, and being free from phase reversal in an overdrive condition.

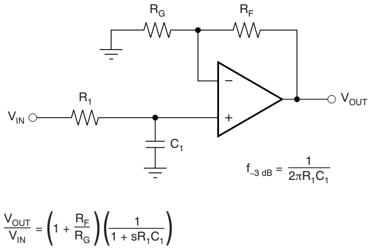
Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV9051	SOT-23 (5)	1.60 mm × 2.90 mm
	SC70 (5)	1.25 mm × 2.00 mm
	SOT553 (5)[2]	1.65 mm × 1.20 mm
	X2SON (5)	0.80 mm × 0.80 mm
TLV9051S	SOT-23 (6)	1.60 mm × 2.90 mm
TLV9052	SOIC (8)	3.91 mm × 4.90 mm
	TSSOP (8)	3.00 mm × 4.40 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	SOT-23 (8)	1.60 mm × 2.90 mm
	WSON (8)	2.00 mm × 2.00 mm
TLV9052S	VSSOP (10)	3.00 mm × 3.00 mm
	X2QFN (10)	1.50 mm × 2.00 mm
TLV9054	SOIC (14)	8.65 mm × 3.91 mm
	TSSOP (14)	4.40 mm × 5.00 mm
	X2QFN (14)	2.00 mm × 2.00 mm
	WQFN (16)	3.00 mm × 3.00 mm
TLV9054S	WQFN (16)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Package is for preview only.

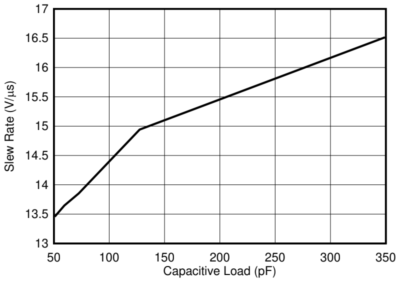
Single-Pole, Low-Pass Filter



$$f_{-3\,dB} = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

Slew Rate vs Load Capacitance



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (September 2019) to Revision H	Page
• Added new human-body model and charged-device model ratings for TLV9051 X2SON package to the *ESD Ratings*	12
• Added *Packages With an Exposed Thermal Pad* section to *Feature Description* section	25

Changes from Revision F (June 2019) to Revision G	Page
• Deleted preview tags for all TLV9051 packages	1
• Deleted preview tags for the TLV9052 SOT-23 (8) - DDF package	1
• Added link to *Shutdown Function* section in all of the $\overline{\text{SHDN}}$ pin function rows	6
• Added *EMI Rejection* section to *Feature Description* section	24
• Added clarification to the *Shutdown Function* section	26

Changes from Revision E (May 2019) to Revision F	Page
• Deleted package preview notation for TLV9052S devices in *Device Information*	1
• Deleted package preview notation for TLV9052S devices under *Device Comparison Table*	4
• Deleted preview notation for TLV9052S devices in *Device Comparison Table*	4
• Deleted package preview notation for TLV9052S in *Pin Configuration and Functions* section	8
• Deleted package preview notation for TLV9052S under *Thermal Information for Dual Channel*	13

Changes from Revision D (April 2019) to Revision E	Page
• Added DDF (SOT-23) information to *Thermal Information for Dual Channel* table	13

Changes from Revision C (April 2019) to Revision D — Page

- Deleted preview notations for TLV9054/S devices in *Device Information* ... 1
- Deleted preview notations for TLV9054 devices in *Device Comparison Table* ... 4
- Deleted preview notations for TLV9054S device in *Device Comparison Table* ... 4
- Deleted preview notations for TLV9054 packages in *Pin Configurations and Functions* section ... 9
- Deleted preview notation for TLV9054S RTE package in *Pin Configurations and Functions* section ... 11
- Deleted preview notation for TLV9054/S packages in *Thermal Information for Quad Channel* ... 13

Changes from Revision B (March 2019) to Revision C — Page

- Added TLV9051 thermal information for DPW, DBV, and DCK packages ... 12

Changes from Revision A (December 2018) to Revision B — Page

- Added Shutdown device notes in the *Description* section ... 1
- Added SOT-23 (8) package to *Device Information* ... 1
- Added Shutdown devices to *Device Information* ... 1
- Added X2QFN (RUC) package to TLV9054 *Device Information* ... 1
- Added DDF package information to *Device Comparison Table* ... 4
- Added Shutdown devices (TLV9051S/TLV9052S/TLV9054S) and packages (DGS/RUG/RTE) to *Device Comparison Table* ... 4
- Added TLV9051S pinout information to *Pin Configurations and Functions* section ... 6
- Added DDF (SOT-23) package ... 7
- Added TLV9052S pinout information to *Pin Configurations and Functions* section ... 8
- Added TLV9054S and TLV9054 X2QFN (RUC) pinout information to *Pin Configurations and Functions* section ... 9
- Added TLV9051 and TLV9051S thermal information to *Thermal Information for Single Channel* ... 12
- Added TLV9052S thermal info to *Thermal Information for Dual Channel* ... 13
- Added DDF (SOT-23) package to *Thermal Information for Dual Channel* ... 13
- Added TLV9054 and TLV9054S thermal information to *Thermal Information for Quad Channel* ... 13
- Added Shutdown Function information in *Feature Description* section ... 26
- Added "S" suffix to *Related Links* to reflect the addition of Shutdown devices ... 33

Changes from Original (August 2018) to Revision A — Page

- Changed the device status from *Advance Information* to *Production Data* ... 1

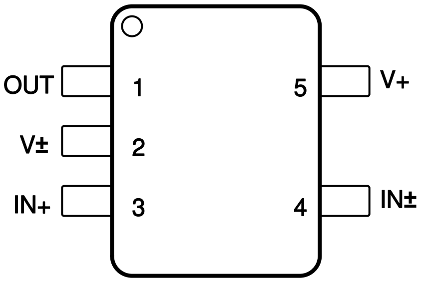
5 Device Comparison Table

DEVICE	NO. OF CH.	PACKAGE LEADS												
		SC70 DCK	SOT-23 DBV	SOT-553(1) DRL	X2SON DPW	SOIC D	WSON DSG	VSSOP DGK	TSSOP PW	SOT-23 DDF	VSSOP DGS	X2QFN RUG	X2QFN RUC	WQFN RTE
TLV9051	1	5	5	5	5	—	—	—	—	—	—	—	—	—
TLV9051S		—	6	—	—	—	—	—	—	—	—	—	—	—
TLV9052	2	—	—	—	—	8	8	8	8	8	—	—	—	—
TLV9052S		—	—	—	—	—	—	—	—	—	10	10	—	—
TLV9054	4	—	—	—	—	14	—	—	14	—	—	—	14	16
TLV9054S		—	—	—	—	—	—	—	—	—	—	—	—	16

(1) Package is for preview only.

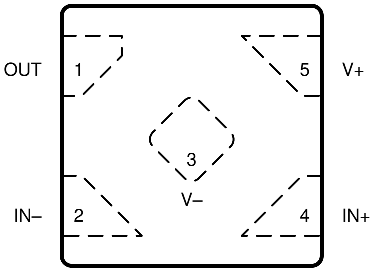
6 Pin Configuration and Functions

TLV9051 DBV, DRL Packages
5-Pin SOT-23, SOT-553
Top View



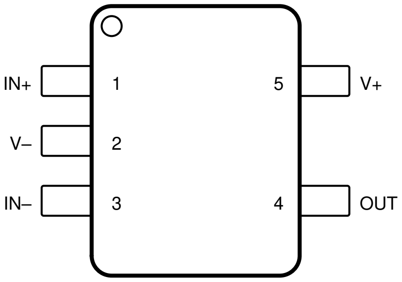
Not to scale

TLV9051 DPW Package
5-Pin X2SON
Top View



Not to scale

TLV9051 DCK Package
5-Pin SC70
Top View

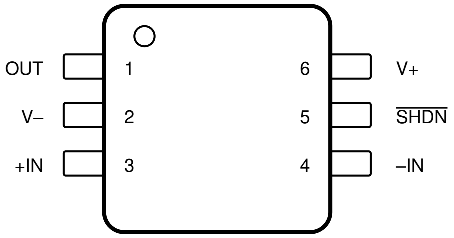


Not to scale

Pin Functions: TLV9051

PIN				I/O	DESCRIPTION
NAME	SOT-23, SOT-553	SC-70	X2SON		
IN–	4	3	2	I	Inverting input
IN+	3	1	4	I	Noninverting input
OUT	1	4	1	O	Output
V–	2	2	3	—	Negative (low) supply or ground (for single-supply operation)
V+	5	5	5	—	Positive (high) supply

TLV9051S DBV Package
6-Pin SOT-23
Top View

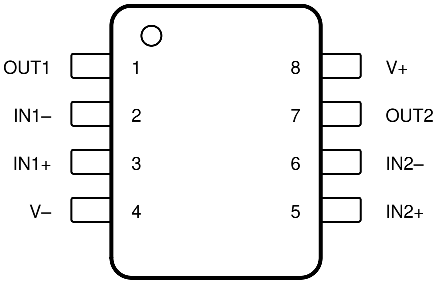


Not to scale

Pin Functions: TLV9051S

PIN		I/O	DESCRIPTION
NAME	NO.		
–IN	4	I	Inverting input
+IN	3	I	Noninverting input
OUT	1	O	Output
$\overline{\text{SHDN}}$	5	I	Shutdown: low = amp disabled, high = amp enabled. See *Shutdown Function* section for more information.
V–	2	—	Negative (lowest) supply or ground (for single-supply operation).
V+	6	—	Positive (highest) supply

TLV9052 D, DGK, PW, DDF Packages
8-Pin SOIC, VSSOP, TSSOP, SOT-23
Top View



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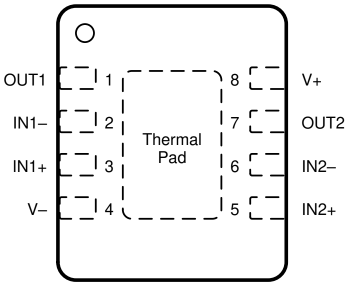
TLV9052 DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



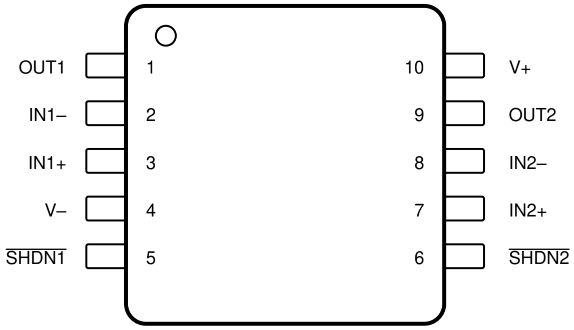
Not to scale

Connect exposed thermal pad to V–. See *Packages With an Exposed Thermal Pad* section for more information.

Pin Functions: TLV9052

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	—	Negative (low) supply or ground (for single-supply operation)
V+	8	—	Positive (high) supply

TLV9052S DGS Package
10-Pin VSSOP
Top View



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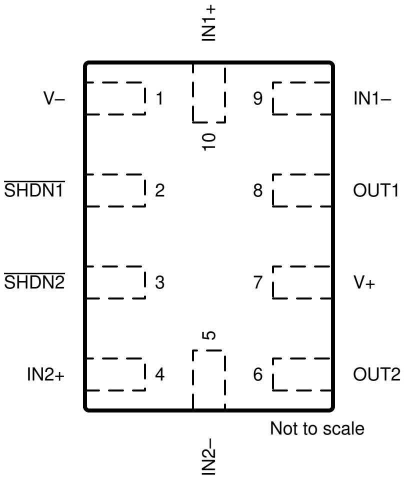
TLV9052S RUG Package
10-Pin X2QFN
Top View

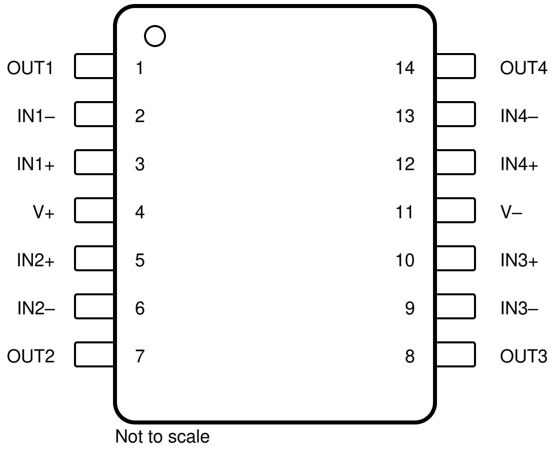


Not to scale

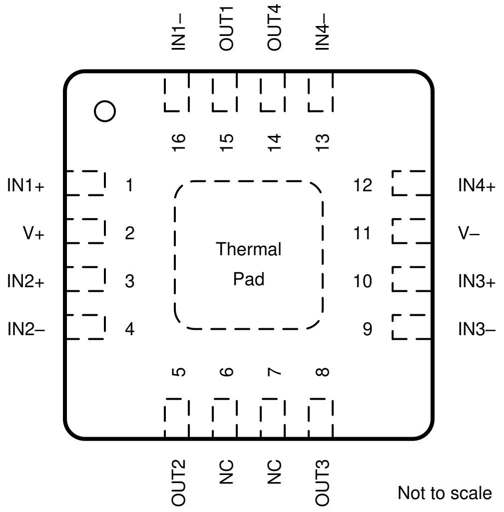
Pin Functions: TLV9052S

PIN			I/O	DESCRIPTION
NAME	VSSOP	X2QFN		
IN1–	2	9	I	Inverting input, channel 1
IN1+	3	10	I	Noninverting input, channel 1
IN2–	8	5	I	Inverting input, channel 2
IN2+	7	4	I	Noninverting input, channel 2
OUT1	1	8	O	Output, channel 1
OUT2	9	6	O	Output, channel 2
$\overline{\text{SHDN1}}$	5	2	I	Shutdown: low = amp disabled, high = amp enabled, channel 1. See *Shutdown Function* section for more information.
$\overline{\text{SHDN2}}$	6	3	I	Shutdown: low = amp disabled, high = amp enabled, channel 2. See *Shutdown Function* section for more information.
V–	4	1	—	Negative (low) supply or ground (for single-supply operation)
V+	10	7	—	Positive (high) supply

TLV9054 D, PW Packages
14-Pin SOIC, TSSOP
Top View

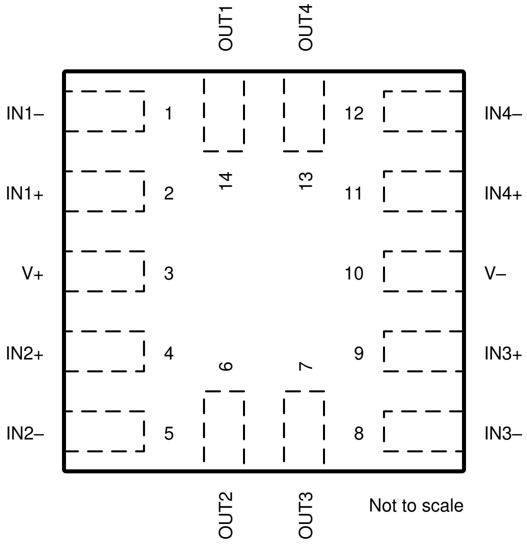


TLV9054 RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View



Connect exposed thermal pad to V–. See *Packages With an Exposed Thermal Pad* section for more information.

TLV9054 RUC Package
14-Pin X2QFN
Top View



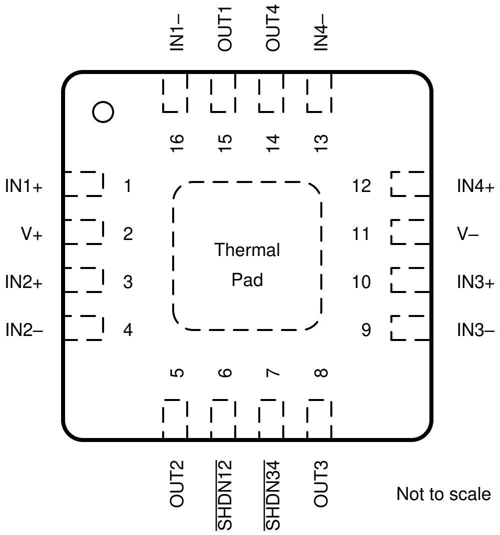
Pin Functions: TLV9054

PIN				I/O	DESCRIPTION
NAME	SOIC, TSSOP	WQFN	X2QFN		
IN1–	2	16	1	I	Inverting input, channel 1
IN1+	3	1	2	I	Noninverting input, channel 1
IN2–	6	4	5	I	Inverting input, channel 2
IN2+	5	3	4	I	Noninverting input, channel 2
IN3–	9	9	8	I	Inverting input, channel 3
IN3+	10	10	9	I	Noninverting input, channel 3
IN4–	13	13	12	I	Inverting input, channel 4
IN4+	12	12	11	I	Noninverting input, channel 4

Pin Functions: TLV9054 (continued)

PIN				I/O	DESCRIPTION
NAME	SOIC, TSSOP	WQFN	X2QFN		
NC	—	6, 7	—	—	No internal connection
OUT1	1	15	14	O	Output, channel 1
OUT2	7	5	6	O	Output, channel 2
OUT3	8	8	7	O	Output, channel 3
OUT4	14	14	13	O	Output, channel 4
V–	11	11	10	—	Negative (low) supply or ground (for single-supply operation)
V+	4	2	3	—	Positive (high) supply

TLV9054S RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View



Connect exposed thermal pad to V–. See *Packages With an Exposed Thermal Pad* section for more information.

Pin Functions: TLV9054S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	1	I	Noninverting input, channel 1
IN1–	16	I	Inverting input, channel 1
IN2+	3	I	Noninverting input, channel 2
IN2–	4	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3–	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4–	13	I	Inverting input, channel 4
$\overline{\text{SHDN12}}$	6	I	Shutdown: low = amp disabled, high = amp enabled, channel 1 and 2. See *Shutdown Function* section for more information.
$\overline{\text{SHDN34}}$	7	I	Shutdown: low = amp disabled, high = amp enabled, channel 3 and 4. See *Shutdown Function* section for more information.
OUT1	15	O	Output, channel 1
OUT2	5	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V–	11	—	Negative (low) supply or ground (for single-supply operation)
V+	2	—	Positive (high) supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)				6	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		V_S + 0.2	V
	Current(2)		–10	10	mA
Output short-circuit(3)			Continuous		
Operating ambient temperature, T_A			–40	150	°C
Junction temperature, T_J				150	°C
Storage temperature, T_{stg}			–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
TLV9051 X2SON PACKAGE				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
ALL OTHER PACKAGES				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, V_S = (V+) – (V–)	1.8	5.5	V
V_{IN}	Input pin voltage	(V–) – 0.1	(V+) + 0.1	V
	Specified temperature	–40	125	°C

7.4 Thermal Information for Single Channel

THERMAL METRIC(1)		TLV9051, TLV9051S					UNIT
		DPW (X2SON)	DBV (SOT-23)		DCK (SC70)	DRL (SOT553)(2)	
		5 PINS	5 PINS	6 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	470.0	228.1	210.8	231.2	TBD	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	211.9	152.1	152.1	144.4	TBD	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	334.8	97.7	92.3	78.6	TBD	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.8	74.1	76.2	51.3	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) This package option is for preview only.

Thermal Information for Single Channel (continued)

THERMAL METRIC(1)		TLV9051, TLV9051S					UNIT
		DPW (X2SON)	DBV (SOT-23)		DCK (SC70)	DRL (SOT553)(2)	
		5 PINS	5 PINS	6 PINS	5 PINS	5 PINS	
ψ_{JB}	Junction-to-board characterization parameter	333.2	97.3	92.1	78.3	TBD	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	N/A	TBD	°C/W

7.5 Thermal Information for Dual Channel

THERMAL METRIC(1)		TLV9052, TLV9052S							UNIT
		D (SOIC)	DGK (VSSOP)	DSG (WSON)	PW (TSSOP)	DDF (SOT-23)	DGS (VSSOP)	RUG (X2QFN)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	155.4	208.8	102.3	205.1	184.4	170.4	197.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	95.5	93.3	120.0	93.7	112.8	84.9	93.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.9	130.7	68.2	135.7	99.9	113.5	123.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	41.9	26.1	15.1	25.0	18.7	16.4	3.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	98.1	128.9	68.2	134.0	99.3	112.3	120.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	43.6	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.6 Thermal Information for Quad Channel

THERMAL METRIC(1)		TLV9054, TLV9054S					UNIT
		D (SOIC)	PW (TSSOP)	RTE (WQFN)		RUC (X2SQFN)	
		14 PINS	14 PINS	14 PINS	16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.0	147.2	65.5	65.6	209.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	71.1	67.2	70.6	70.6	68.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.0	91.6	40.5	40.5	153.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.7	16.6	5.8	5.8	3.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.6	90.7	40.5	40.5	152.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	24.5	24.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.7 Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V–) = 1.8 V to 5.5 V

For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage	V_S = 5 V			±0.33	±1.6	mV
		V_S = 5 V	T_A = –40°C to 125°C			±2	
dV_{OS}/dT	Drift	V_S = 5 V	T_A = –40°C to 125°C		±0.5		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V – 5.5 V, V_{CM} = (V–)			±13	±80	µV/V
	Channel separation, DC	At DC			100		dB
INPUT BIAS CURRENT							
I_B	Input bias current				±2		pA
I_{OS}	Input offset current				±1		pA
NOISE							
E_n	Input voltage noise (peak-to-peak)	V_S = 5 V, f = 0.1 Hz to 10 Hz			6		μV_{PP}
e_n	Input voltage noise density	V_S = 5 V, f = 10 kHz			15		nV/√Hz
		V_S = 5 V, f = 1 kHz			20		
i_n	Input current noise density	f = 1 kHz			18		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range	V_S = 1.8 V to 5.5 V		(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V	T_A = –40°C to 125°C	80	96		dB
		V_S = 5.5 V, V_{CM} = –0.1 V to 5.6 V	T_A = –40°C to 125°C	62	79		
		V_S = 1.8 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V	T_A = –40°C to 125°C		88		
		V_S = 1.8 V, V_{CM} = –0.1 V to 1.9 V	T_A = –40°C to 125°C		72		
INPUT CAPACITANCE							
C_{ID}	Differential				2		pF
C_{IC}	Common-mode				4		pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10 kΩ			106		dB
		V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ		104	128		
		V_S = 1.8 V, (V–) + 0.06 V < V_O < (V+) – 0.06 V, R_L = 2 kΩ			108		
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ			130		
FREQUENCY RESPONSE							
GBW	Gain bandwidth product	V_S = 5.5 V, G = +1			5		MHz
φ_m	Phase margin	V_S = 5.5 V, G = +1			60		°
SR	Slew rate	V_S = 5.5 V, G = +1, C_L= 130 pF			15		V/µs
t_S	Settling time	To 0.1%, V_S = 5.5 V, 2-V step , G = +1, C_L = 100 pF			0.75		µs
		To 0.01%, V_S = 5.5 V, 2-V step, G = +1, C_L = 100 pF			1		
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S			0.3		µs
THD + N	Total harmonic distortion + noise(1)	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz			0.0006%		

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V–) = 1.8 V to 5.5 V (continued)

For V_S = (V+) – (V–) = 1.8 V to 5.5 V (±0.9 V to ±2.75 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT							
V_O	Voltage output swing from rail	Positive rail headroom, V_S = 5.5 V	R_L = 2 kΩ			40	mV
			R_L = 10 kΩ			16	
		Negative rail headroom, V_S = 5.5 V	R_L = 2 kΩ			40	
			R_L = 10 kΩ			16	
I_{SC}	Short-circuit current	V_S = 5 V			±50		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 5 MHz			250		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 mA			330	450	µA
		V_S = 5.5 V, I_O = 0 mA	T_A = –40°C to 125°C			475	
SHUTDOWN							
I_{QSD}	Quiescent current per amplifier	V_S = 1.8 V to 5.5 V, all amplifiers disabled, $\overline{SHDN}$ = $V_{S–}$			0.35	1	µA
Z_{SHDN}	Output impedance during shutdown	V_S = 1.8 V to 5.5 V, amplifier disabled			10 || 8		GΩ || pF
V_{IH}	High voltage (amplifier enabled)	V_S = 1.8 V to 5.5 V, amplifier enabled			(V–) + 0.9	(V–) + 1.1	V
V_{IL}	Low voltage (amplifier disabled)	V_S = 1.8 V to 5.5 V, amplifier disabled		(V–) + 0.2	(V–) + 0.7		V
t_{ON}	Amplifier enable time (full shutdown)(2)(3)	V_S = 1.8 V to 5.5 V, full shutdown; G = 1, V_{OUT} = 0.9 × V_S / 2			35		µs
	Amplifier enable time (partial shutdown)(2)(3)	V_S = 1.8 V to 5.5 V, partial shutdown; G = 1, V_{OUT} = 0.9 × V_S / 2			10		
t_{OFF}	Amplifier disable time(2)	V_S = 1.8 V to 5.5 V, G = 1, V_{OUT} = 0.1 × V_S / 2			6		µs
	$\overline{SHDN}$ pin input bias current (per pin)	V_S = 1.8 V to 5.5 V, V+ ≥ $\overline{SHDN}$ ≥ (V+) – 0.8 V			40		nA
		V_S = 1.8 V to 5.5 V, V– ≤ $\overline{SHDN}$ ≤ (V–) + 0.8 V			160		

(2) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

(3) Full shutdown refers to the dual TLV9052S having both channels 1 and 2 disabled ($\overline{SHDN\_1}$ = $\overline{SHDN\_2}$ = $V_–$) and the quad TLV9054S having all channels 1 to 4disabled ($\overline{SHDN\_12}$ = $\overline{SHDN\_34}$ = $V_–$). For partial shutdown, only one $\overline{SHDN}$ pin is exercised; in this mode, the internal biasing circuitry remains operational and the enable time is shorter.

7.8 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

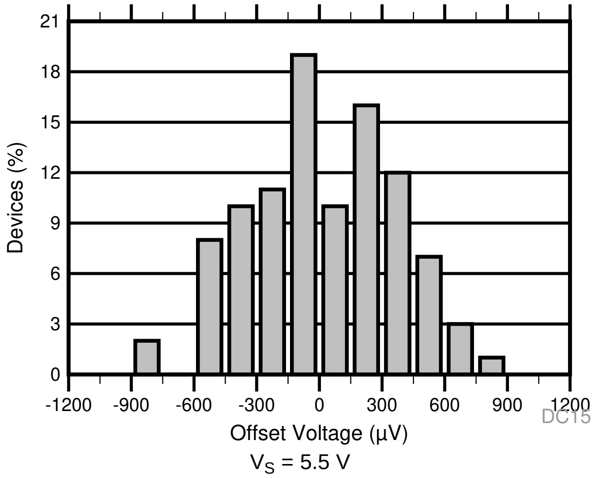


Figure 1. Offset Voltage Production Distribution

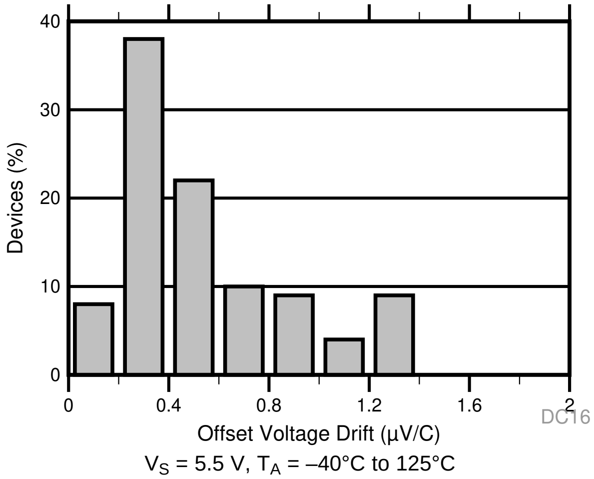


Figure 2. Offset Voltage Drift Distribution

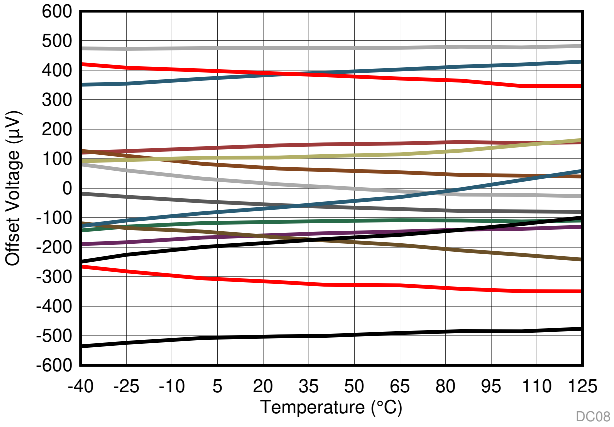


Figure 3. Offset Voltage vs Temperature

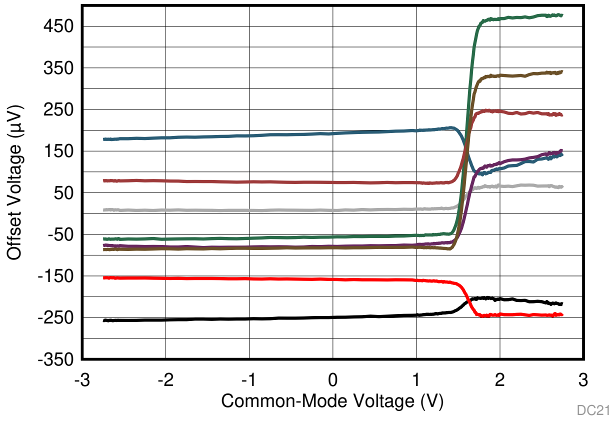


Figure 4. Offset Voltage vs Common-Mode Voltage

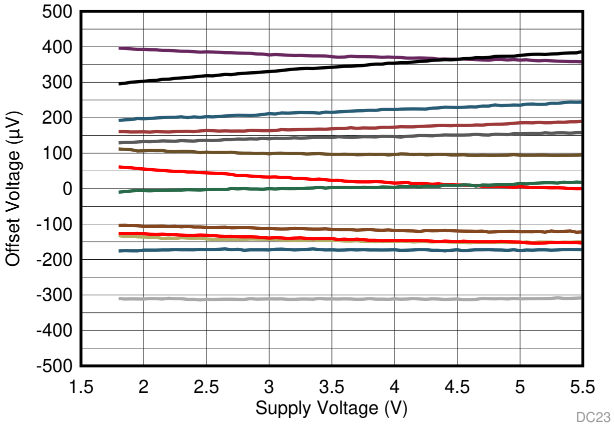


Figure 5. Offset Voltage vs Power Supply

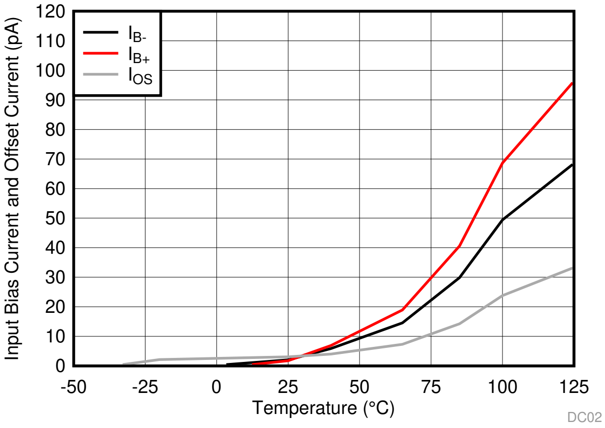


Figure 6. Input Bias Current vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

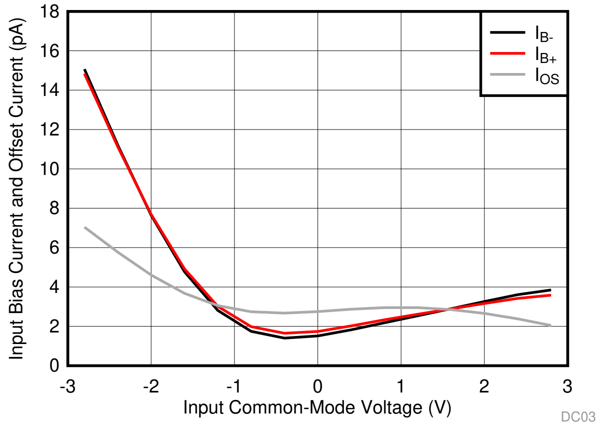


Figure 7. Input Bias Current and Offset Current vs Common-Mode Voltage

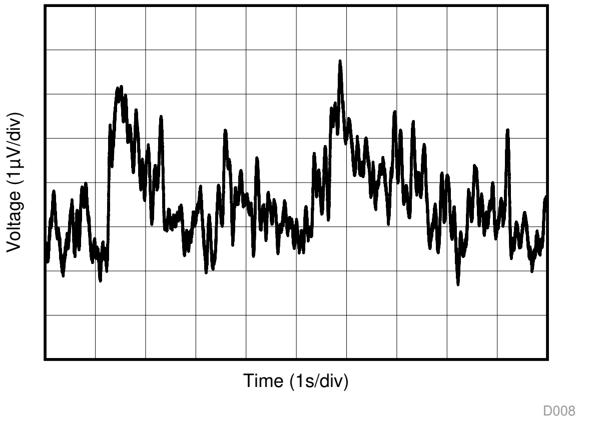


Figure 8. 0.1-Hz to 10-Hz Input Voltage Noise

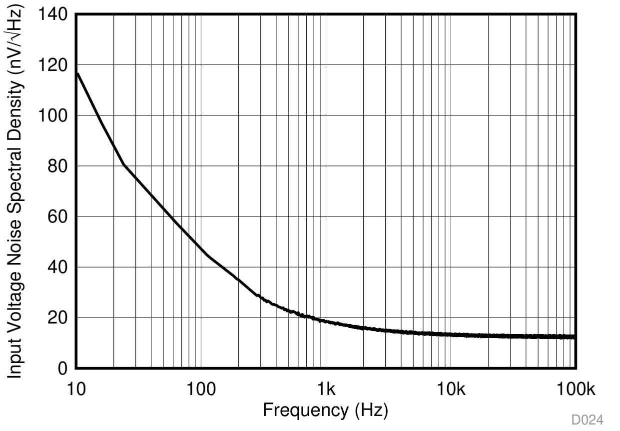


Figure 9. Input Voltage Noise Spectral Density vs Frequency

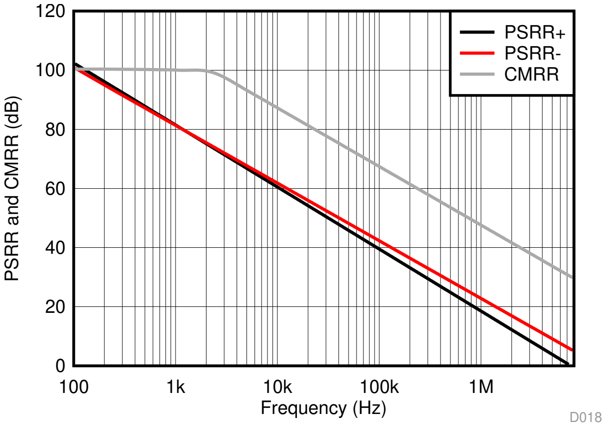


Figure 10. CMRR and PSRR vs Frequency (Referred to Input)

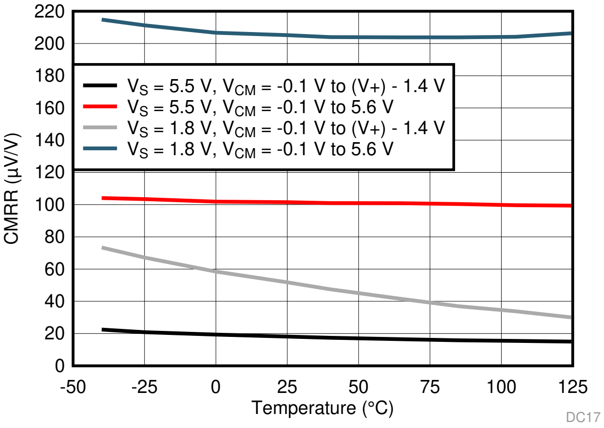
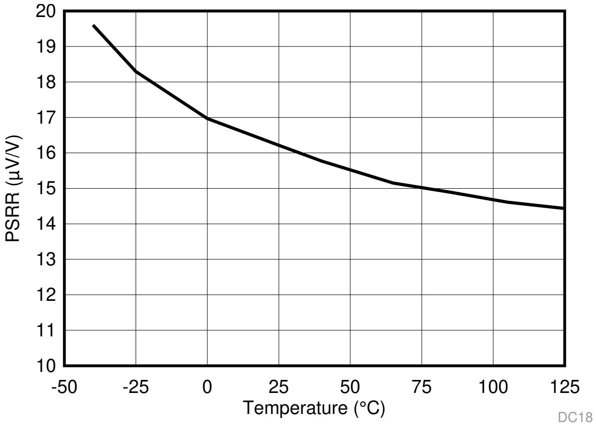


Figure 11. CMRR vs Temperature



V_S = 1.8 V to 5.5 V

Figure 12. PSRR vs Temperature

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

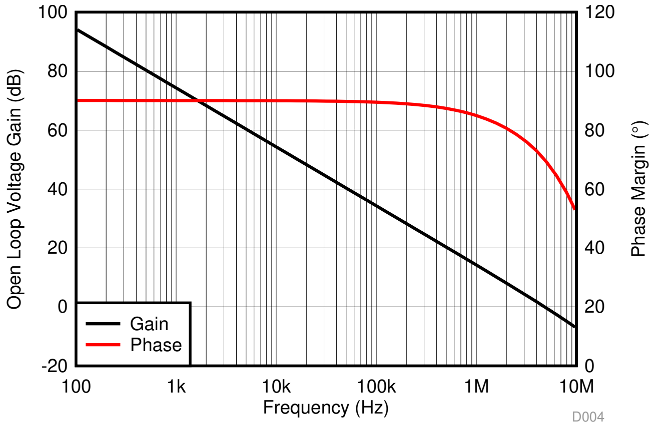


Figure 13. Open Loop Voltage Gain and Phase vs Frequency

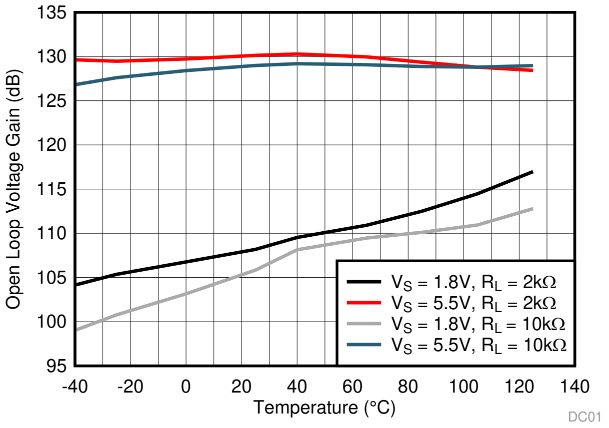


Figure 14. Open Loop Voltage Gain vs Temperature

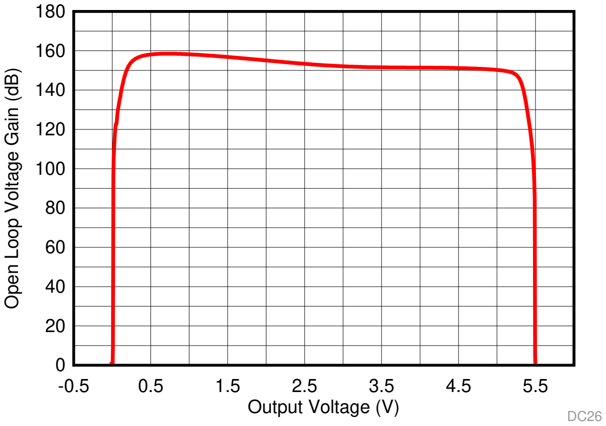


Figure 15. Open Loop Voltage Gain vs Output Voltage

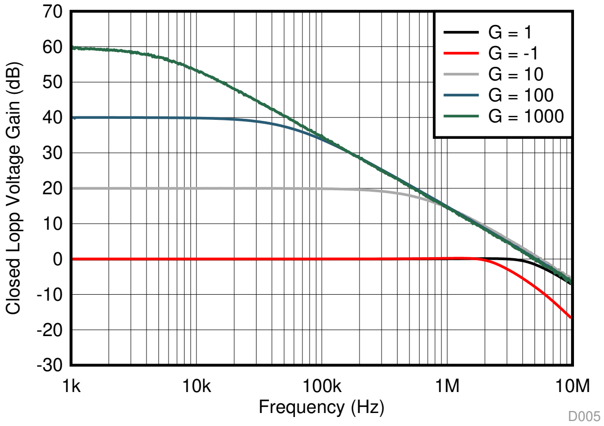


Figure 16. Closed Loop Voltage Gain vs Frequency

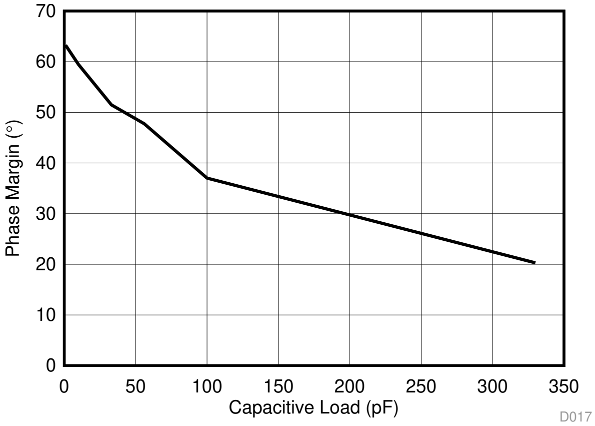


Figure 17. Phase Margin vs Capacitive Load

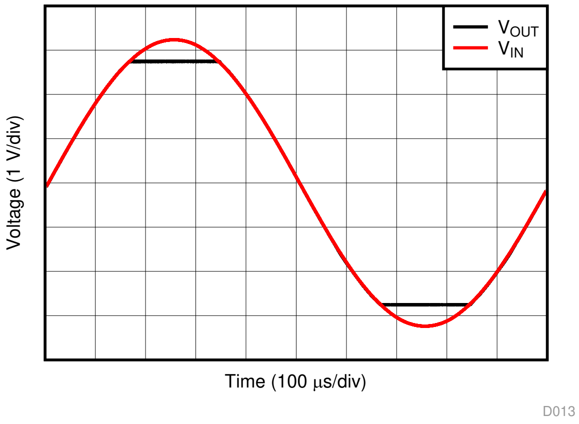
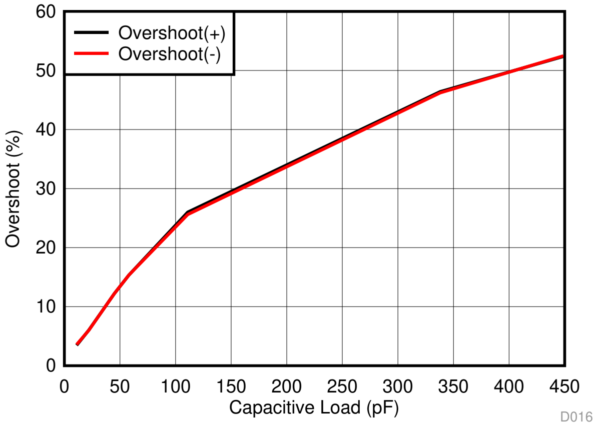


Figure 18. No Phase Reversal

Typical Characteristics (continued)

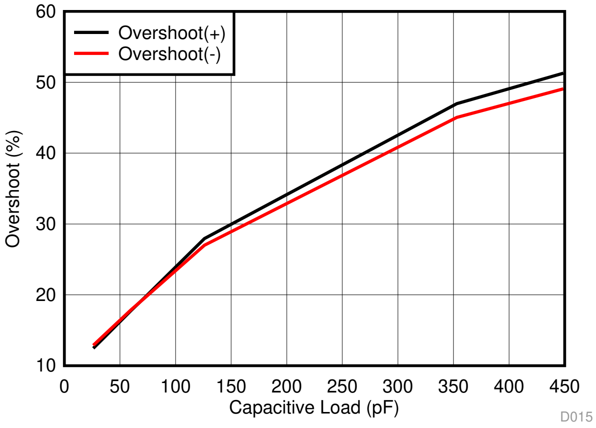
at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



G = +1 V/V

V_{OUT} step = 100 mV_{p-p}

Figure 19. Small-Signal Overshoot vs Load Capacitance



G = –1 V/V

V_{OUT} step = 100 mV_{p-p}

Figure 20. Small-Signal Overshoot vs Load Capacitance

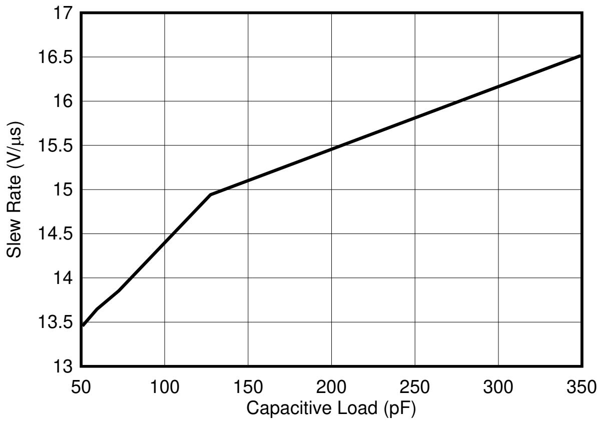
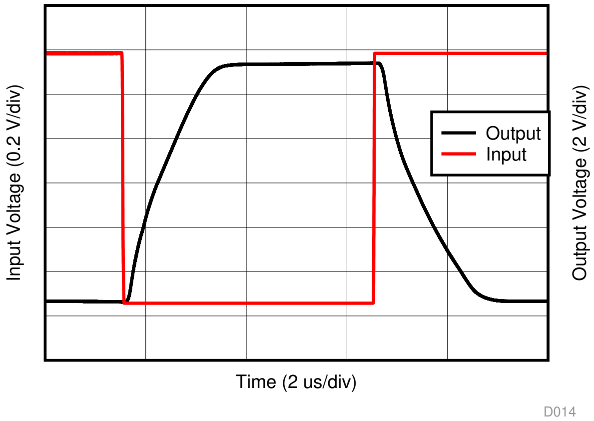


Figure 21. Slew Rate vs Capacitive Load



G = –10 V/V

Figure 22. Overload Recovery

G = +1 V/V

V_{OUT} step = 10 mV_{p-p}

Figure 23. Small-Signal Step Response

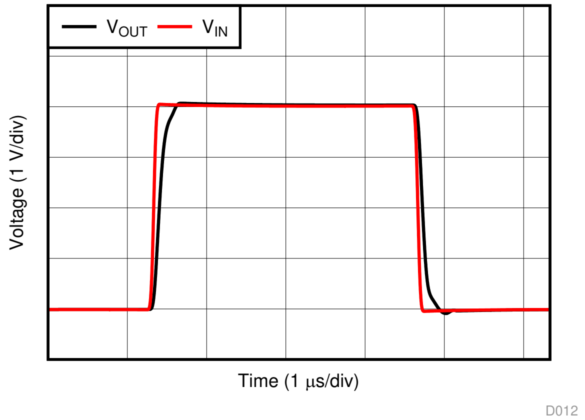
G = –1 V/V

V_{OUT} step = 10 mV_{p-p}

Figure 24. Small-Signal Step Response

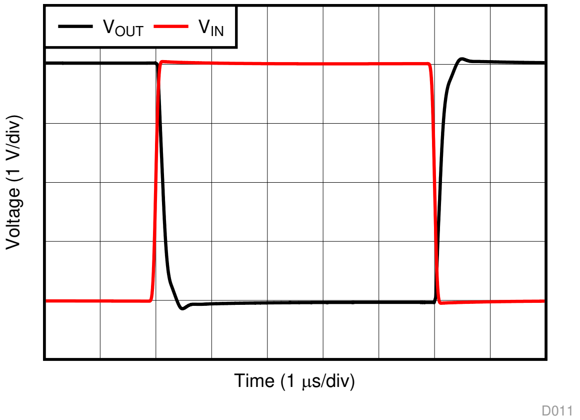
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



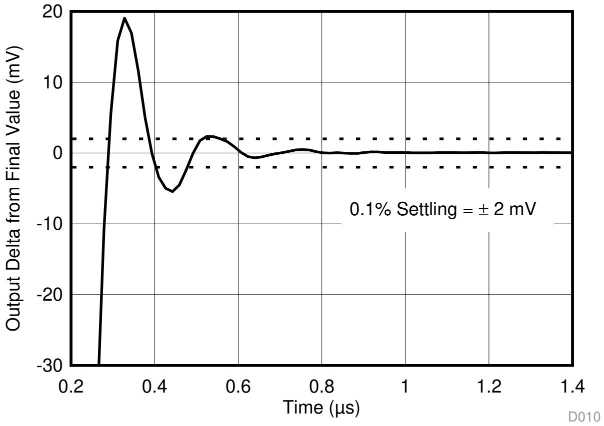
G = +1 V/V
V_{OUT} step = 4 $V_{p\text{-}p}$

Figure 25. Large-Signal Step Response



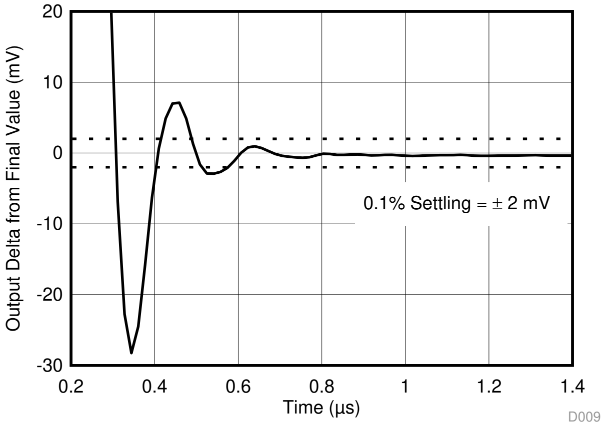
G = –1 V/V
V_{OUT} step = 4 $V_{p\text{-}p}$

Figure 26. Large-Signal Step Response



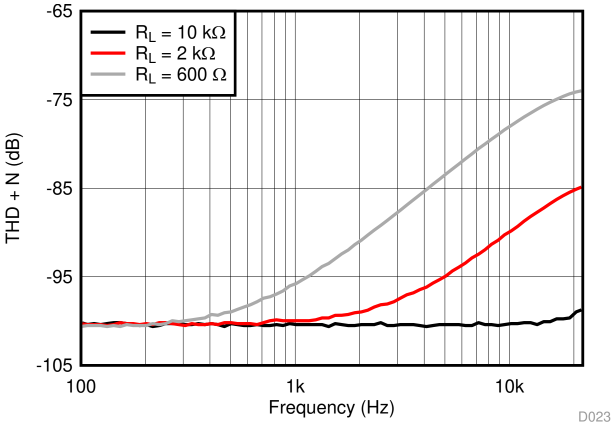
C_L = 100 pF G = +1 V/V

Figure 27. Positive Large-Signal Settling Time



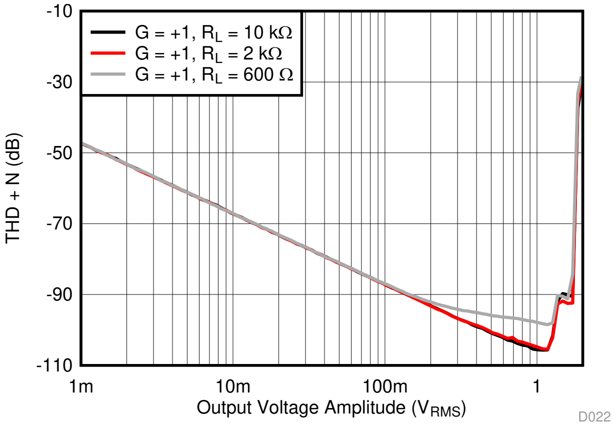
C_L = 100 pF G = +1 V/V

Figure 28. Negative Large-Signal Settling Time



V_{OUT} = 0.5 V_{RMS} G = +1 V_{CM} = 2.5 V
BW = 80 kHz

Figure 29. THD + N vs Frequency



f = 1 kHz G = +1 V_{CM} = 2.5 V
BW = 80 kHz

Figure 30. THD + N vs Amplitude

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

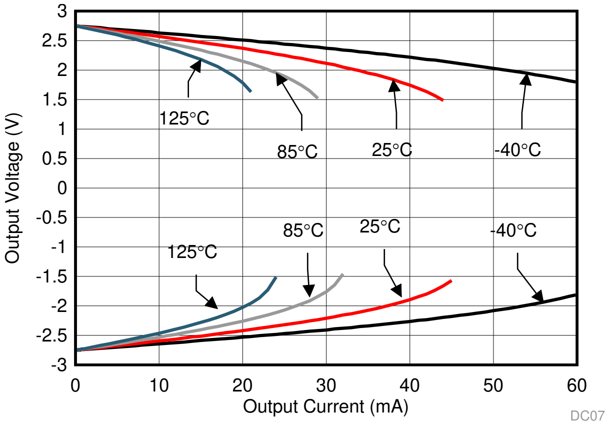


Figure 31. Output Voltage Swing vs Output Current

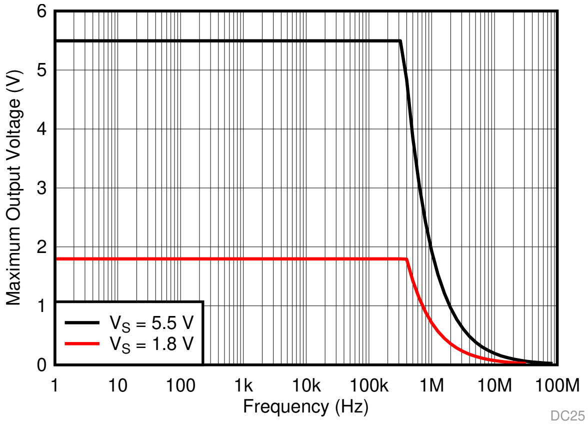


Figure 32. Maximum Output Voltage vs Frequency and Supply Voltage

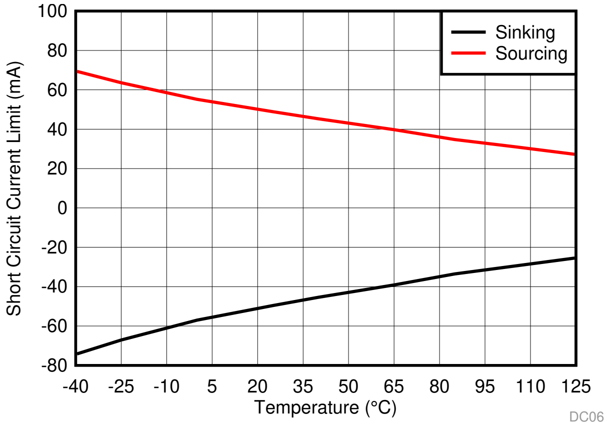


Figure 33. Short-Circuit Current vs Temperature

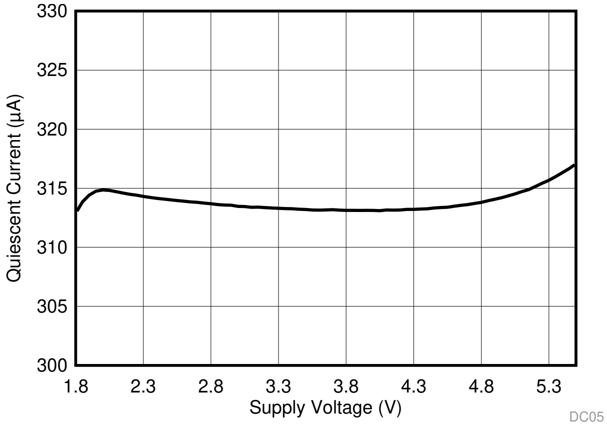


Figure 34. Quiescent Current vs Supply Voltage

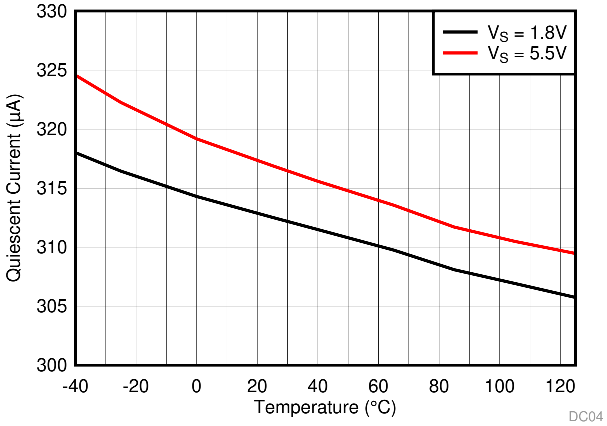


Figure 35. Quiescent Current vs Temperature

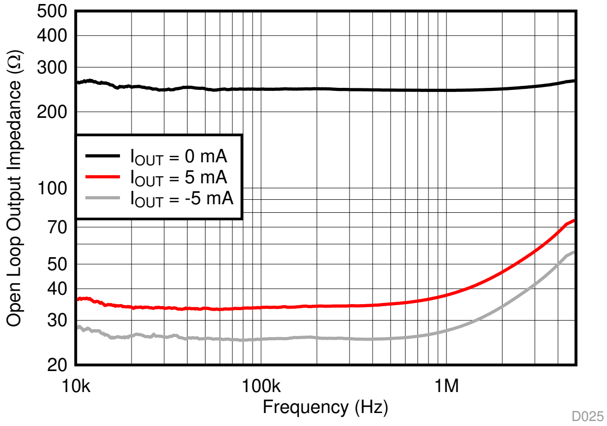
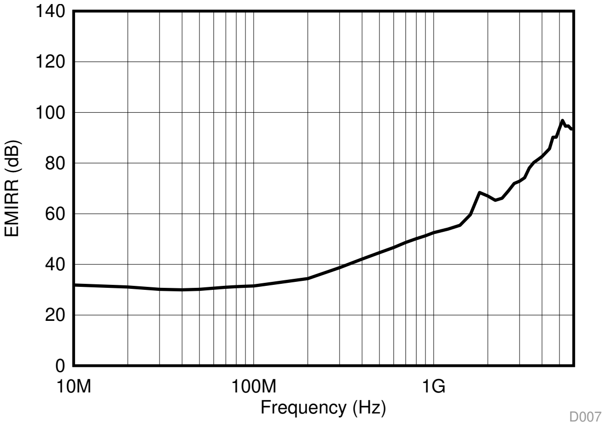


Figure 36. Open-Loop Output Impedance vs Frequency

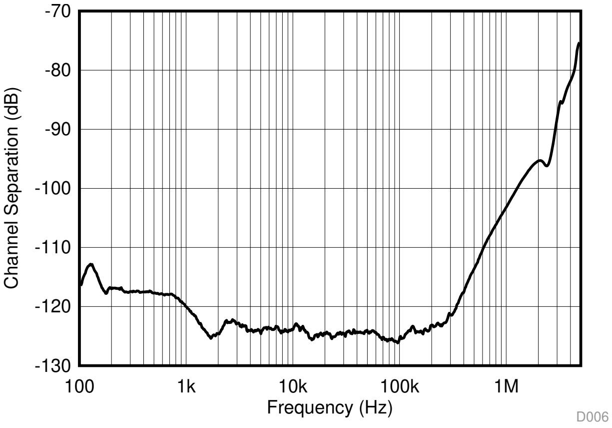
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



P_{RF} = –10 dBm

Figure 37. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency



P_{RF} = –10 dBm

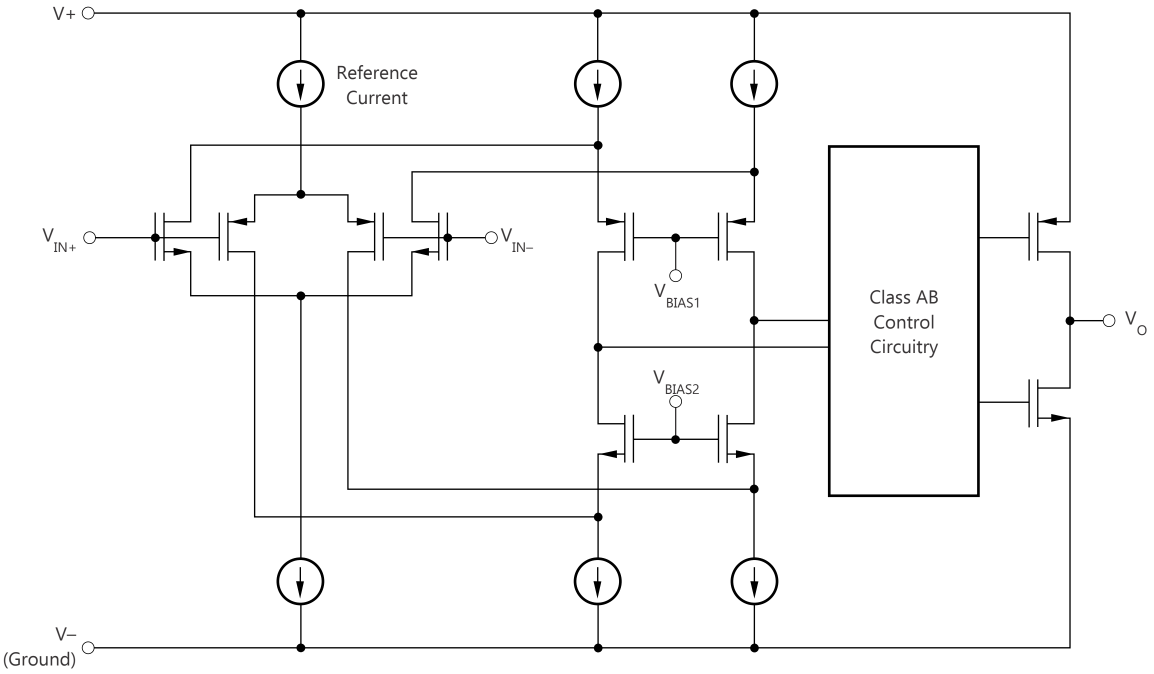
Figure 38. Channel Separation vs Frequency

8 Detailed Description

8.1 Overview

The TLV905x devices are a 5-MHz family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV905x family to be used in virtually any single-supply application. The unique combination of a high slew rate and low quiescent current makes this family a potential choice for battery-powered motor-drive applications. Rail-to-rail input and output swing significantly increase dynamic range, especially in low-supply applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The TLV905x family of op amps is specified for operation from 1.8 V to 5.5 V. In addition, many specifications apply from –40°C to 125°C. Parameters that vary significantly with operating voltages or temperature are illustrated in the *Typical Characteristics* section.

8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV905x family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

8.3.3 Rail-to-Rail Output

Designed as low-power, low-voltage operational amplifiers, the TLV905x family delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within 16 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.4 EMI Rejection

The TLV905x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV905x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 39 shows the results of this testing on the TLV905x. Table 1 shows the EMIRR IN+ values for the TLV905x at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

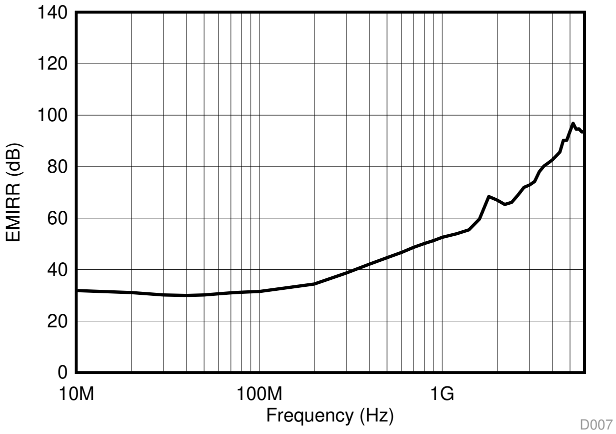


Figure 39. EMIRR Testing

Table 1. TLV905x EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	68.9 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	77.8 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	78.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	87.6 dB

8.3.5 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. After the device enters the saturation region, the output devices require time to return to the linear operating state. After the output devices return to their linear operating state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV905x family is approximately 300 ns.

8.3.6 Packages With an Exposed Thermal Pad

The TLV905x family is available in packages such as the WSON-8 (DSG) and WQFN-16 (RTE) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V– or left floating. Attaching the thermal pad to a potential other then V– is not allowed, and the performance of the device is not assured when doing so.

8.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 40 shows the ESD circuits contained in the TLV905x devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

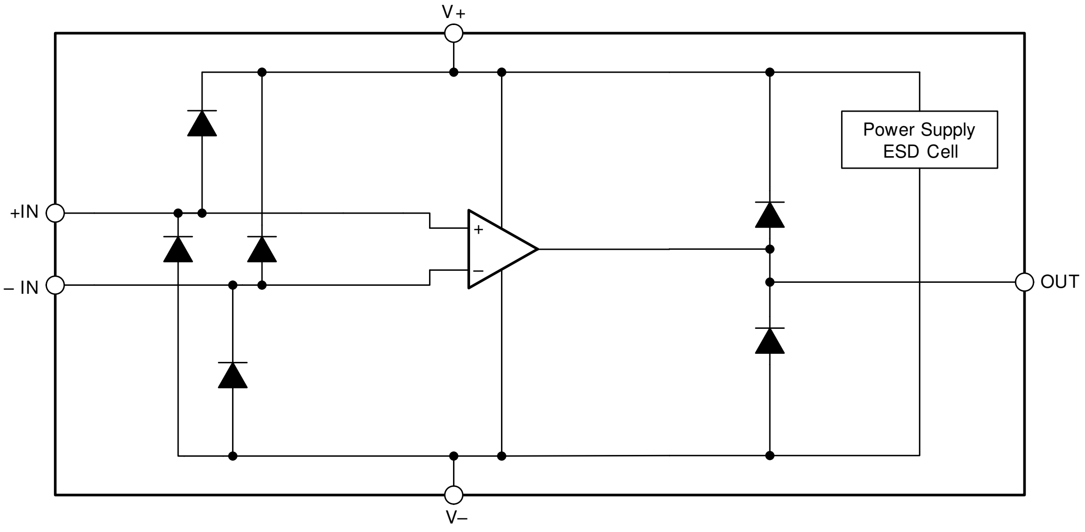


Figure 40. Equivalent Internal ESD Circuitry

8.3.8 Input Protection

The TLV905x family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as shown in the *Absolute Maximum Ratings*. Figure 41 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

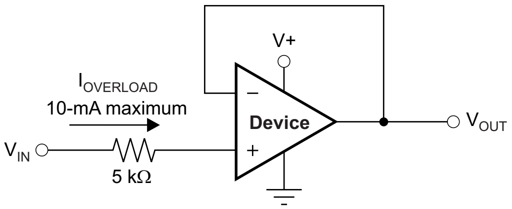


Figure 41. Input Current Protection

8.3.9 Shutdown Function

The TLV905xS devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes less than 1 µA. The $\overline{\text{SHDN}}$ pins are active low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.4 V. A valid logic high is defined as a voltage between V– + 1.2 V and V+. The shutdown pin circuitry includes a pull-up resistor, which will inherently pull the voltage of the pin to the positive supply rail if not driven. Thus, to enable the amplifier, the $\overline{\text{SHDN}}$ pins should either be left floating or driven to a valid logic high. To disable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic low .While we highly recommend that the shutdown pin be connected to a valid high or a low voltage or driven, we have included a pull-up resistor connected to VCC. The maximum voltage allowed at the $\overline{\text{SHDN}}$ pins is (V+) + 0.5 V. Exceeding this voltage level will damage the device.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 35 µs for full shutdown of all channels; disable time is 6 µs. When disabled, the output assumes a high-impedance state. This architecture allows the TLV905xS to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to midsupply (V_S / 2) is required. If using the TLV905xS without a load, the resulting turnoff time is significantly increased.

8.4 Device Functional Modes

The TLV905x family is operational when the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

The TLV905xS devices feature a shutdown mode and are shutdown when a valid logic low is applied to the shutdown pin.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TLV905x family features 5-MHz bandwidth and very high slew rate of 15 V/µs with only 330 µA of supply current per channel, providing excellent AC performance at very low-power consumption. DC applications are well served with a very low input noise voltage of 15 nV/$\sqrt{Hz}$ at 10 kHz, low input bias current, and a typical input offset voltage of 0.33 mV.

9.2 Typical Low-Side Current Sense Application

Figure 42 shows the TLV905x configured in a low-side current sensing application.

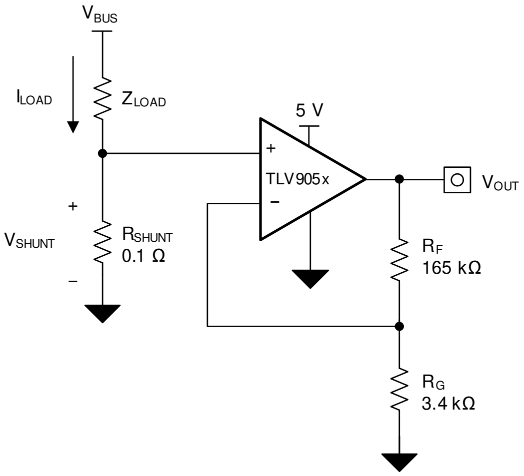


Figure 42. TLV905x in a Low-Side, Current-Sensing Application

9.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

Typical Low-Side Current Sense Application (continued)

9.2.2 Detailed Design Procedure

The transfer function of the circuit in Figure 42 is given in Equation 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using Equation 2.

$$R_{SHUNT} \quad \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} \quad \frac{100mV}{1A} = 100m\Omega \tag{2}$$

Using Equation 2, R_{SHUNT} equals 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV905x device to produce an output voltage of approximately 0 V to 4.95 V. Equation 3 calculates the gain required for the TLV905x device to produce the required output voltage.

$$Gain \quad \frac{\left(V_{OUT\_MAX} - V_{OUT\_MIN}\right)}{\left(V_{IN\_MAX} - V_{IN\_MIN}\right)} \tag{3}$$

Using Equation 3, the required gain equals 49.5 V/V, which is set with the R_F and R_G resistors. Equation 4 sizes the R_F and R_G, resistors to set the gain of the TLV905x device to 49.5 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \tag{4}$$

Selecting R_F to equal 165 kΩ and R_G to equal 3.4 kΩ provides a combination that equals approximately 49.5 V/V. Figure 43 shows the measured transfer function of the circuit shown in Figure 42.

9.2.3 Application Curve

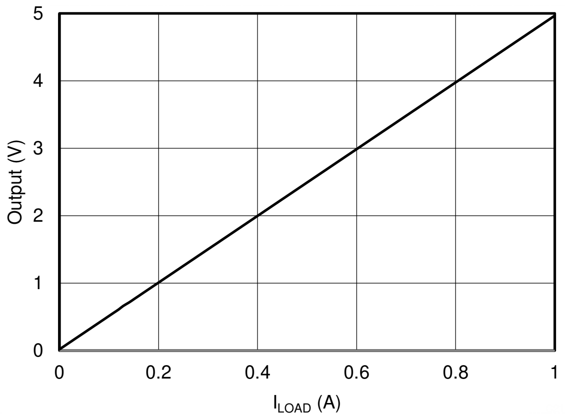


Figure 43. Low-Side, Current-Sense Transfer Function

10 Power Supply Recommendations

The TLV905x family is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more-detailed information on bypass capacitor placement, see the *Layout Example* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in Figure 45, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

11.2 Layout Example

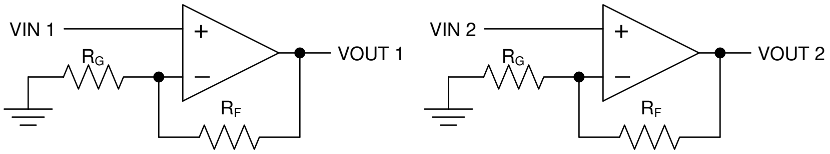
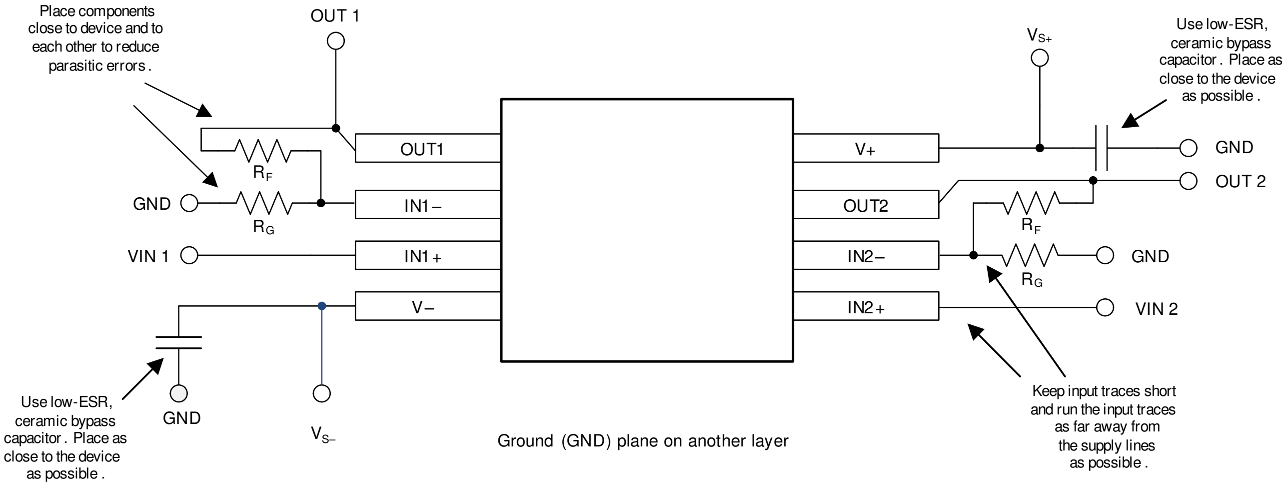


Figure 44. Schematic Representation for Figure 45



Place components close to device and to each other to reduce parasitic errors.

Use low-ESR, ceramic bypass capacitor. Place as close to the device as possible.

Use low-ESR, ceramic bypass capacitor. Place as close to the device as possible.

Ground (GND) plane on another layer

Keep input traces short and run the input traces as far away from the supply lines as possible.

Figure 45. Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

Texas Instruments, *TLVx313 Low-Power, Rail-to-Rail In/Out, 500-µV Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems*

Texas Instruments, *TLVx314 3-MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier*

Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers*

Texas Instruments, *QFN/SON PCB Attachment*

Texas Instruments, *Quad Flatpack No-Lead Logic Packages*

Texas Instruments, *Circuit Board Layout Techniques*

Texas Instruments, *Single-Ended Input to Differential Output Conversion Circuit Reference Design*

12.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

Table 2. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV9051/S	Click here	Click here	Click here	Click here	Click here
TLV9052/S	Click here	Click here	Click here	Click here	Click here
TLV9054/S	Click here	Click here	Click here	Click here	Click here

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9051IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	Call TI | SN | NIPDAU	Level-1-260C-UNLIM	-40 to 125	T51D	Samples
TLV9051IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T51	Samples
TLV9051IDPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	FH	Samples
TLV9051SIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T51S	Samples
TLV9052IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T052	Samples
TLV9052IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1PWX	Samples
TLV9052IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL9052	Samples
TLV9052IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	9052	Samples
TLV9052IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL9052	Samples
TLV9052SIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T052	Samples
TLV9052SIRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	FPF	Samples
TLV9054IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9054D	Samples
TLV9054IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T9054PW	Samples
TLV9054IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T54RT	Samples
TLV9054IRUCR	ACTIVE	QFN	RUC	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1FF	Samples
TLV9054SIRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9054S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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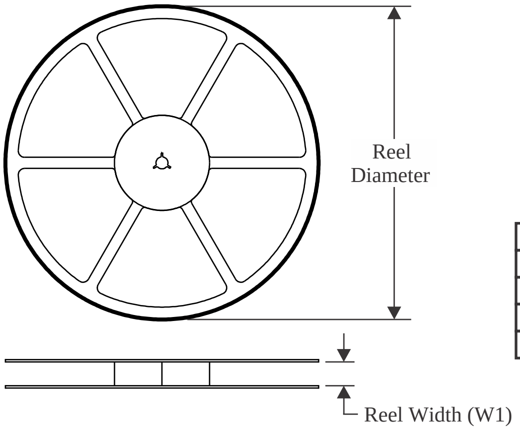
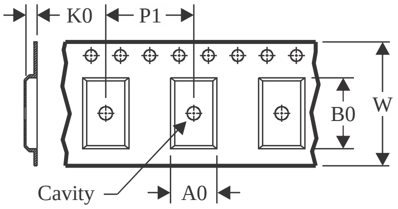
TAPE AND REEL INFORMATION

REEL DIMENSIONS

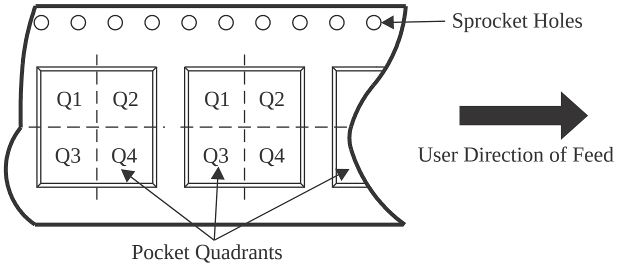


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

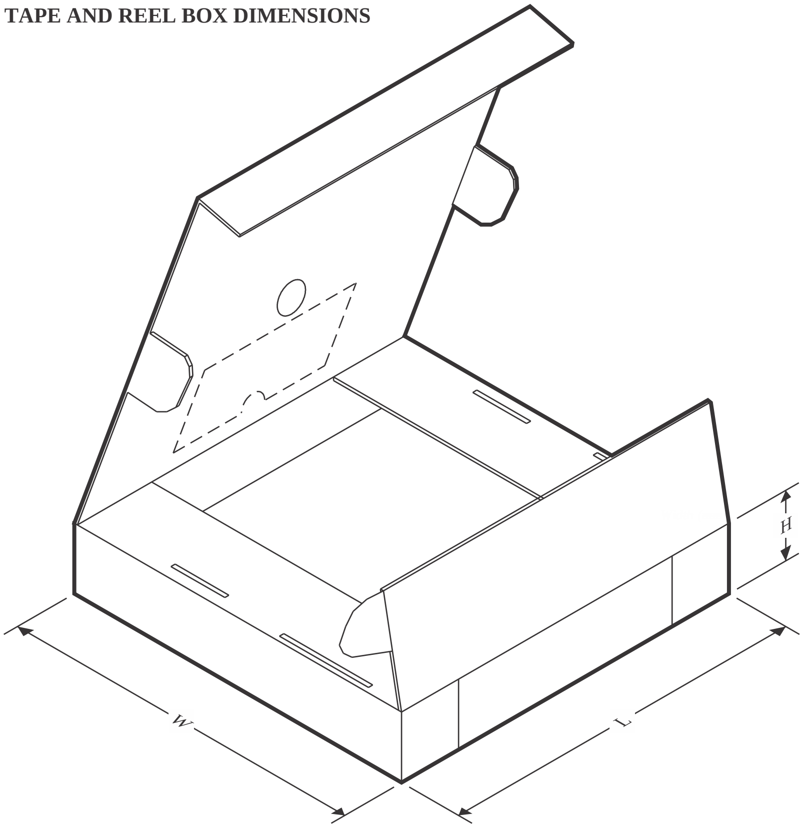


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9051IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9051IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9051IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9051IDPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV9051SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9052IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9052IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9052IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9052IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9052IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9052IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9052SIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9052SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1
TLV9054IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9054IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV9054IRUCR	QFN	RUC	14	3000	180.0	9.5	2.16	2.16	0.5	4.0	8.0	Q2
TLV9054SIRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



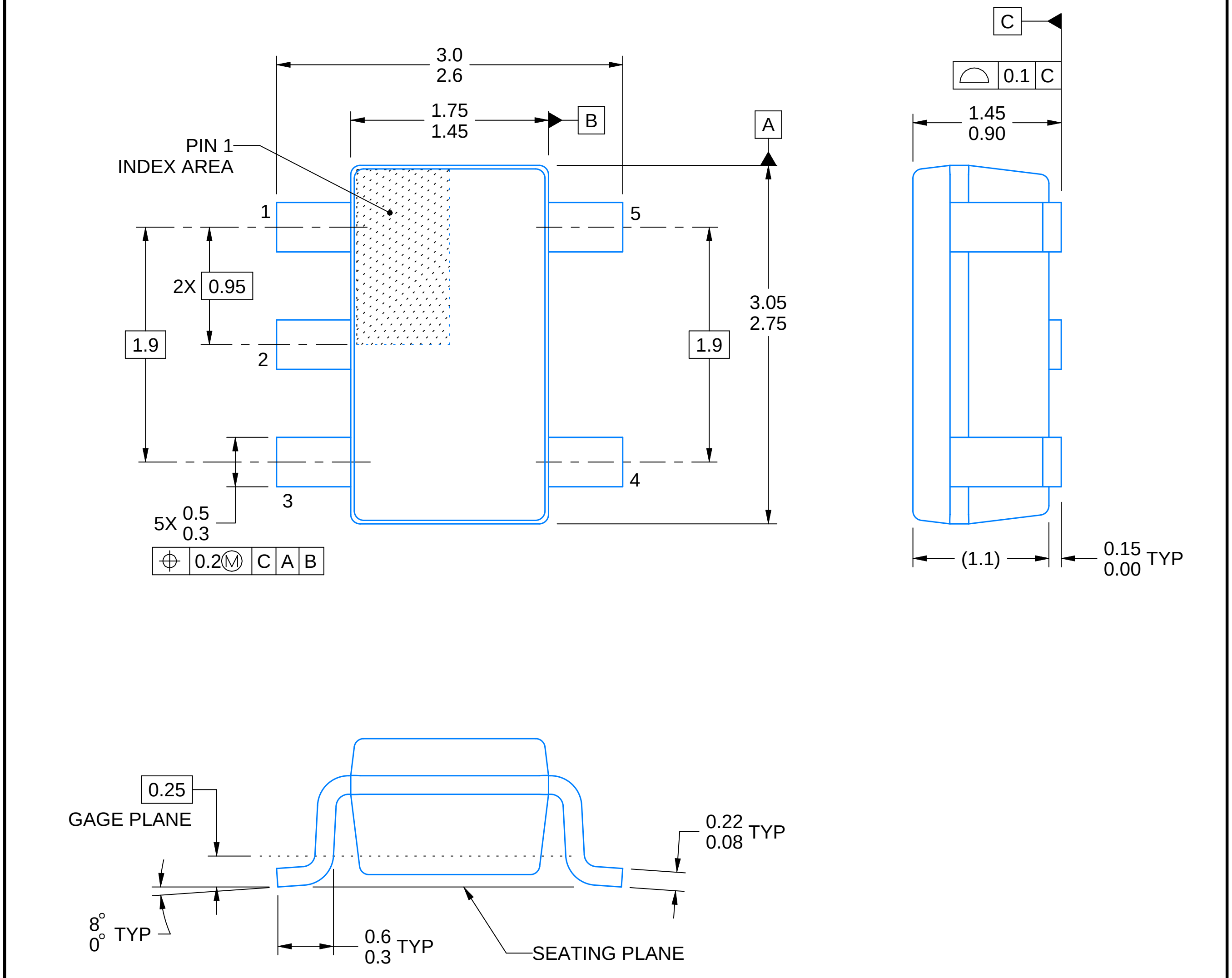
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9051IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9051IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9051IDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV9051IDPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV9051SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9052IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9052IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9052IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9052IDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV9052IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9052IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV9052SIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TLV9052SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0
TLV9054IDR	SOIC	D	14	2500	356.0	356.0	35.0
TLV9054IPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
TLV9054IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TLV9054IRUCR	QFN	RUC	14	3000	205.0	200.0	30.0
TLV9054SIRTER	WQFN	RTE	16	3000	367.0	367.0	35.0

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

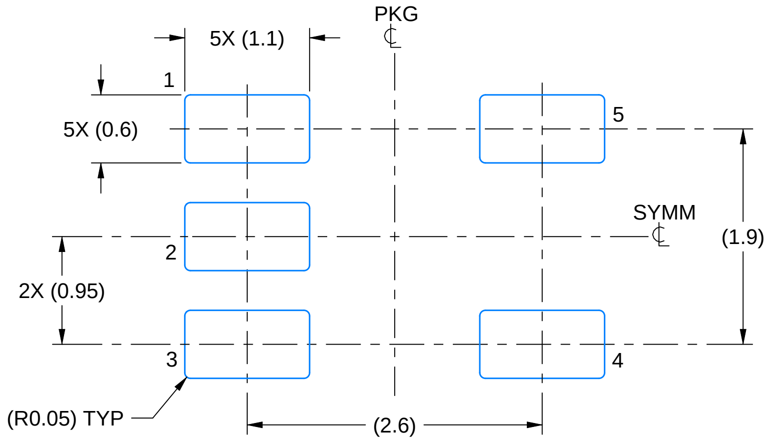
SMALL OUTLINE TRANSISTOR



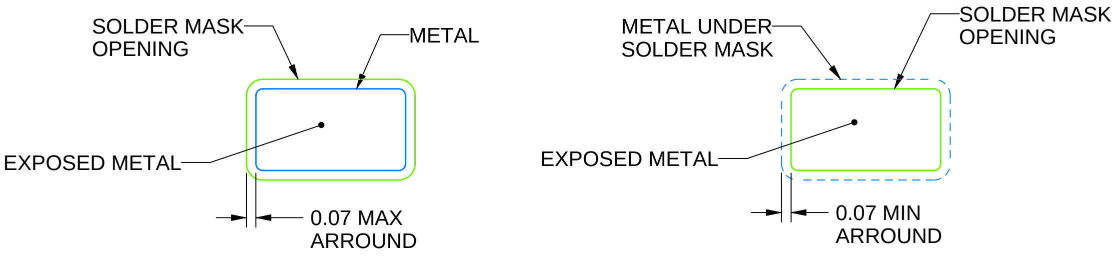
4214839/F 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



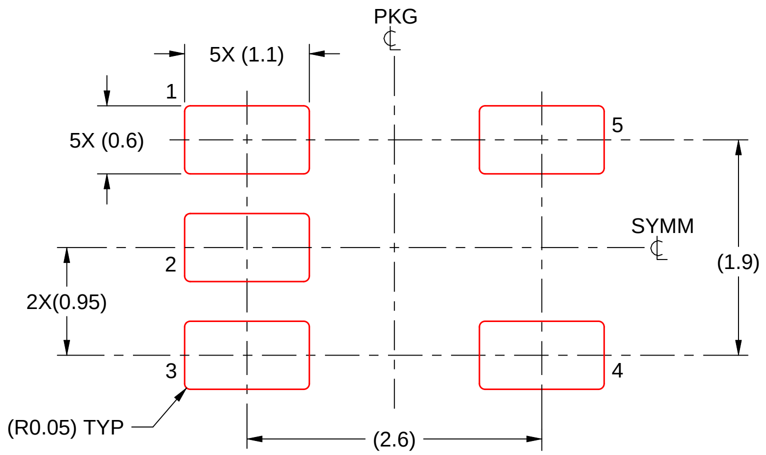
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

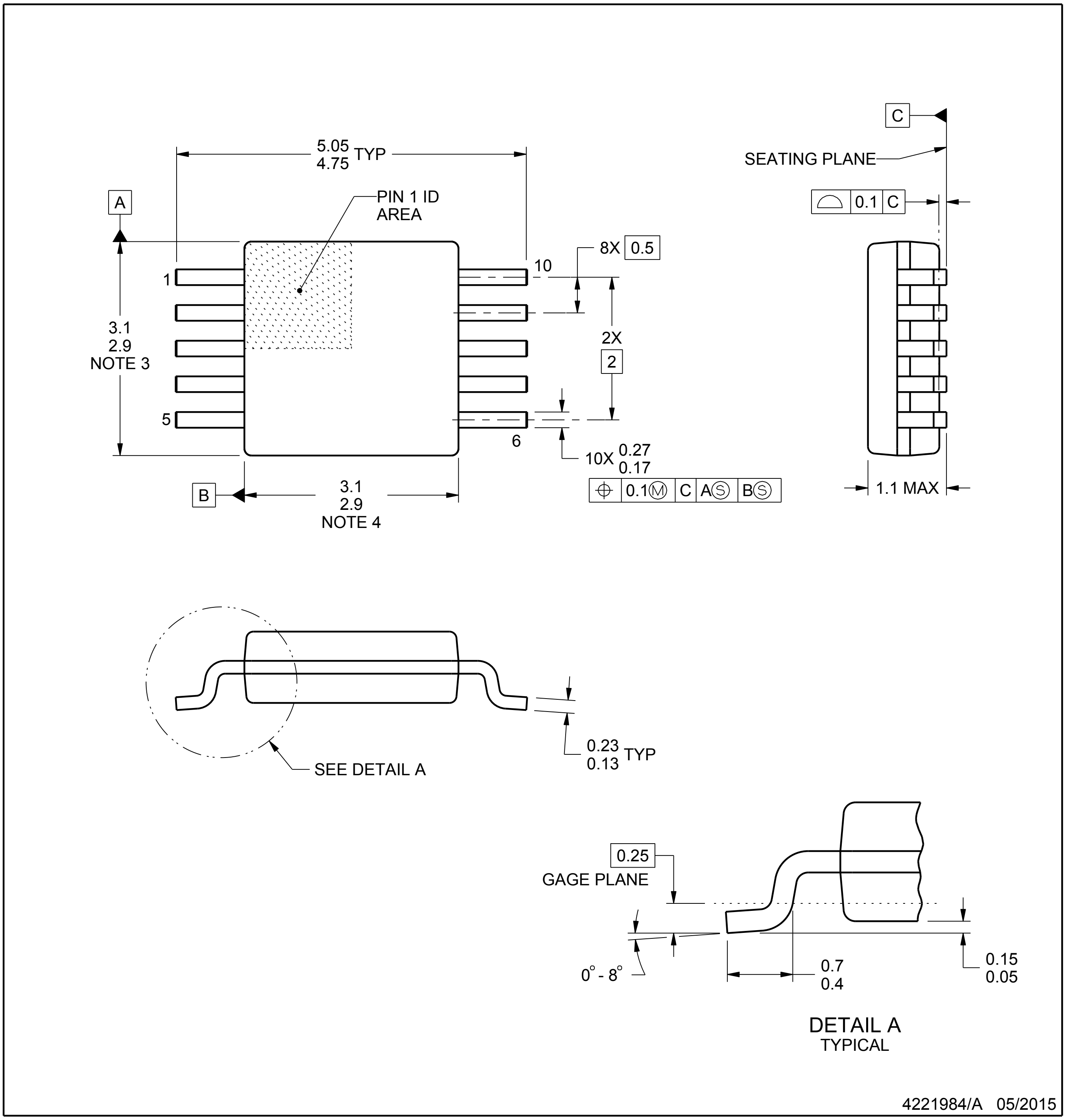
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

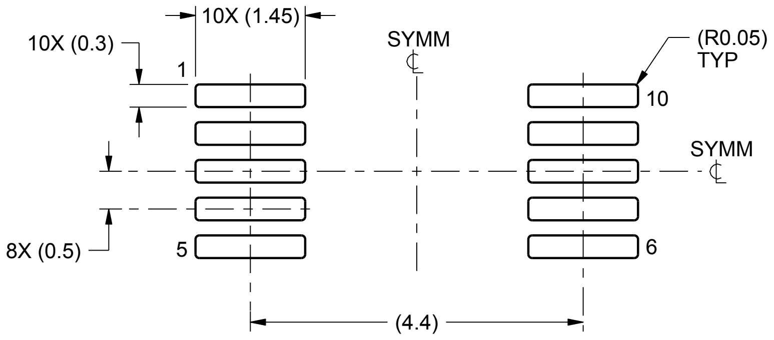
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

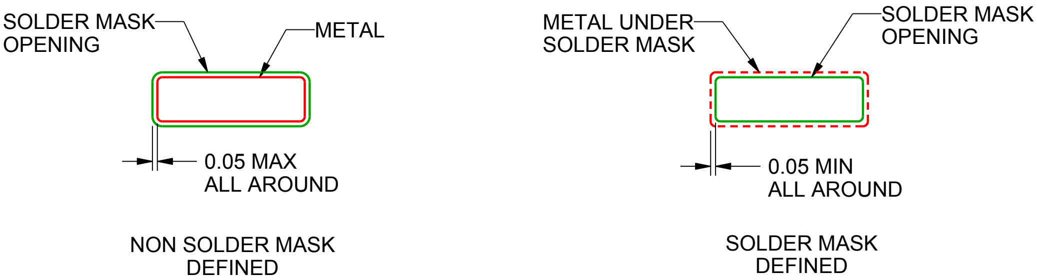


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



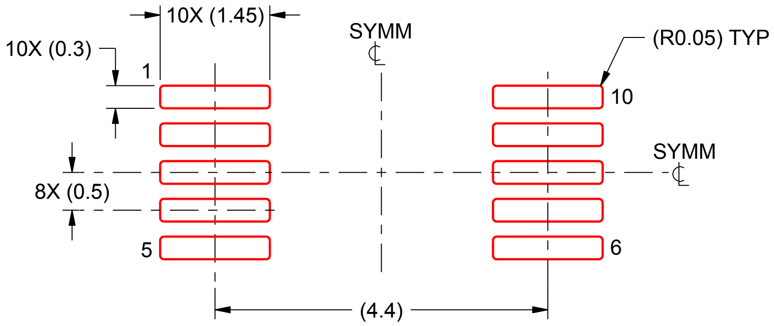
LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

NOTES: (continued)

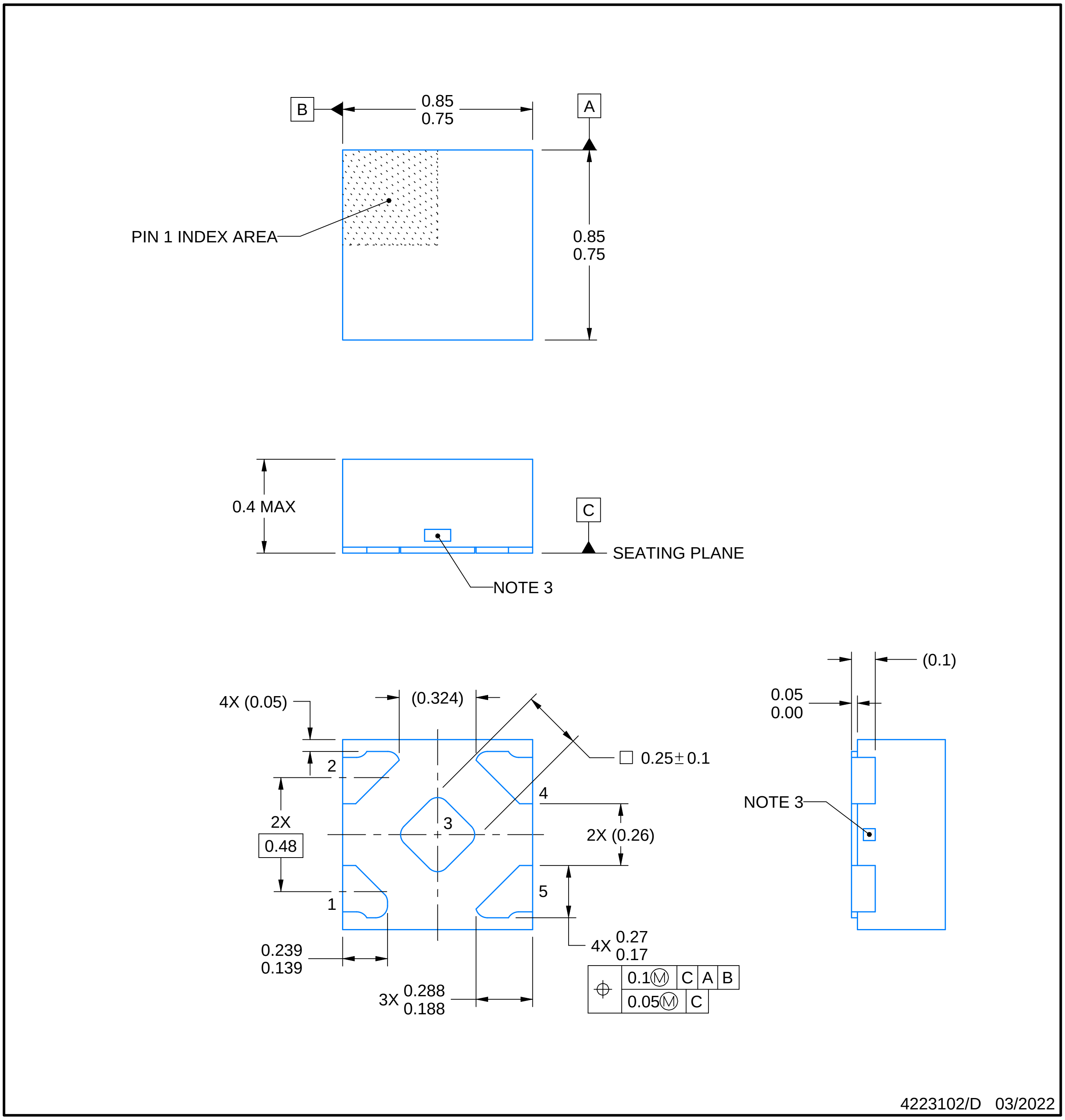
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5 **X2SON - 0.4 mm max height**

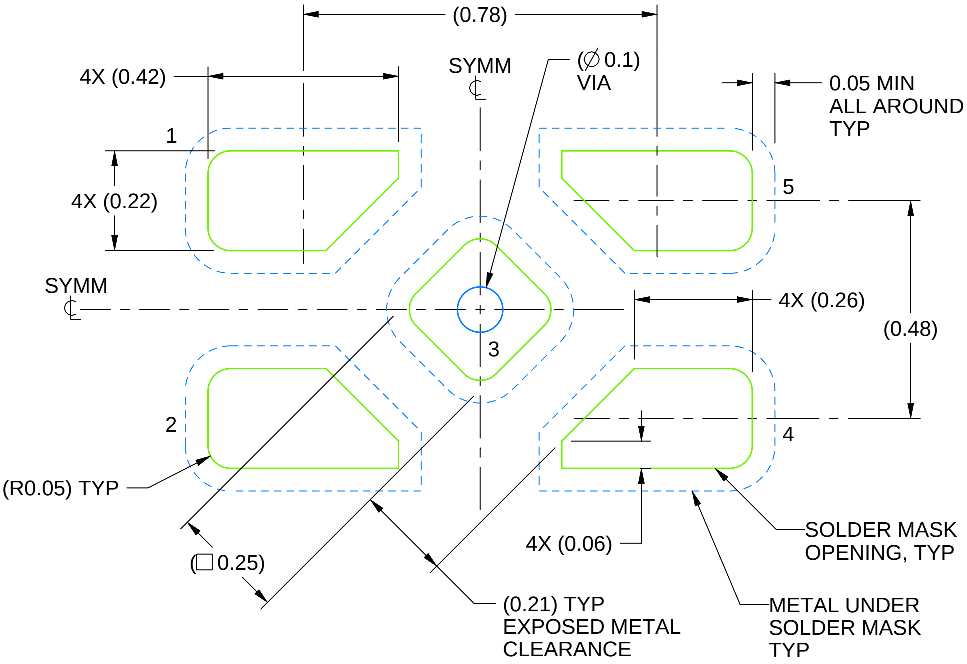
PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



NOTES:

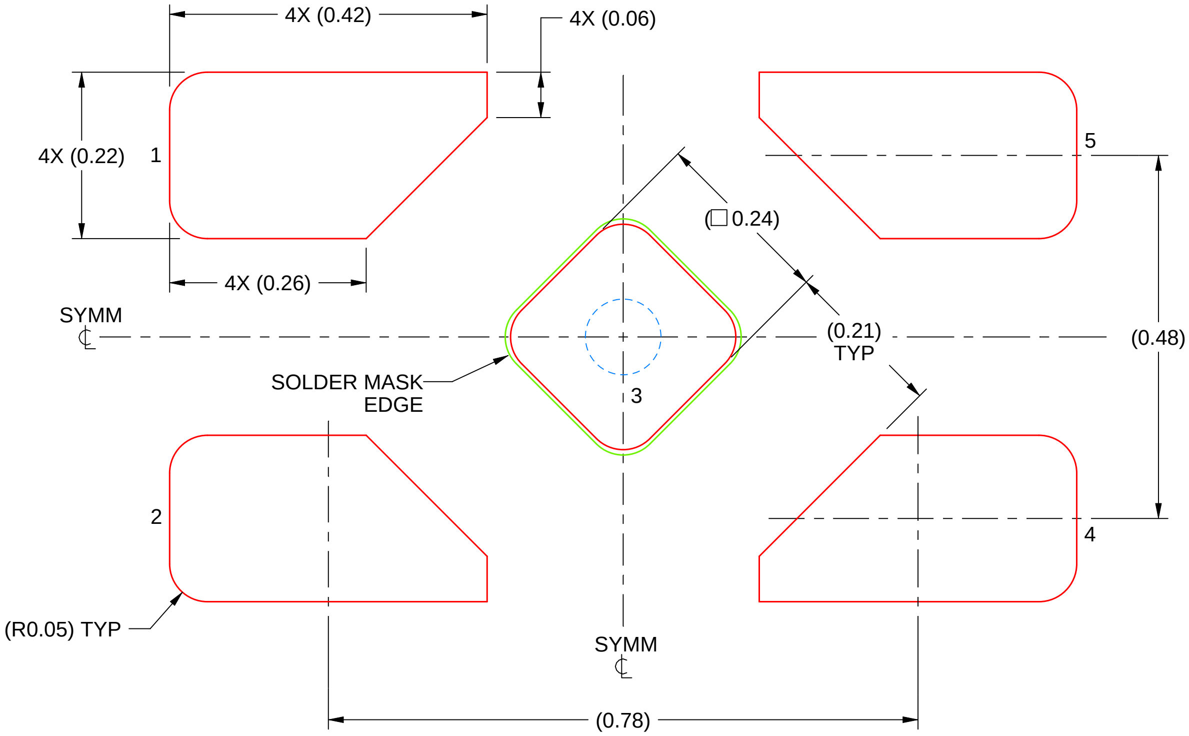
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).



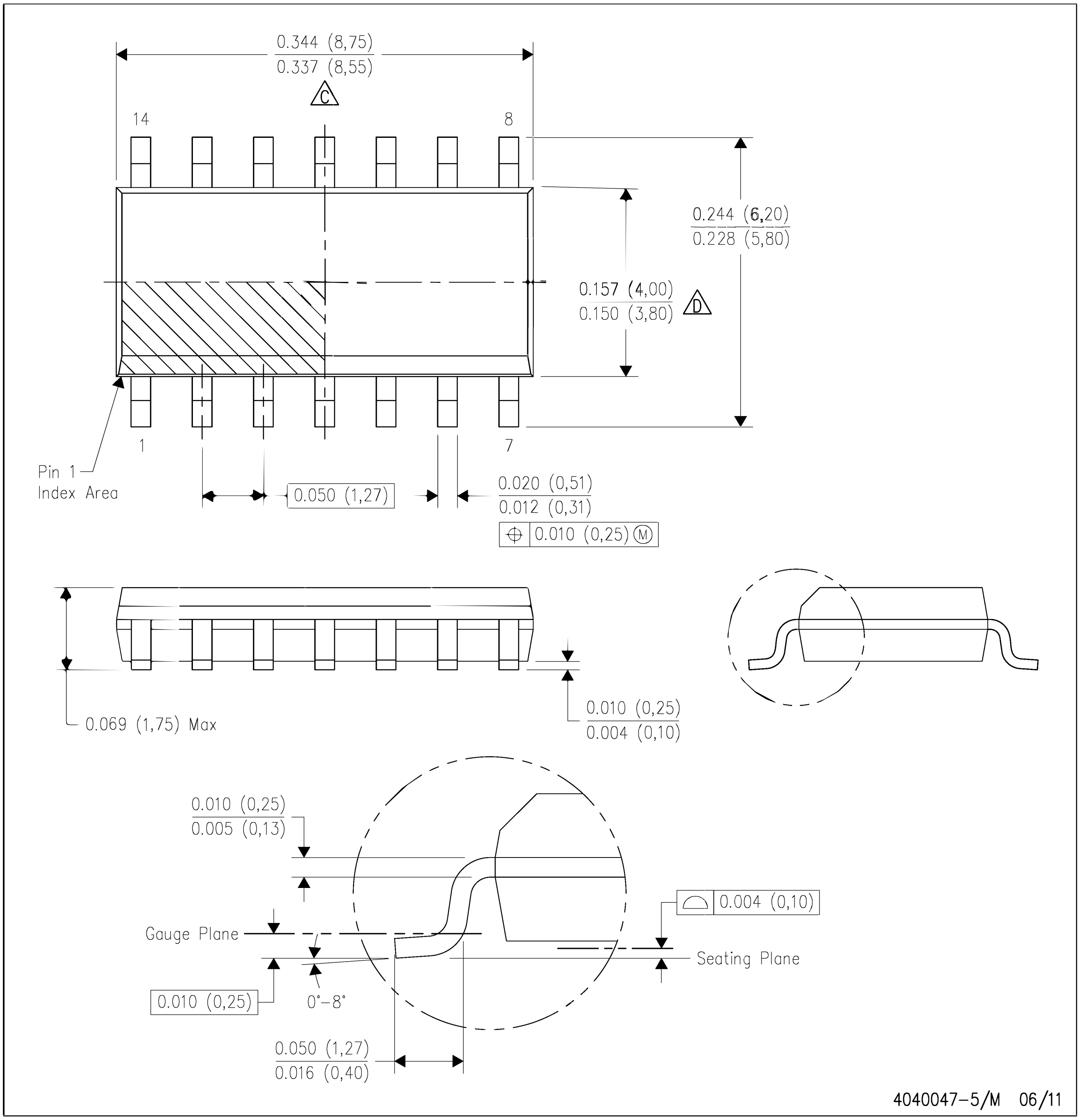
SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

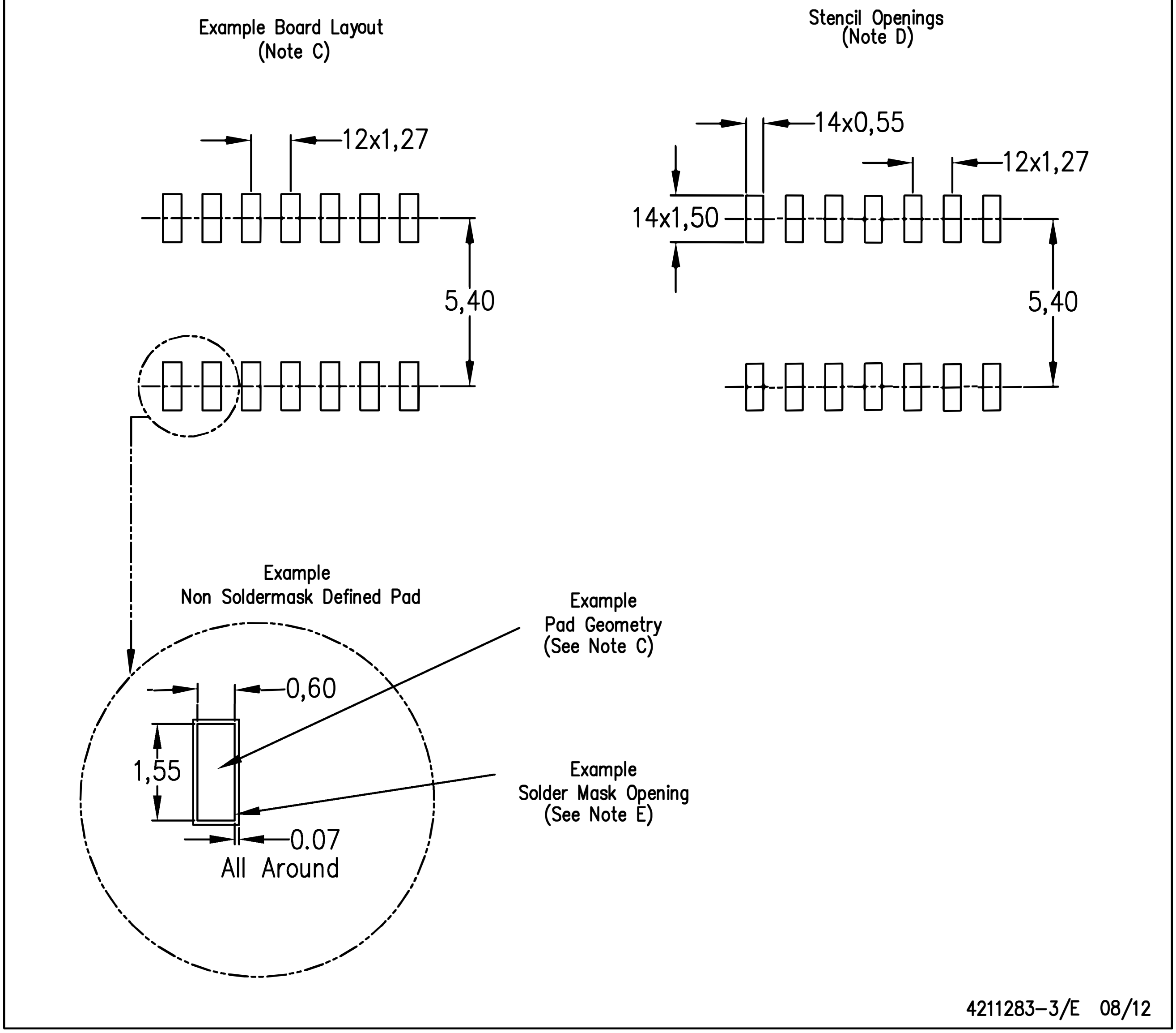
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

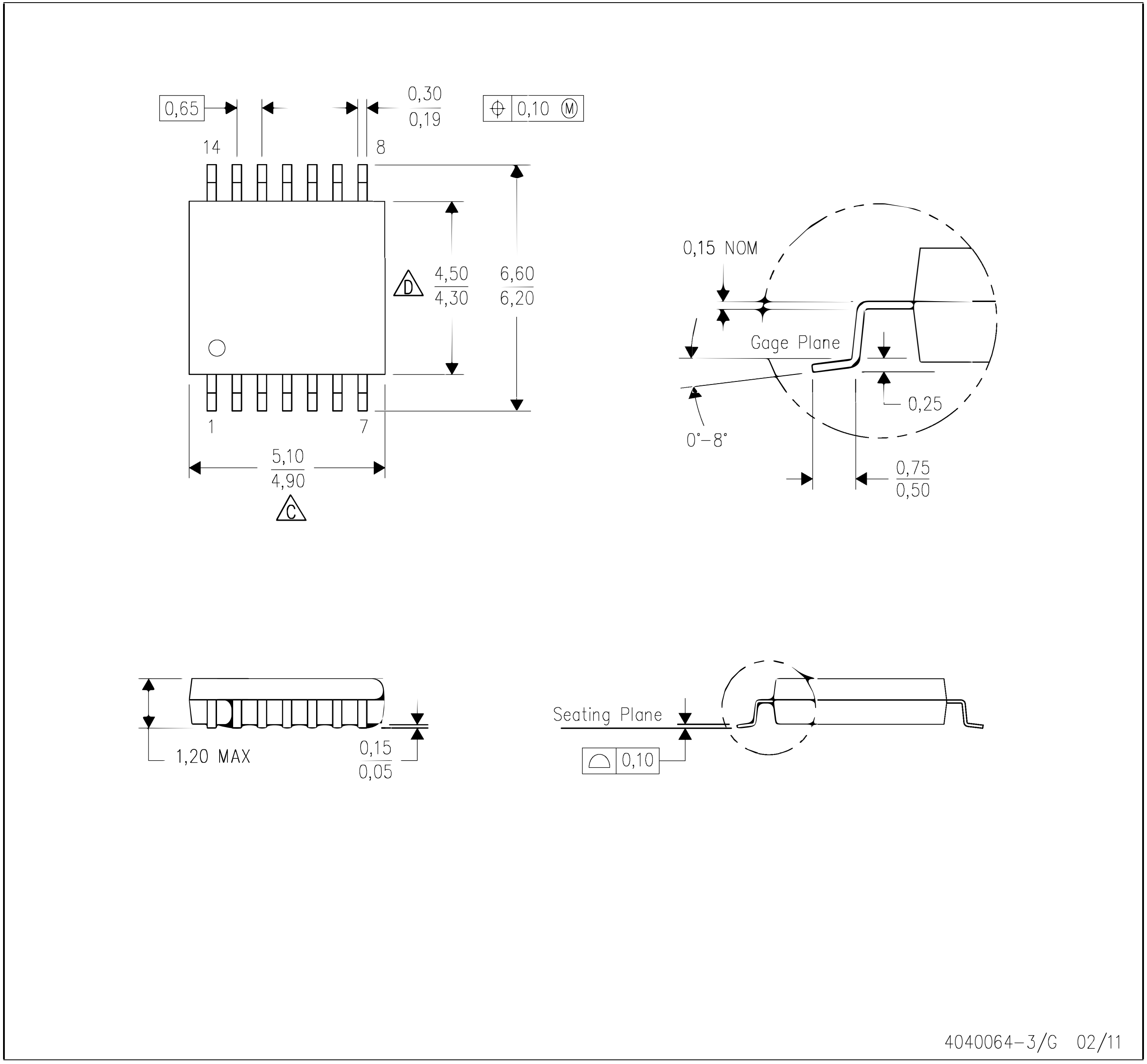
D (R-PDSO-G14) PLASTIC SMALL OUTLINE



4211283-3/E 08/12

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.

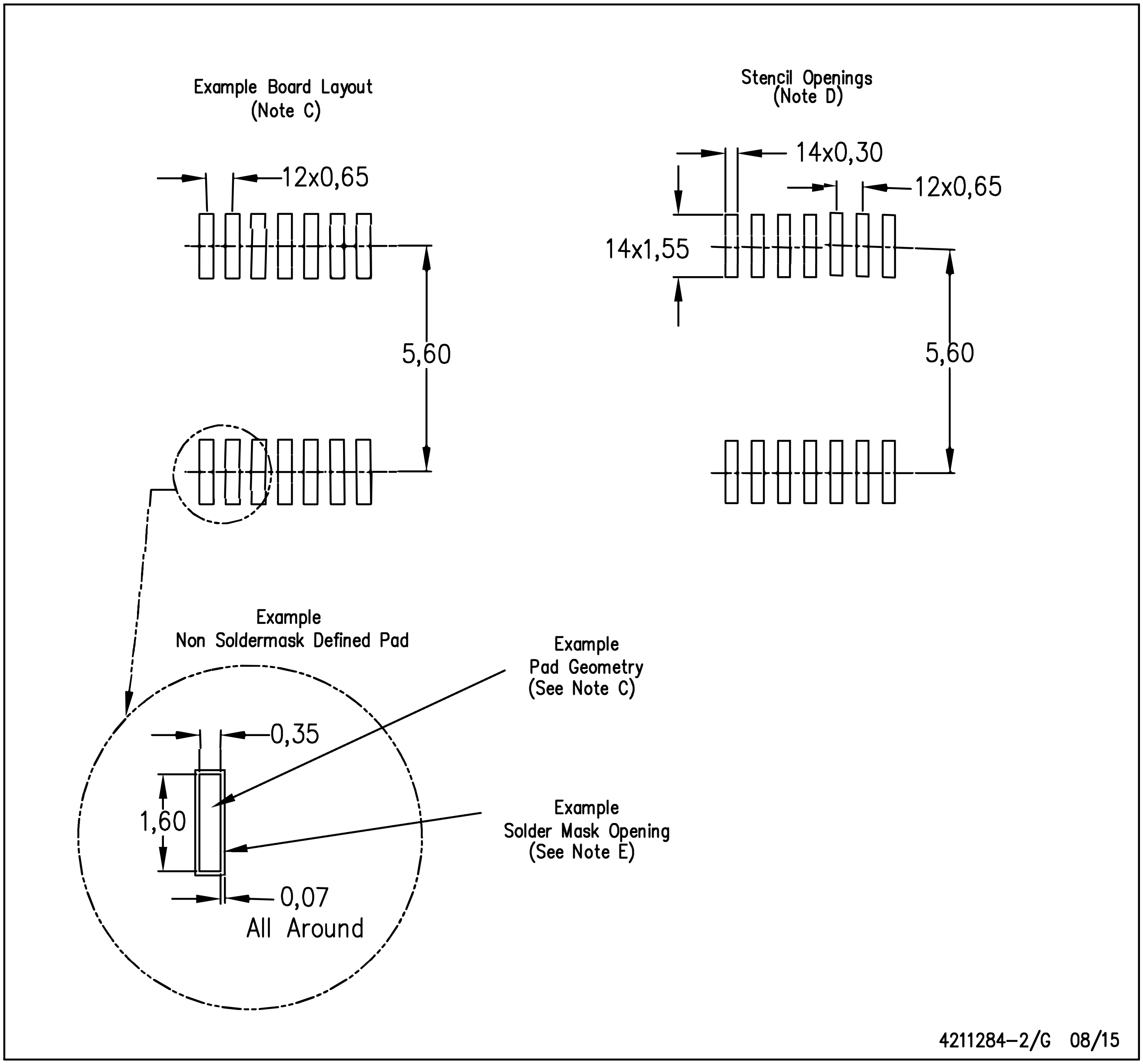
B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

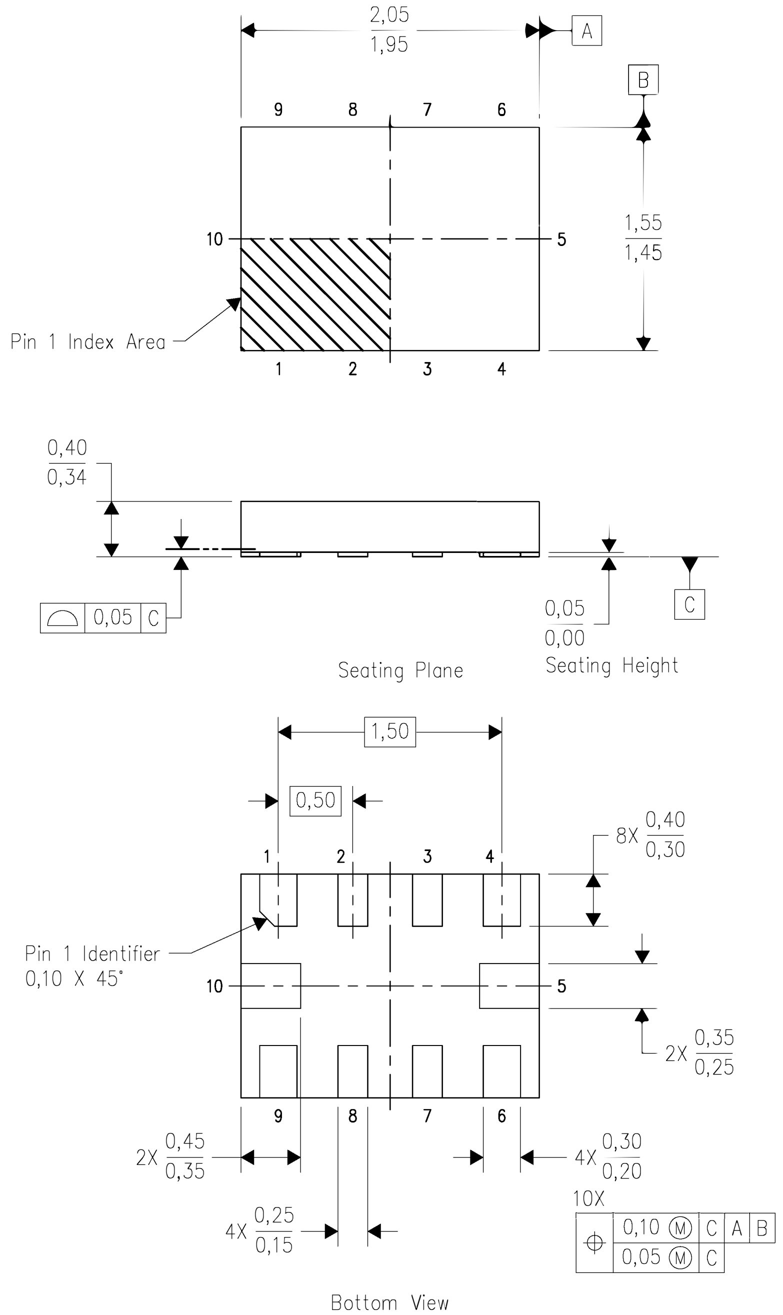
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

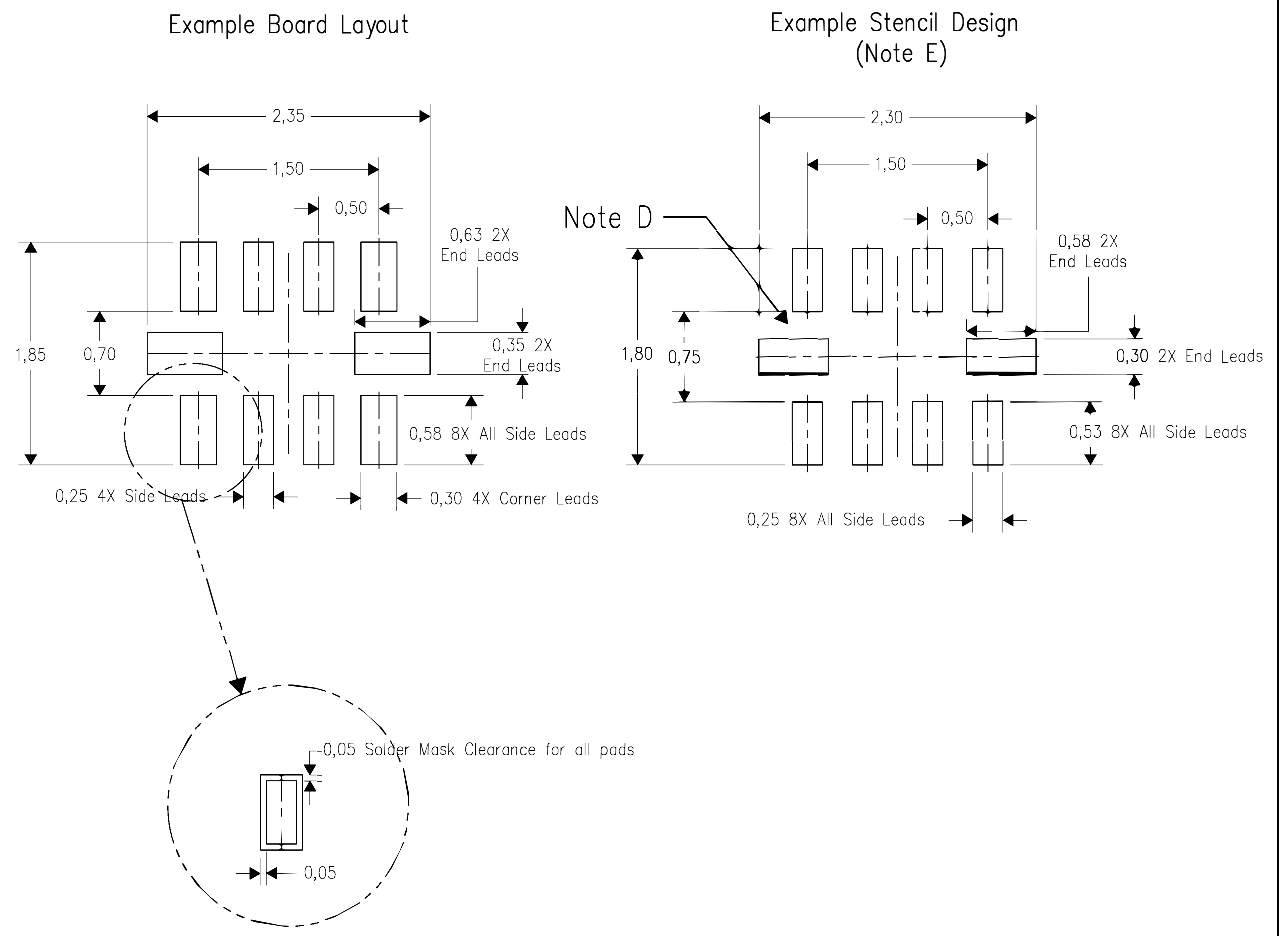
RUG (R-PQFP-N10) PLASTIC QUAD FLATPACK



4208528-3/B 04/2008

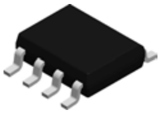
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. This package complies to JEDEC MO-288 variation X2EFD.

RUG (R–PQFP–N10)



4210299–3/A 06/09

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
- E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
- F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

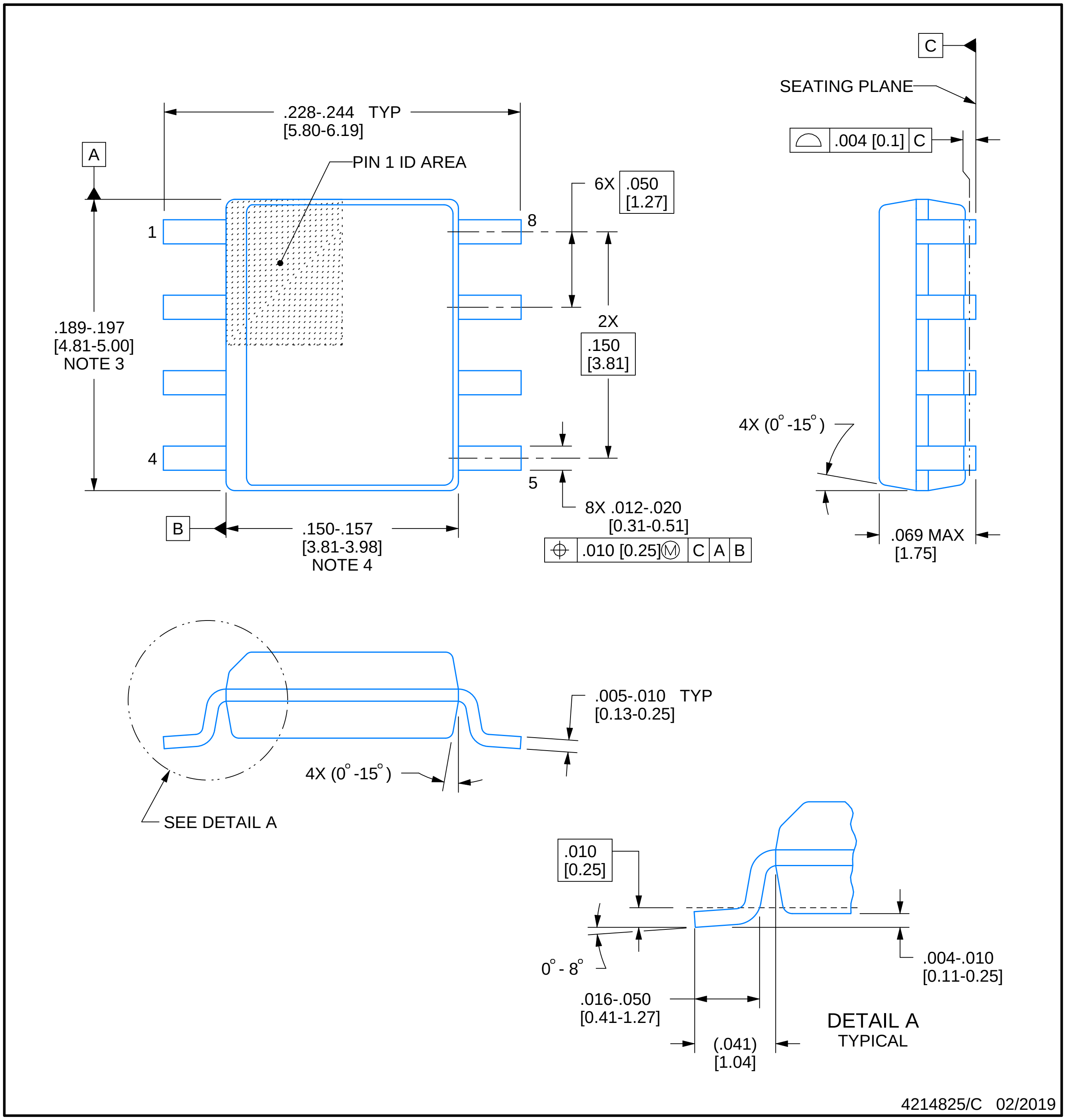


D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

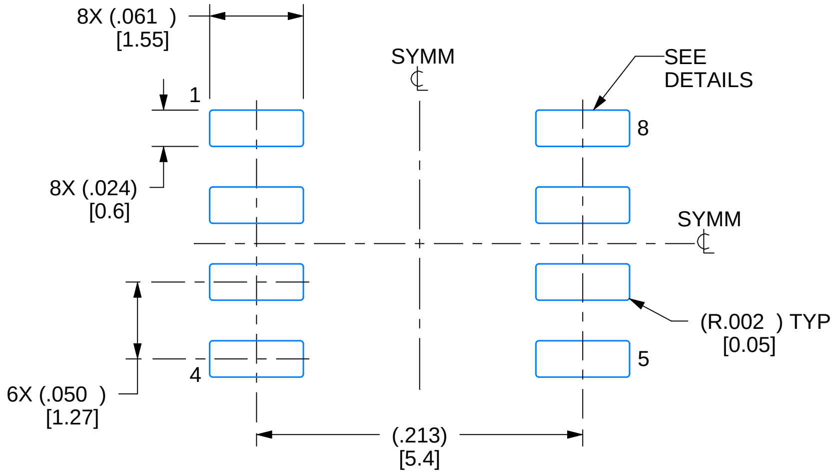
SMALL OUTLINE INTEGRATED CIRCUIT



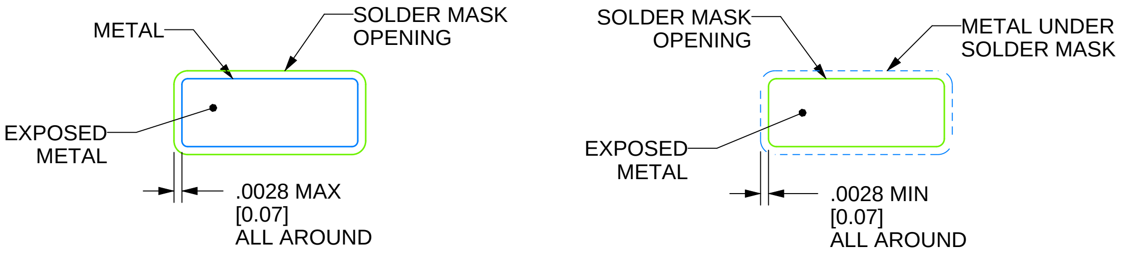
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



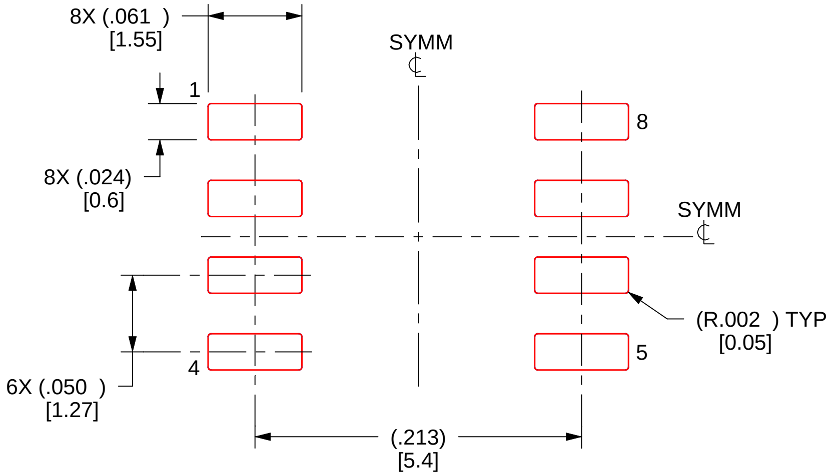
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

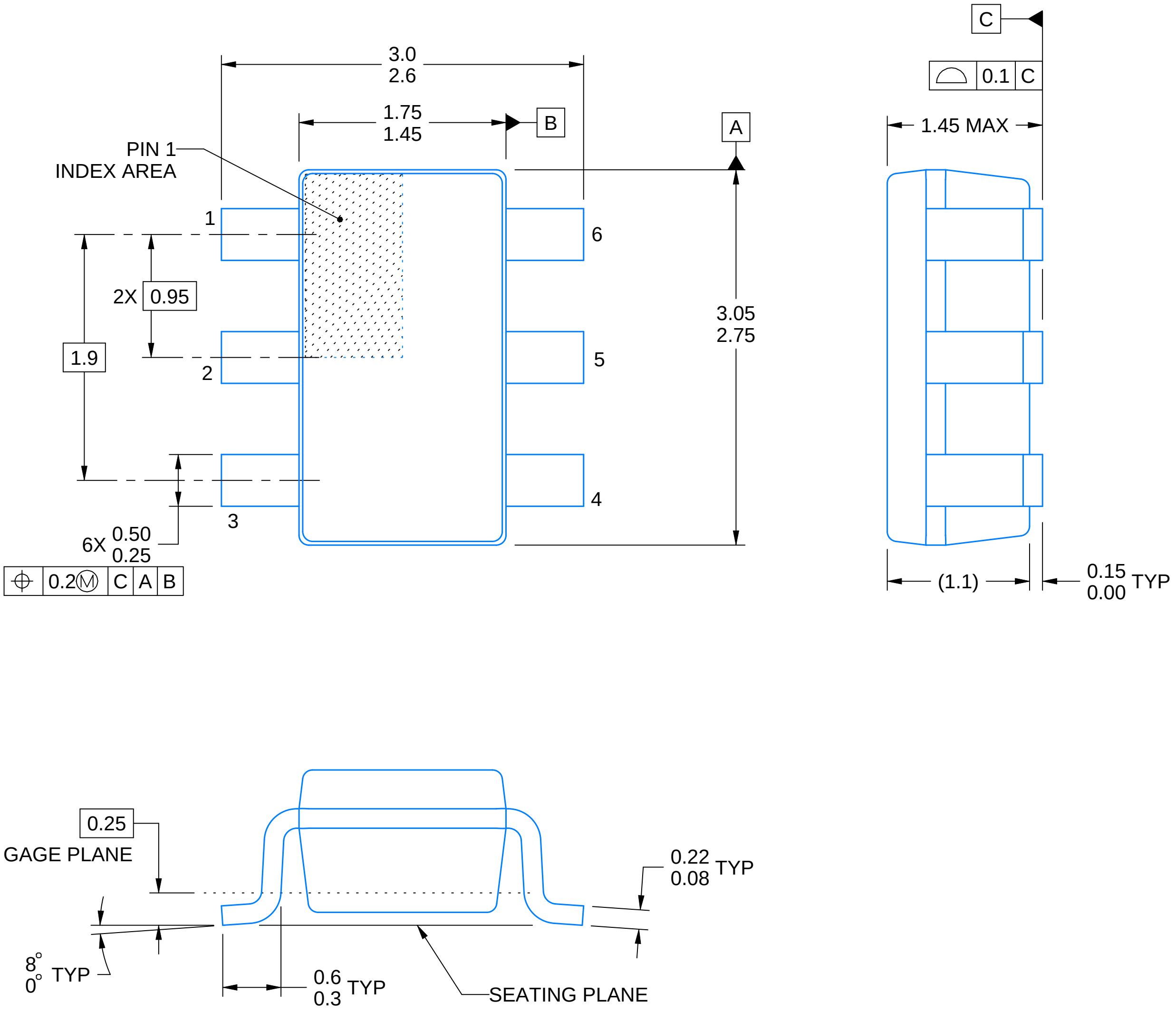
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DBV0006A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

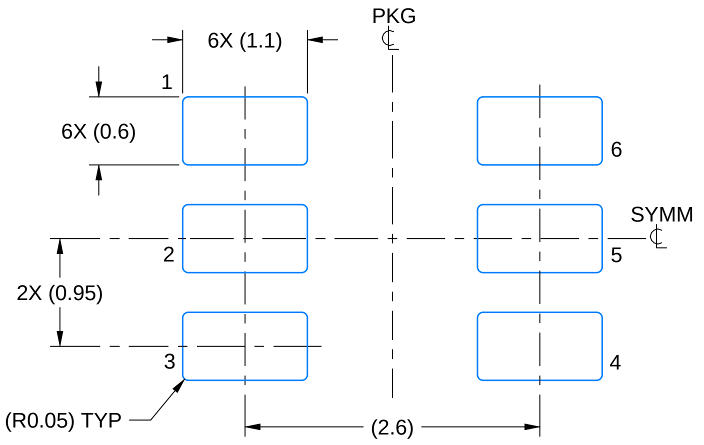
SMALL OUTLINE TRANSISTOR



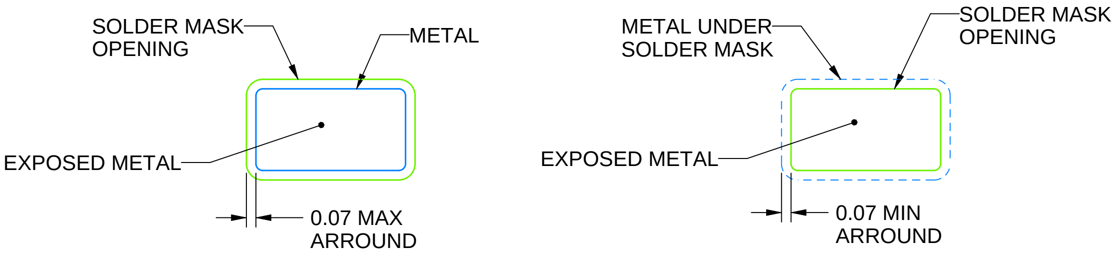
4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



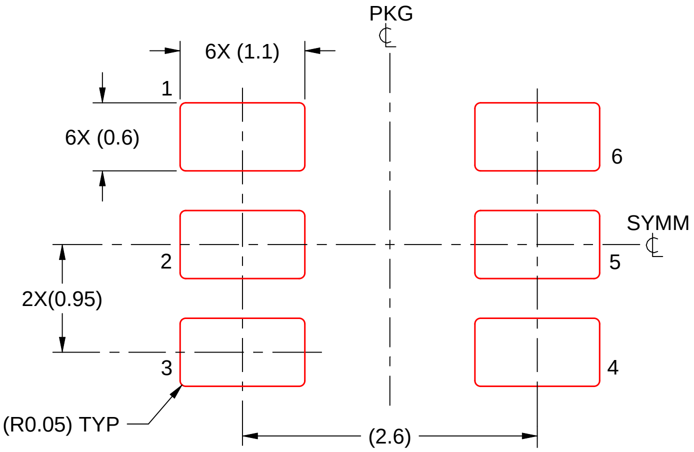
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

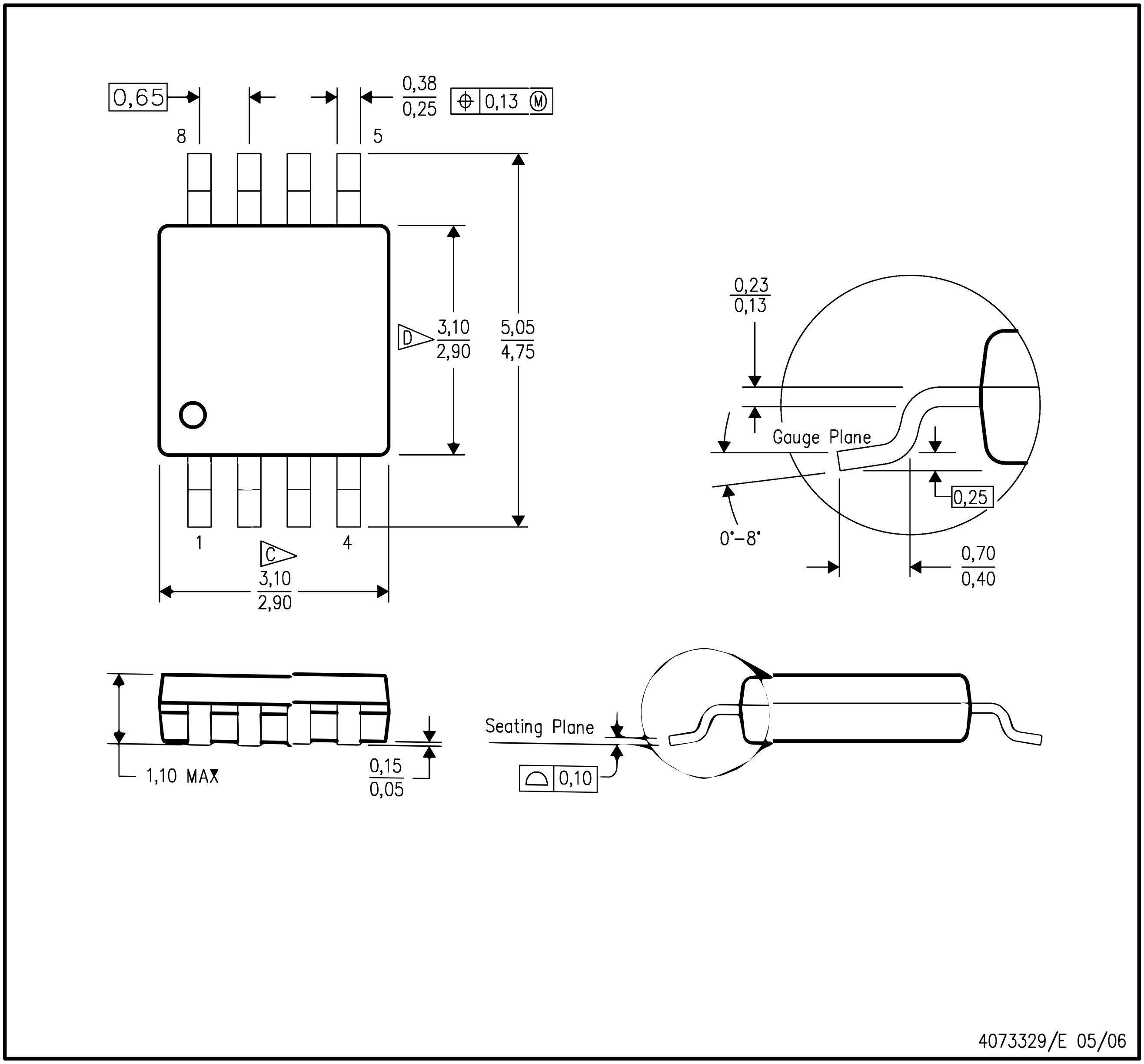


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

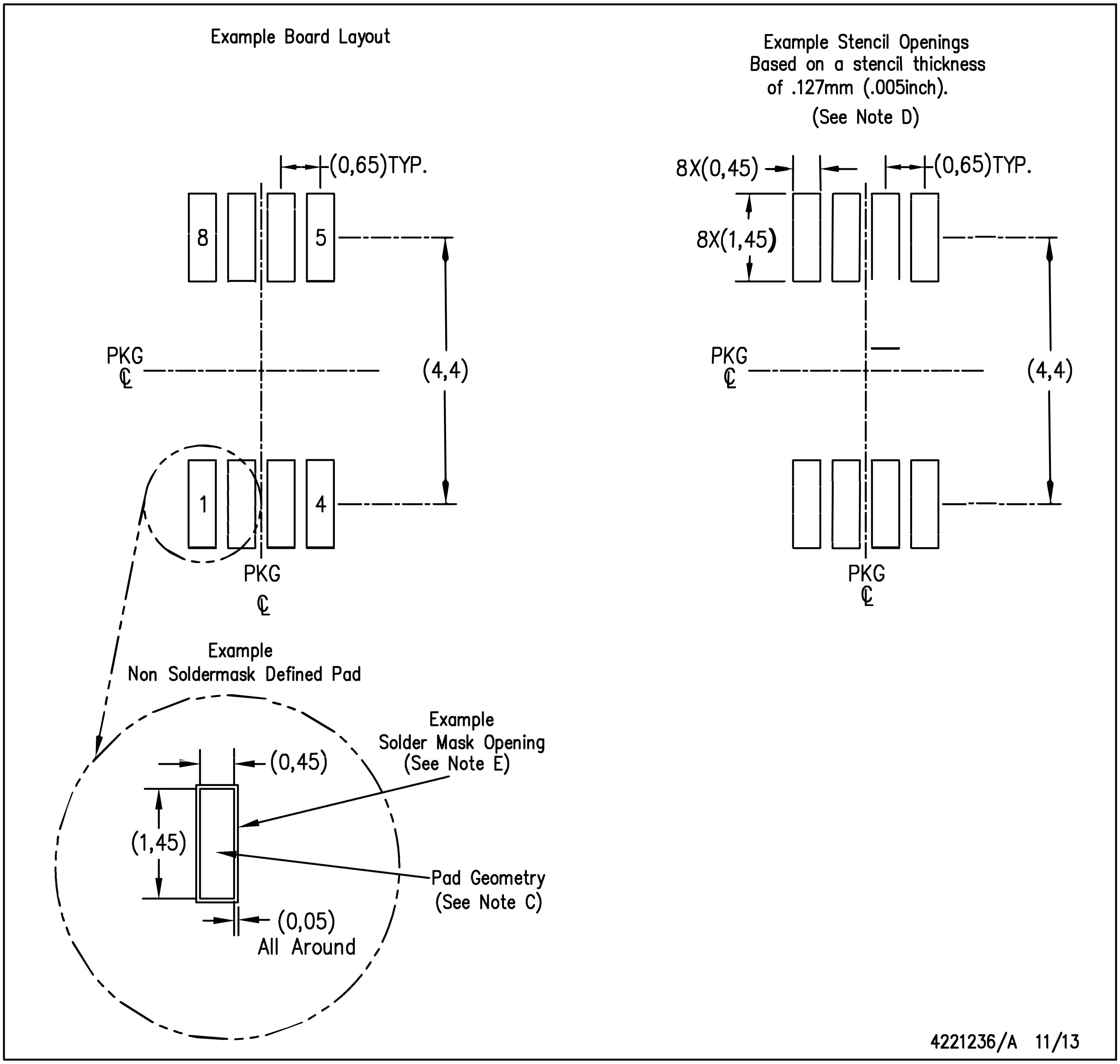
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

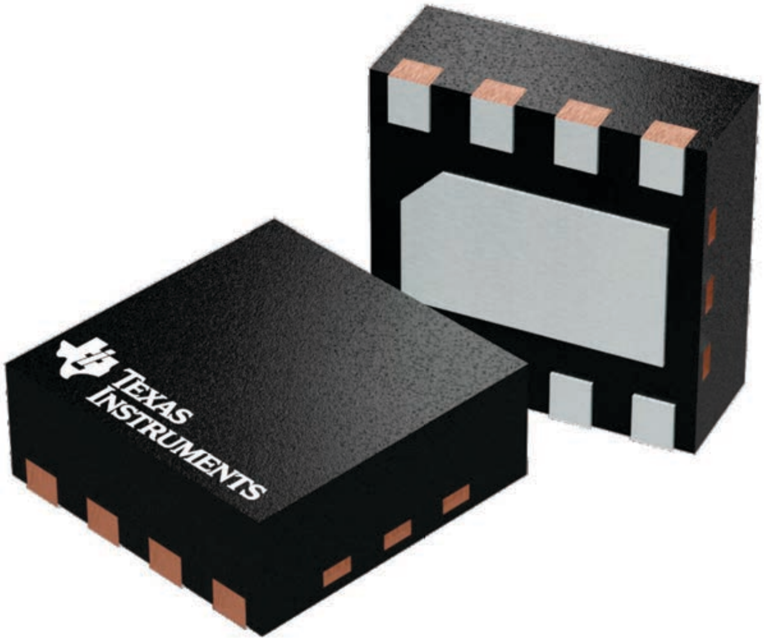
DSG 8

WSON - 0.8 mm max height

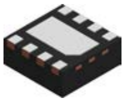
2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



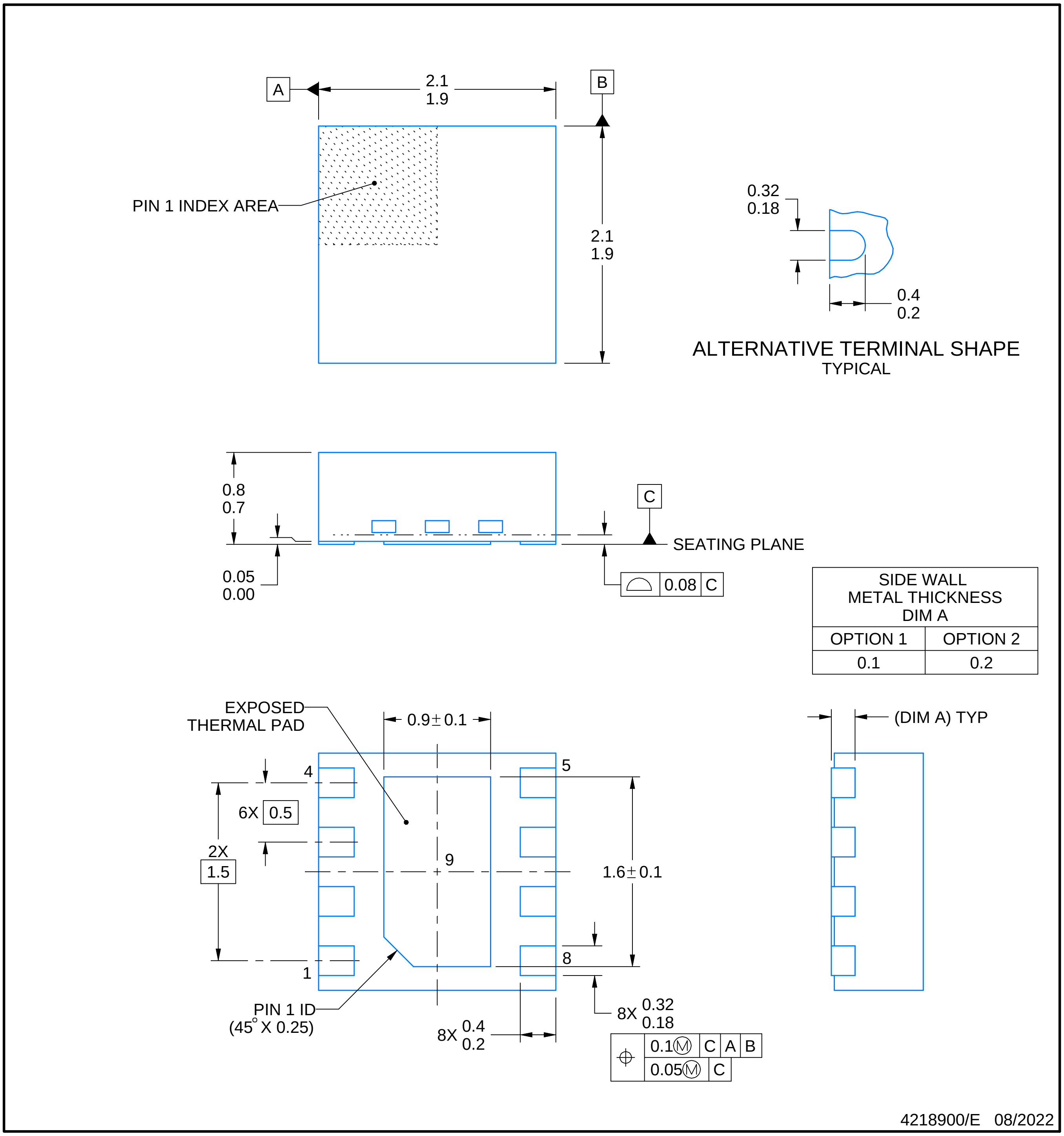
DSG0008A



PACKAGE OUTLINE

WSON - 0.8 mm max height

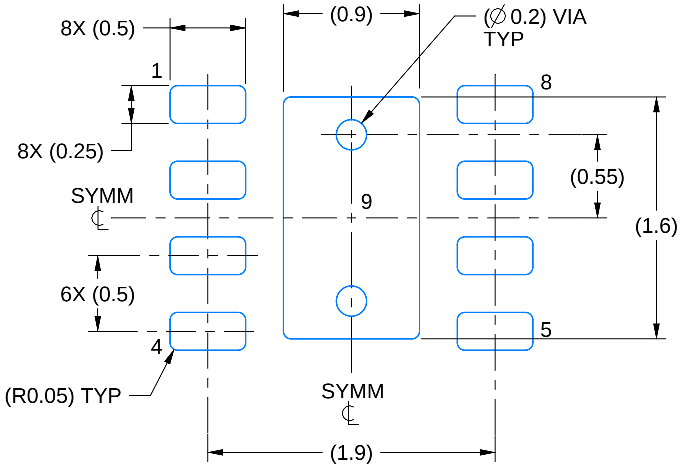
PLASTIC SMALL OUTLINE - NO LEAD



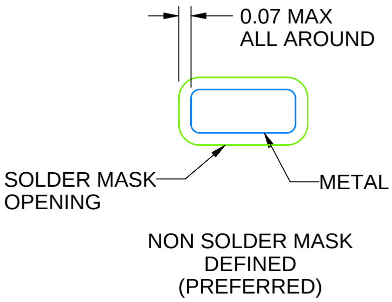
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

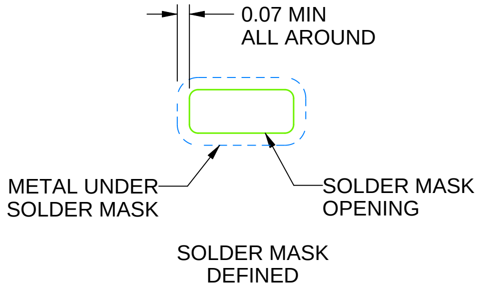
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

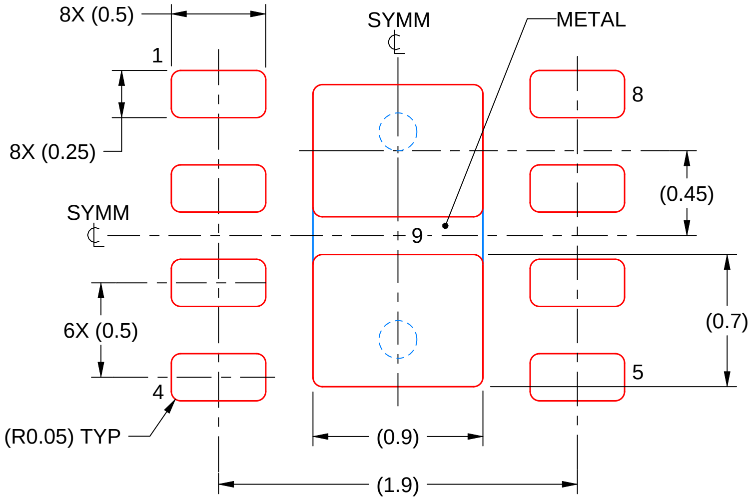


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



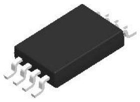
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

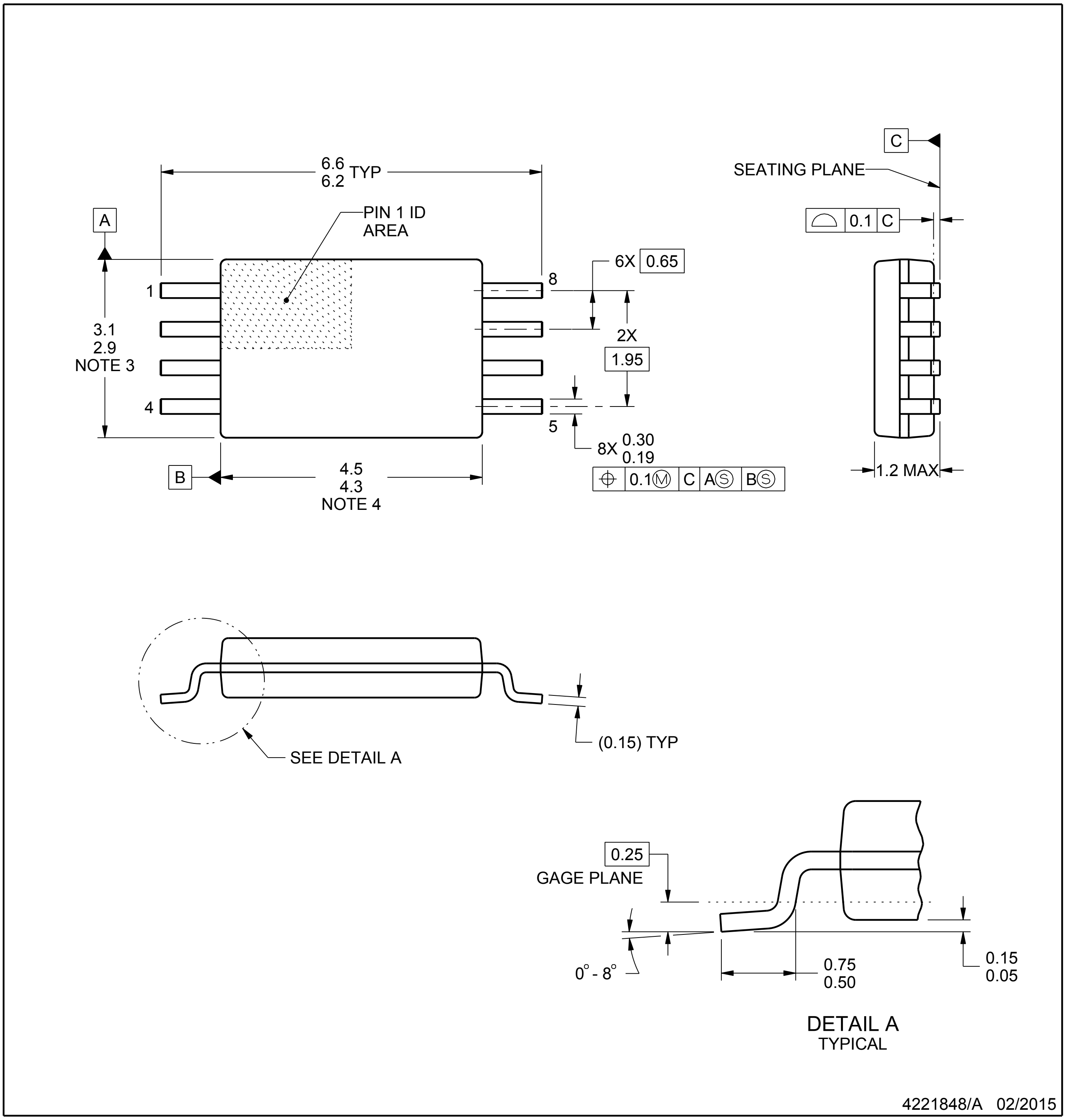
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

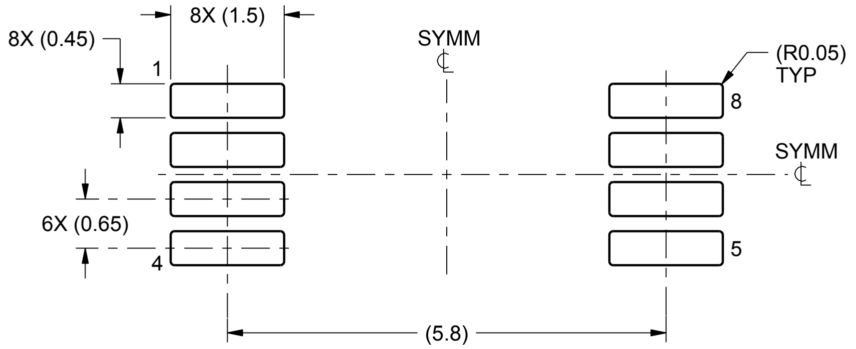
SMALL OUTLINE PACKAGE



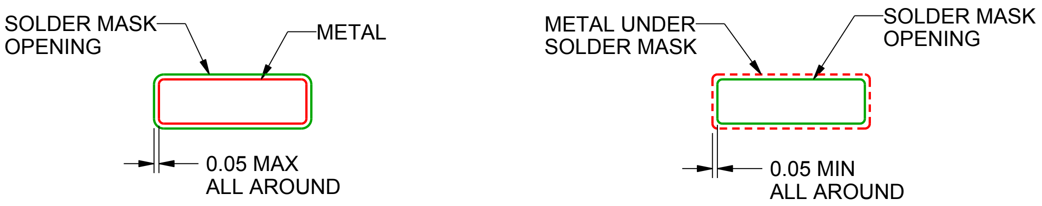
4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



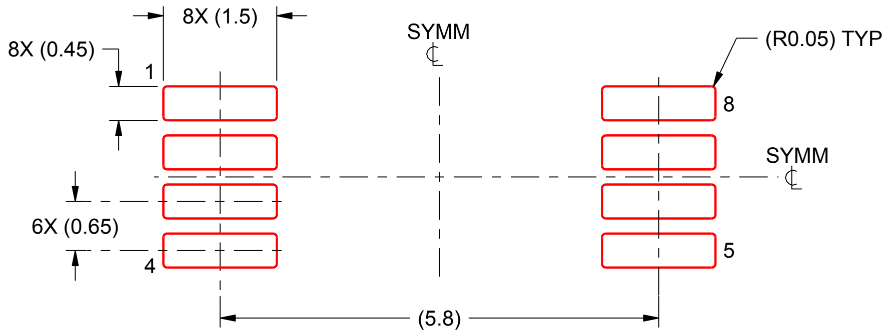
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

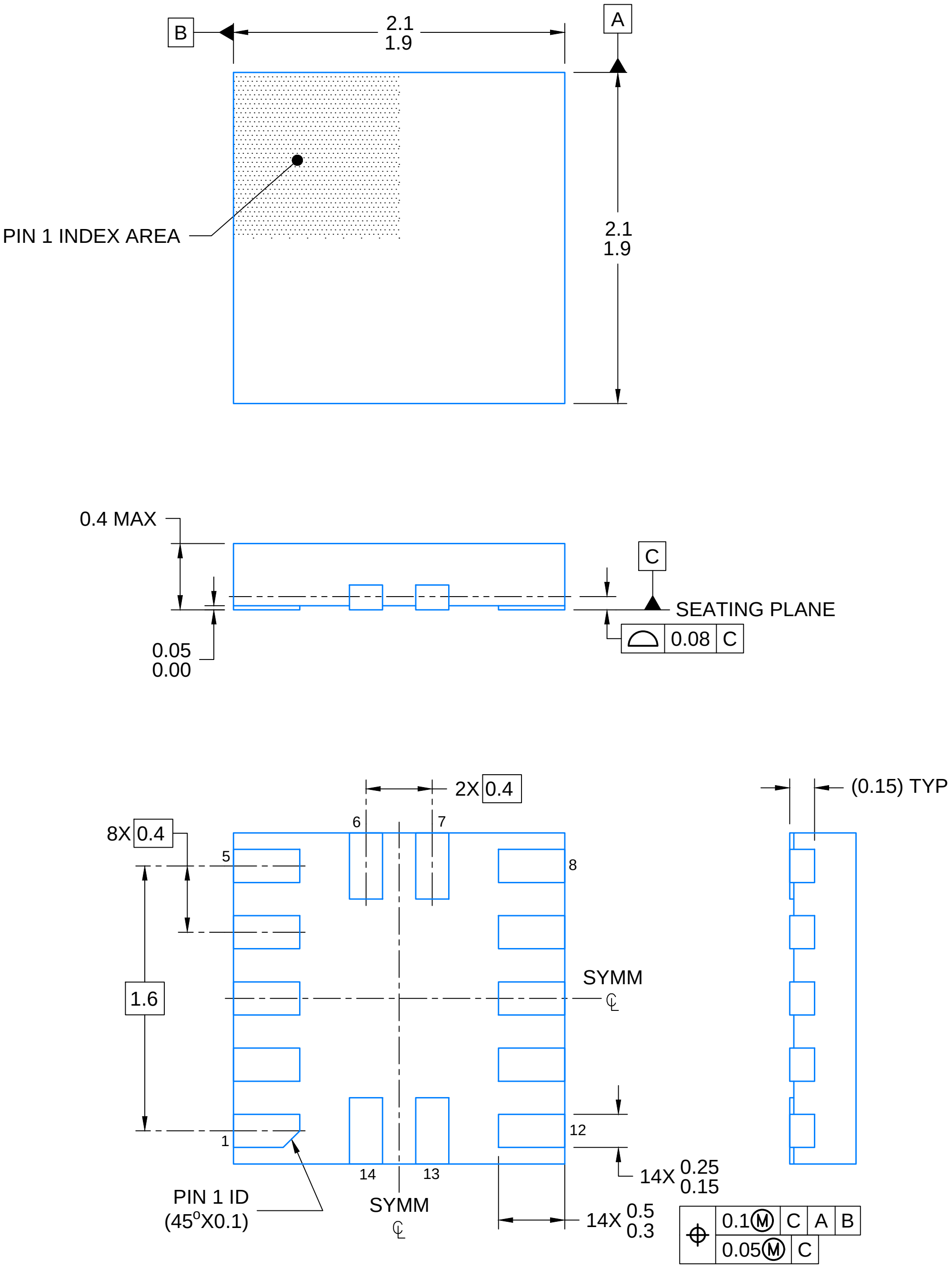
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



4220584/A 05/2019

NOTES:

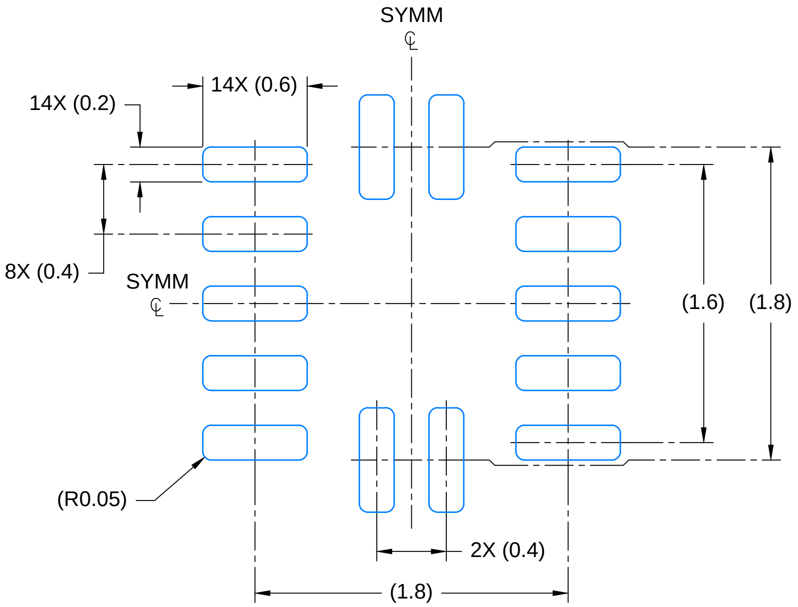
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

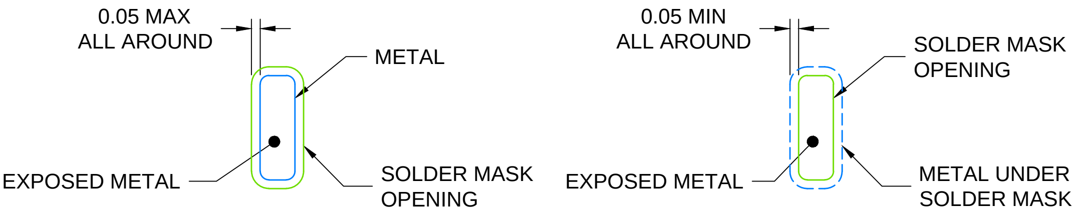
RUC0014A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X



NON-SOLDER MASK
DEFINED
(PREFERRED)

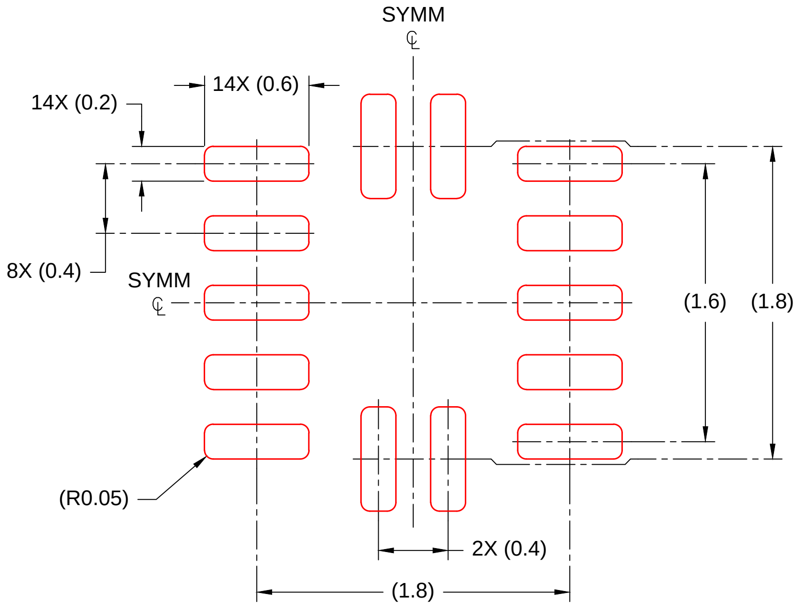
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

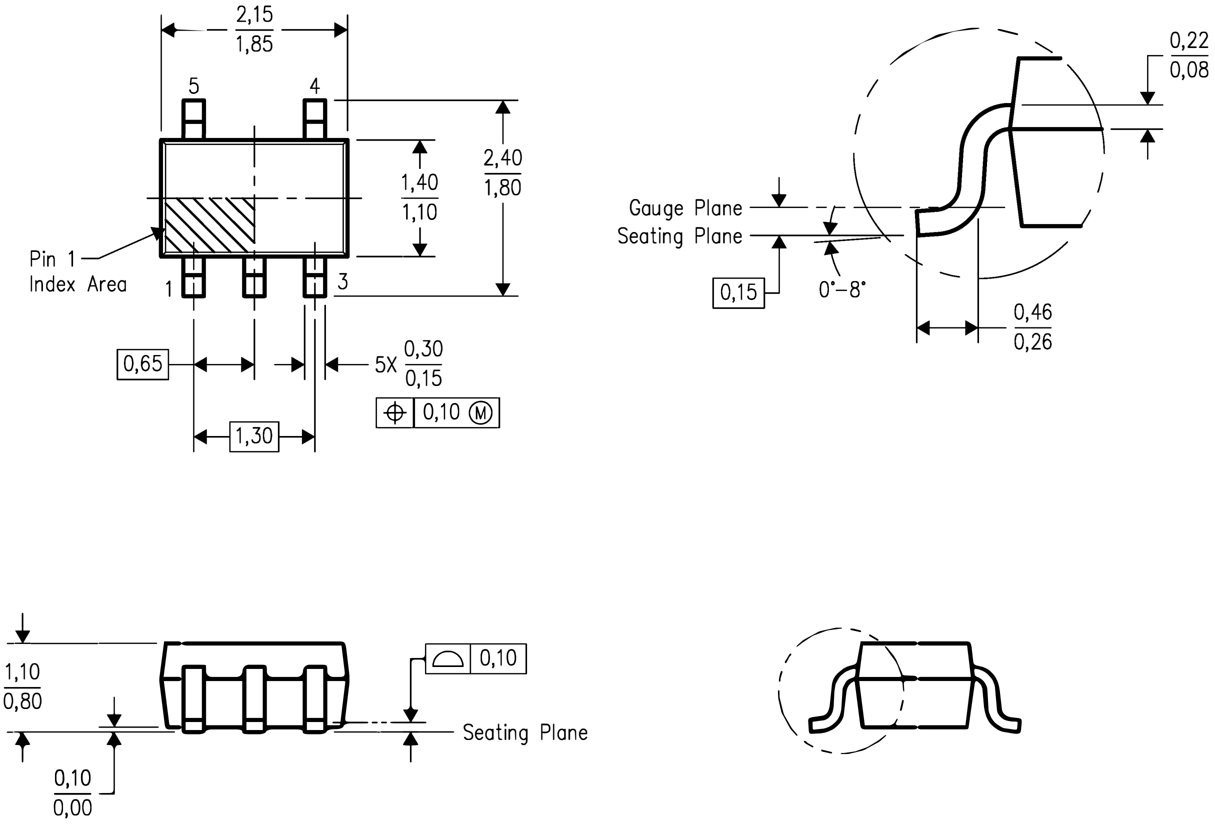


SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

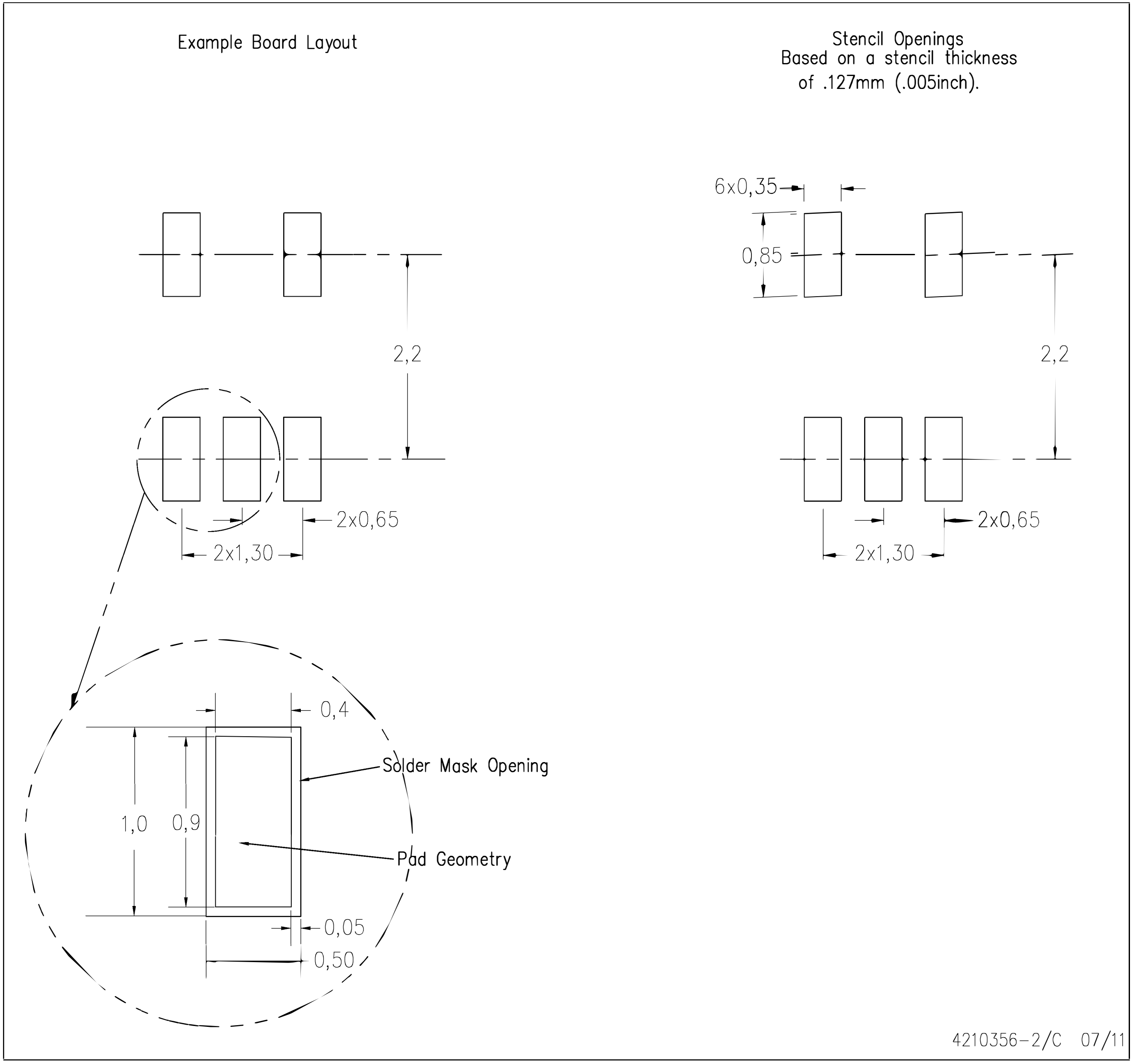
DCK (R-PDSO-G5) PLASTIC SMALL-OUTLINE PACKAGE



4093553-3/G 01/2007

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



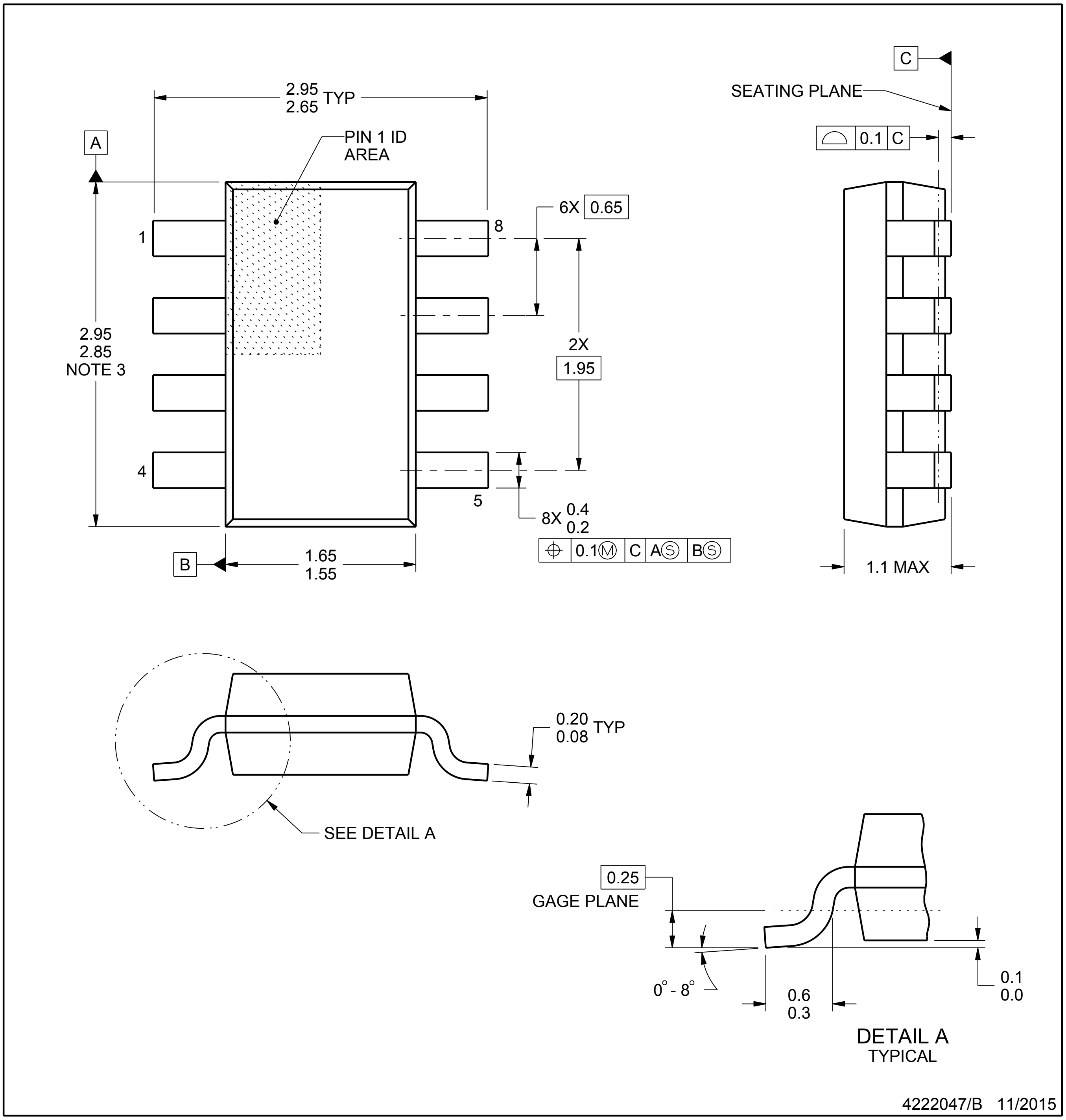
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PACKAGE OUTLINE

DDF0008A

SOT-23 - 1.1 mm max height

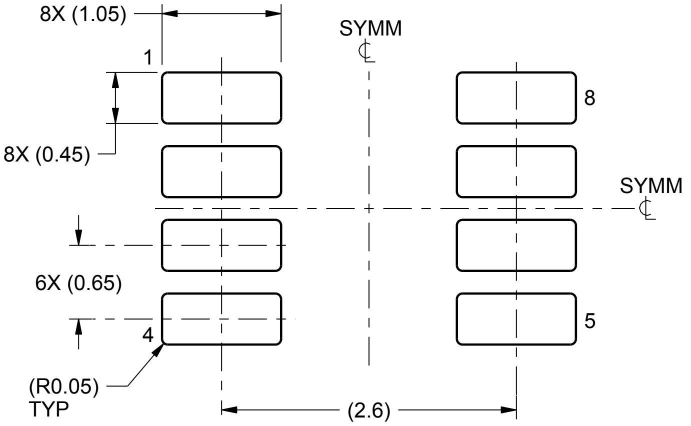
PLASTIC SMALL OUTLINE



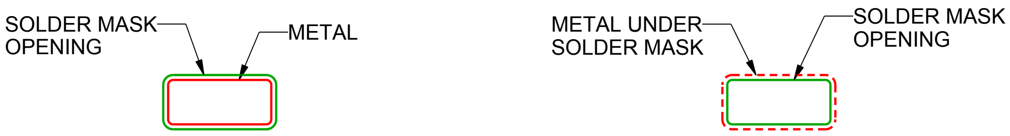
4222047/B 11/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



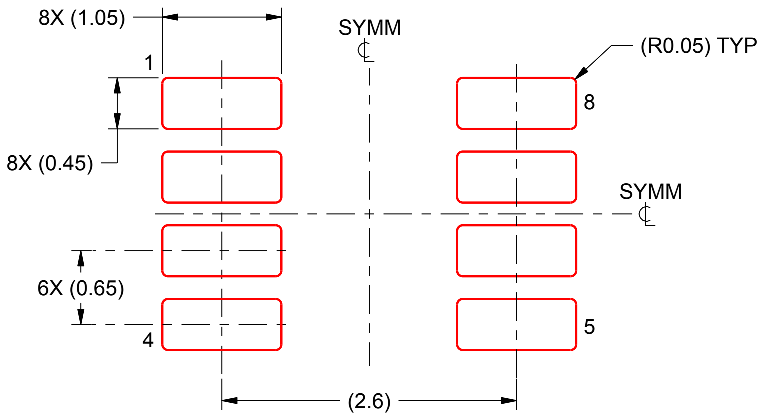
NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

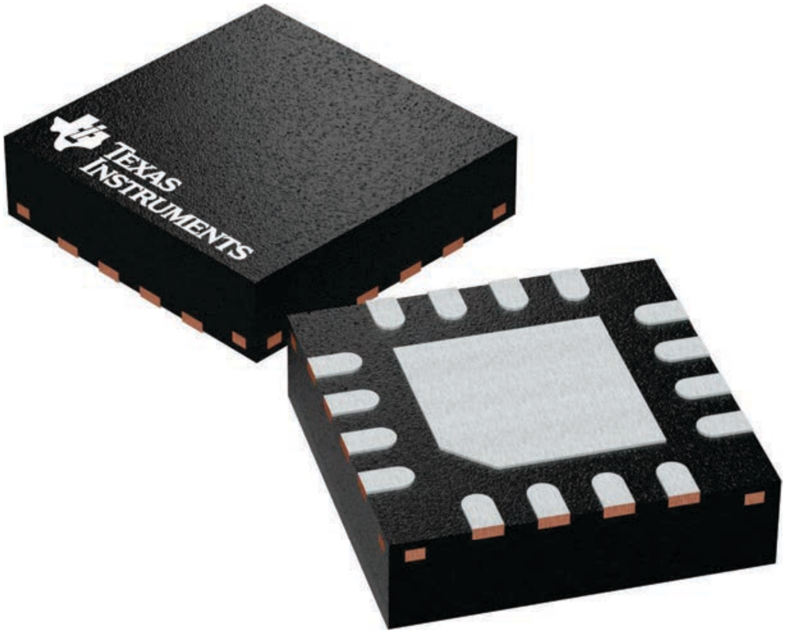
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

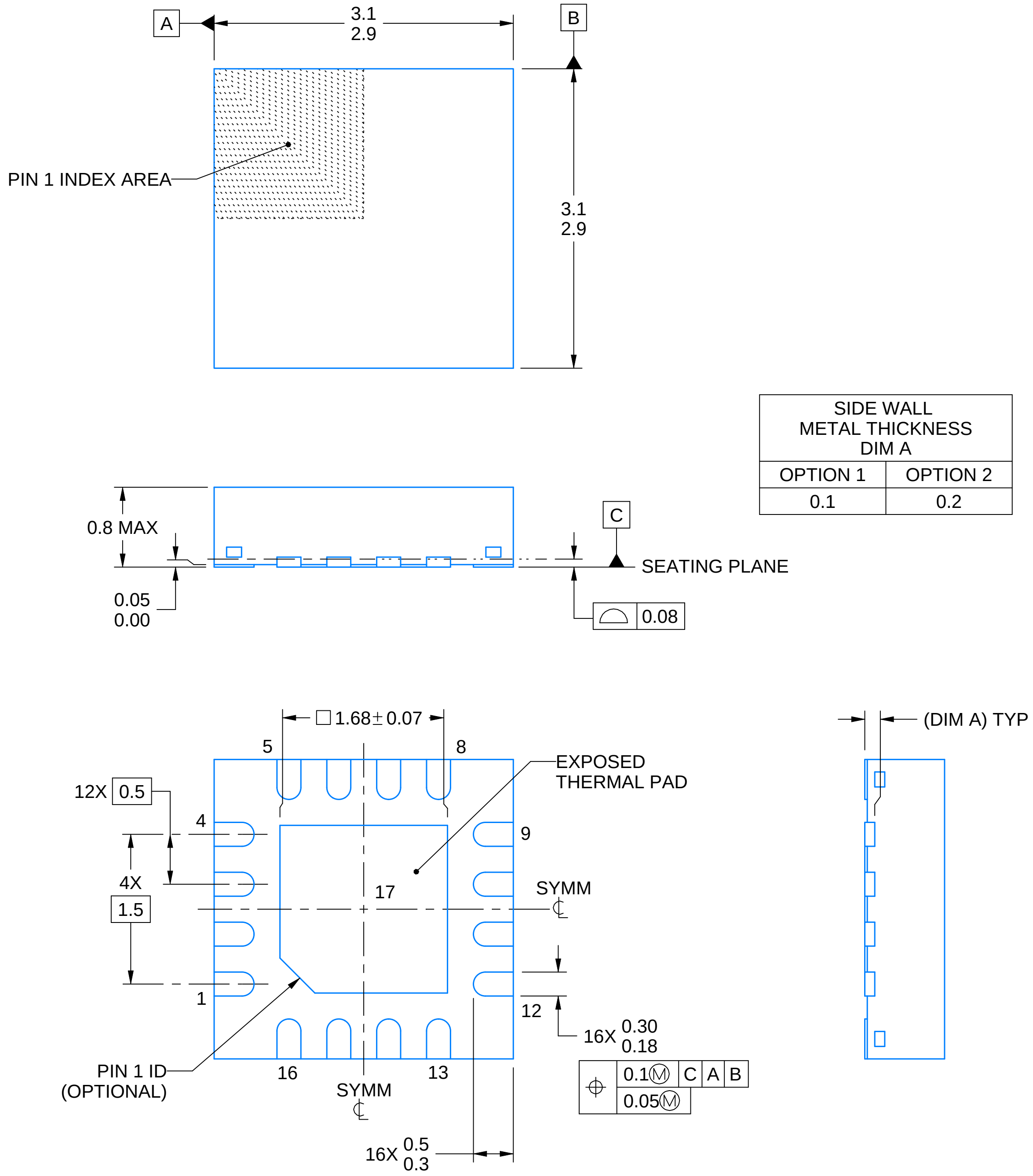


PACKAGE OUTLINE

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

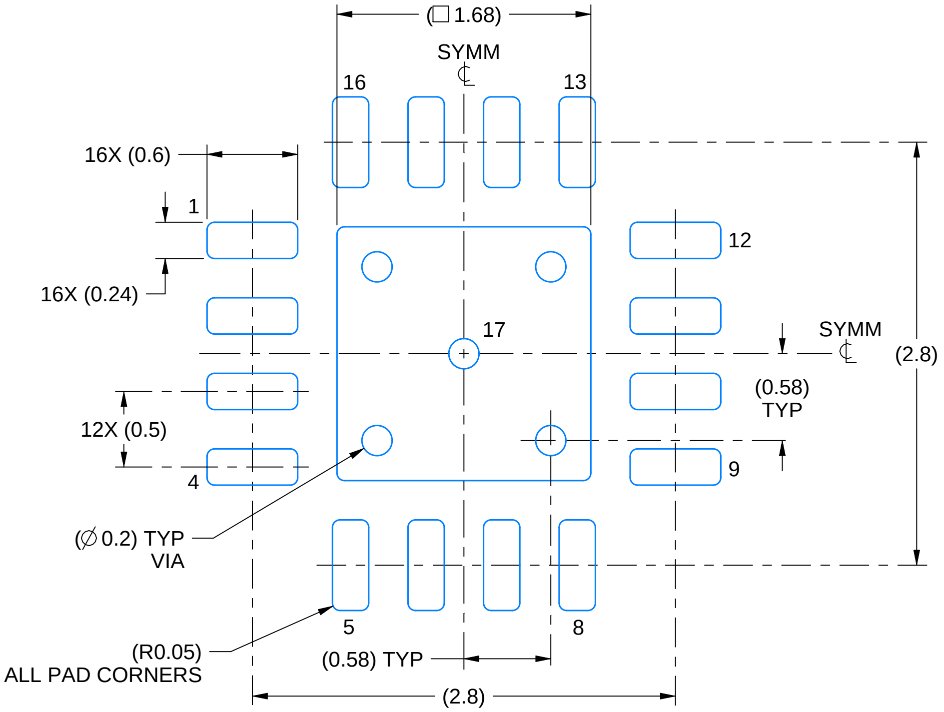
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

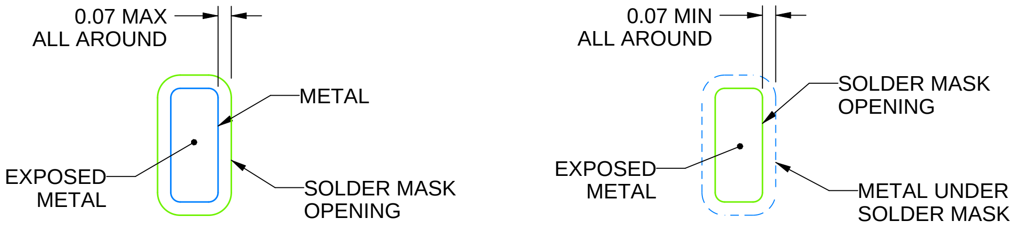
RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



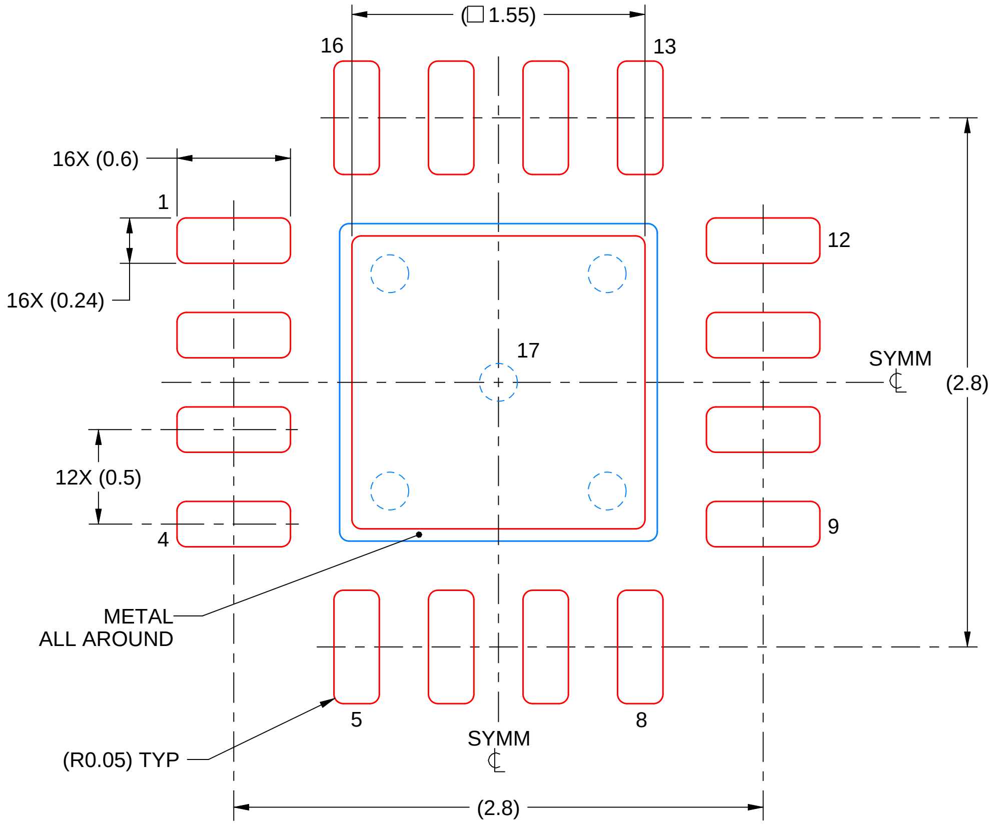
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.