

# TXB0101 1-Bit Bidirectional Level-Shifting and Voltage Translator With Auto Direction-Sensing and $\pm 15$ -kV ESD Protection

## 1 Features

- Available in the Texas Instruments NanoFree™ Package
- 1.2 V to 3.6 V on A Port and 1.65 V to 5.5 V on B Port ( $V_{CCA} \leq V_{CCB}$ )
- $V_{CC}$  Isolation Feature – If Either  $V_{CC}$  Input is at GND, All Outputs are in the High-Impedance State
- OE Input Circuit Referenced to  $V_{CCA}$
- Low Power Consumption, 5  $\mu$ A Maximum  $I_{CC}$
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - A Port
    - 2000 V Human Body Model (A114-B)
    - 250 V Machine Model (A115-A)
    - 1500 V Charged-Device Model (C101)
  - B Port
    - 15 kV Human Body Model (A114-B)
    - 250 V Machine Model (A115-A)
    - 1500 V Charged-Device Model (C101)

## 2 Applications

- Handsets
- Smartphones
- Tablets
- Desktop PCs

## 3 Description

This 1-bit noninverting translator uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.  $V_{CCA}$  should not exceed  $V_{CCB}$ .

When the output-enable (OE) input is low, all outputs are placed in the high-impedance state.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

To ensure the high-impedance state during power up or power down, OE should be tied to GND through a pulldown resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

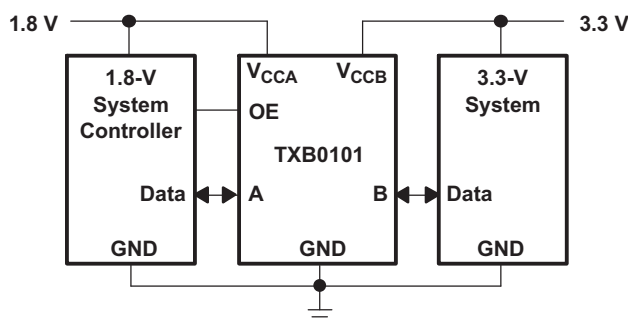
NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TXB0101DBV	SOT-23 (6)	2.90 mm x 1.60 mm
TXB0101DCK	SC70 (6)	2.00 mm x 1.25 mm
TXB0101DRL	SOT (6)	1.60 mm x 1.20 mm
TXB0101YZP	DSBGA (6)	1.1 mm x 1.20 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Typical Operating Circuit



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## 4 Revision History

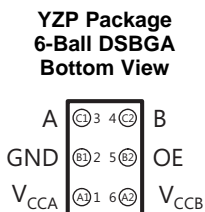
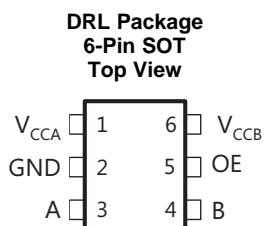
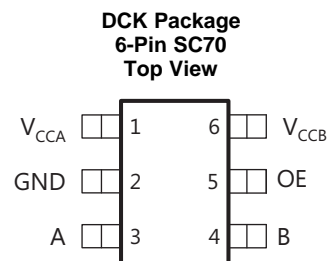
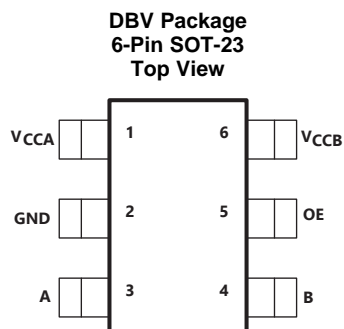
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (June 2015) to Revision D	Page
• Added Absolute maximum junction temperature, $T_J$ in <i>Absolute Maximum Ratings</i> .....	<b>4</b>
• Added TXB0101 Port A and Port B specifications in <i>ESD Ratings</i> table .....	<b>4</b>
• Added <i>Receiving Notification of Documentation Updates</i> section .....	<b>17</b>

Changes from Revision B (May 2012) to Revision C	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	<b>1</b>
• Removed <i>Ordering Information</i> table .....	<b>1</b>

Changes from Revision A (November 2008) to Revision B	Page
• Added notes to pin out graphics .....	<b>3</b>

## 5 Pin Configuration and Functions



- A. See mechanical drawings for dimensions.
- B. Pullup resistors are not required on both sides for Logic I/O.
- C. If pullup or pulldown resistors are needed, the resistor value must be over 50 kΩ.
- D. 50 kΩ is a safe recommended value, if the customer can accept higher Vol or lower Voh, smaller pullup or pulldown resistor is allowed, the draft estimation is  $V_{ol} = V_{ccout} \times 4.5 \text{ k} / (4.5 \text{ k} + R_{pu})$  and  $V_{oh} = V_{ccout} \times R_{dw} / (4.5 \text{ k} + R_{dw})$ .
- E. If pull up resistors are needed, please refer to the TXS0101 or contact TI.
- F. For detailed information, please refer to application note [SCEA043](#).

### Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	V <sub>CCA</sub>	—	A-port supply voltage. $1.2 \text{ V} \leq V_{CCA} \leq 3.6 \text{ V}$ and $V_{CCA} \leq V_{CCB}$
2	GND	—	Ground
3	A	I/O	Input/output A. Referenced to V <sub>CCA</sub> .
4	B	I/O	Input/output B. Referenced to V <sub>CCB</sub> .
5	OE	I	3-state output enable. Pull OE low to place all outputs in 3-state mode. Referenced to V <sub>CCA</sub> .
6	V <sub>CCB</sub>	—	B-port supply voltage. $1.65 \text{ V} \leq V_{CCB} \leq 5.5 \text{ V}$

## 6 Specification

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage		−0.5	4.6	V
V <sub>CCB</sub>	Supply voltage		−0.5	6.5	
V <sub>I</sub>	Input voltage <sup>(2)</sup>		−0.5	6.5	V
V <sub>O</sub>	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>		−0.5	6.5	V
V <sub>O</sub>	Voltage applied to any output in the high or low state <sup>(2) (3)</sup>	A port	−0.5	V <sub>CCA</sub> + 0.5	V
		B port	−0.5	V <sub>CCB</sub> + 0.5	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		−50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		−50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through V <sub>CCA</sub> , V <sub>CCB</sub> , or GND			±100	mA
T <sub>JMAX</sub>	Absolute maximum junction temperature			150	°C
T <sub>stg</sub>	Storage temperature		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative Voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V<sub>CCA</sub> and V<sub>CCB</sub> are provided in the recommended operating conditions table.

### 6.2 ESD Ratings

			VALUE	UNIT
TXB0101 Port A				
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	
TXB0101 Port B				
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±15	kV
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	V

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

See <sup>(1) (2)</sup>.

			V <sub>CCA</sub>	V <sub>CCB</sub>	MIN	MAX	UNIT
V <sub>CCA</sub>	Supply voltage				1.2	3.6	V
					1.65	5.5	
V <sub>IH</sub>	High-level input voltage	Data inputs	1.2 V to 3.6 V	1.65 V to 5.5 V	V <sub>CCI</sub> × 0.65 <sup>(3)</sup>	V <sub>CCI</sub>	V
		OE	1.2 V to 3.6 V	1.65 V to 5.5 V	V <sub>CCA</sub> × 0.65	5.5	
V <sub>IL</sub>	Low-level input voltage	Data inputs	1.2 V to 5.5 V	1.65 V to 5.5 V	0	V <sub>CCI</sub> × 0.35 <sup>(3)</sup>	V
		OE	1.2 V to 3.6 V	1.65 V to 5.5 V	0	V <sub>CCA</sub> × 0.35	
Δt/Δv	Input transition rise or fall rate	A-port inputs	1.2 V to 3.6 V	1.65 V to 5.5 V		40	ns/V
		B-port inputs	1.2 V to 3.6 V	1.65 V to 3.6 V		40	
				4.5 V to 5.5 V		30	
T <sub>A</sub>	Operating free-air temperature				−40	85	°C

(1) The A and B sides of an unused data I/O pair must be held in the same state, i.e., both at V<sub>CCI</sub> or both at GND.

(2) V<sub>CCA</sub> must be less than or equal to V<sub>CCB</sub> and must not exceed 3.6 V.

(3) V<sub>CCI</sub> is the supply voltage associated with the input port.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	TXB0101				UNIT
	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	YZP (DSBGA)	
	6 PINS	6 PINS	6 PINS	6 PINS	
$R_{\theta JA}$ Junction-to-ambient thermal resistance	192.3	266.9	204.2	105.8	°C/W
$R_{\theta JC(top)}$ Junction-to-case (top) thermal resistance	164.8	80.4	76.4	1.6	°C/W
$R_{\theta JB}$ Junction-to-board thermal resistance	38.6	99.1	38.7	10.8	°C/W
$\Psi_{JT}$ Junction-to-top characterization parameter	43.7	1.5	3.4	3.1	°C/W
$\Psi_{JB}$ Junction-to-board characterization parameter	38.1	98.3	38.5	10.8	°C/W
$R_{\theta JC(bot)}$ Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)<sup>(1)(2)</sup>

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25°C			−40°C to 85°C			UNIT	
					MIN	TYP	MAX	MIN	TYP	MAX		
V <sub>OHA</sub>		I <sub>OH</sub> = −20 μA	1.2 V		1.1			V <sub>CCA</sub> − 0.4			V	
			1.4 V to 3.6 V									
V <sub>OLA</sub>		I <sub>OL</sub> = 20 μA	1.2 V		0.9			0.4			V	
			1.4 V to 3.6 V									
V <sub>OHB</sub>		I <sub>OH</sub> = −20 μA		1.65 V to 5.5 V			V <sub>CCB</sub> − 0.4			V		
V <sub>OLB</sub>		I <sub>OL</sub> = 20 μA		1.65 V to 5.5 V			0.4			V		
I <sub>I</sub>	OE		1.2 V to 3.6 V	1.65 V to 5.5 V			±1			±2	μA	
I <sub>off</sub>	A port		0 V	0 V to 5.5 V			±1			±2	μA	
	B port		0 V to 3.6 V	0 V			±1			±2		
I <sub>OZ</sub>	A or B port	OE = GND	1.2 V to 3.6 V	1.65 V to 5.5 V			±1			±2	μA	
I <sub>CCA</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.2 V	1.65 V to 5.5 V			0.06				μA	
			1.4 V to 3.6 V	1.65 V to 5.5 V						3		
			3.6 V	0 V						2		
			0 V	5.5 V						−2		
I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCl</sub> or GND, I <sub>O</sub> = 0	1.2 V	1.65 V to 5.5 V			3.4				μA	
			1.4 V to 3.6 V	1.65 V to 5.5 V						5		
			3.6 V	0 V						−2		
			0 V	5.5 V						2		
I <sub>CCA</sub> + I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCl</sub> or GND, I <sub>O</sub> = 0	1.2 V	1.65 V to 5.5 V			3.5				μA	
			1.4 V to 3.6 V	1.65 V to 5.5 V						8		
I <sub>CCZA</sub>		V <sub>I</sub> = V <sub>CCl</sub> or GND, I <sub>O</sub> = 0, OE = GND	1.2 V	1.65 V to 5.5 V			0.05				μA	
			1.4 V to 3.6 V	1.65 V to 5.5 V						3		
I <sub>CCZB</sub>		V <sub>I</sub> = V <sub>CCl</sub> or GND, I <sub>O</sub> = 0, OE = GND	1.2 V	1.65 V to 5.5 V			3.3				μA	
			1.4 V to 3.6 V	1.65 V to 5.5 V						5		
C <sub>i</sub>	OE		1.2 V to 3.6 V	1.65 V to 5.5 V			2.5			3	pF	
C <sub>io</sub>	A port		1.2 V to 3.6 V	1.65 V to 5.5 V	5						6	pF
	B port				11			13				

(1)  $V_{CCl}$  is the supply voltage associated with the input port.

(2)  $V_{CCO}$  is the supply voltage associated with the output port.

**6.6 Timing Requirements,  $V_{CCA} = 1.2\text{ V}$**  $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 1.2\text{ V}$ 

			$V_{CCB} = 1.8\text{ V}$	$V_{CCB} = 2.5\text{ V}$	$V_{CCB} = 3.3\text{ V}$	$V_{CCB} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
Data rate			20	20	20	20	Mbps
$t_w$	Pulse duration	Data inputs	50	50	50	50	ns

**6.7 Timing Requirements,  $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$** over recommended operating free-air temperature range,  $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$  (unless otherwise noted)

			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate			40		40		40		40		Mbps
$t_w$	Pulse duration	Data inputs	25		25		25		25		ns

**6.8 Timing Requirements,  $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$** over recommended operating free-air temperature range,  $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$  (unless otherwise noted)

			$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data rate			60		60		60		60		Mbps
$t_w$	Pulse duration	Data inputs	17		17		17		17		ns

**6.9 Timing Requirements,  $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$** over recommended operating free-air temperature range,  $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted)

			$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Data rate			100		100		100		Mbps
$t_w$	Pulse duration	Data inputs	10		10		10		ns

**6.10 Timing Requirements,  $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$** over recommended operating free-air temperature range,  $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted)

			$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
Data rate			100		100		Mbps
$t_w$	Pulse duration	Data inputs	10		10		ns

## 6.11 Switching Characteristics, $V_{CCA} = 1.2\text{ V}$

$T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 1.2\text{ V}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V}$	$V_{CCB} = 2.5\text{ V}$	$V_{CCB} = 3.3\text{ V}$	$V_{CCB} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
$t_{pd}$	A	B	6.9	5.7	5.3	5.5	ns
	B	A	7.4	6.4	6	5.8	
$t_{en}$	OE	A	1	1	1	1	$\mu\text{s}$
		B	1	1	1	1	
$t_{dis}$	OE	A	18	15	14	14	ns
		B	20	17	16	16	
$t_{rA}, t_{fA}$	A-port rise and fall times		4.2	4.2	4.2	4.2	ns
$t_{rB}, t_{fB}$	B-port rise and fall times		2.1	1.5	1.2	1.1	ns
Max data rate			20	20	20	20	Mbps

## 6.12 Switching Characteristics, $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1.4	12.9	1.2	10.1	1.1	10	0.8	9.9	ns
	B	A	0.9	14.2	0.7	12	0.4	11.7	0.3	13.7	
$t_{en}$	OE	A		1		1		1		1	$\mu\text{s}$
		B		1		1		1		1	
$t_{dis}$	OE	A	5.9	31	5.7	25.9	5.6	23	5.7	22.4	ns
		B	5.4	30.3	4.9	22.8	4.8	20	4.9	19.5	
$t_{rA}, t_{fA}$	A-port rise and fall times		1.4	5.1	1.4	5.1	1.4	5.1	1.4	5.1	ns
$t_{rB}, t_{fB}$	B-port rise and fall times		0.9	4.5	0.6	3.2	0.5	2.8	0.4	2.7	ns
Max data rate			40		40		40		40		Mbps

## 6.13 Switching Characteristics, $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1.6	11	1.4	7.7	1.3	6.8	1.2	6.5	ns
	B	A	1.5	12	1.3	8.4	1	7.6	0.9	7.1	
$t_{en}$	OE	A		1		1		1		1	$\mu\text{s}$
		B		1		1		1		1	
$t_{dis}$	OE	A	5.9	31	5.1	21.3	5	19.3	5	17.4	ns
		B	5.4	30.3	4.4	20.8	4.2	17.9	4.3	16.3	
$t_{rA}, t_{fA}$	A-port rise and fall times		1	4.2	1.1	4.1	1.1	4.1	1.1	4.1	ns
$t_{rB}, t_{fB}$	B-port rise and fall times		0.9	4.5	0.6	3.2	0.5	2.8	0.4	2.7	ns
Max data rate			60		60		60		60		Mbps

## 6.14 Switching Characteristics, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	1.1	6.3	1	5.2	0.9	4.7	ns
	B	A	1.2	6.6	1.1	5.1	0.9	4.4	
$t_{en}$	OE	A		1		1		1	$\mu\text{s}$
		B		1		1		1	
$t_{dis}$	OE	A	5.1	21.3	4.6	15.2	4.6	13.2	ns
		B	4.4	20.8	3.8	16	3.9	13.9	
$t_{rA}, t_{fA}$	A-port rise and fall times		0.8	3	0.8	3	0.8	3	ns
$t_{rB}, t_{fB}$	B-port rise and fall times		0.7	3	0.5	2.8	0.4	2.7	ns
Max data rate			100		100		100		Mbps

## 6.15 Switching Characteristics, $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V} \pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}$	A	B	0.9	4.7	0.8	4	ns
	B	A	1	4.9	0.9	4.5	
$t_{en}$	OE	A		1		1	$\mu\text{s}$
		B		1		1	
$t_{dis}$	OE	A	4.6	15.2	4.3	12.1	ns
		B	3.8	16	3.4	13.2	
$t_{rA}, t_{fA}$	A-port rise and fall times		0.7	2.5	0.7	2.5	ns
$t_{rB}, t_{fB}$	B-port rise and fall times		0.5	2.3	0.4	2.7	ns
Max data rate			100		100		Mbps

## 6.16 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	V <sub>CCA</sub>							UNIT
			1.2 V	1.2 V	1.5 V	1.8 V	2.5 V	2.5 V	3.3 V	
			V <sub>CCB</sub>							
			5 V	1.8 V	1.8 V	1.8 V	2.5 V	5 V	3.3 V to 5 V	
			TYP	TYP	TYP	TYP	TYP	TYP	TYP	
C <sub>pdA</sub>	A-port input, B-port output	C <sub>L</sub> = 0, f = 10 MHz, t <sub>r</sub> = t <sub>f</sub> = 1 ns, OE = V <sub>CCA</sub> (outputs enabled)	7.8	8	8	7	7	8	8	pF
	B-port input, A-port output		12	11	11	11	11	11	11	
C <sub>pdB</sub>	A-port input, B-port output		38.1	28	29	29	29	29	30	
	B-port input, A-port output		25.4	18	17	17	18	20	21	
C <sub>pdA</sub>	A-port input, B-port output	C <sub>L</sub> = 0, f = 10 MHz, t <sub>r</sub> = t <sub>f</sub> = 1 ns, OE = GND (outputs disabled)	0.01	0.01	0.01	0.01	0.01	0.01	0.01	pF
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.01	
C <sub>pdB</sub>	A-port input, B-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.02	
	B-port input, A-port output		0.01	0.01	0.01	0.01	0.01	0.01	0.03	



## 6.17 Typical Characteristics

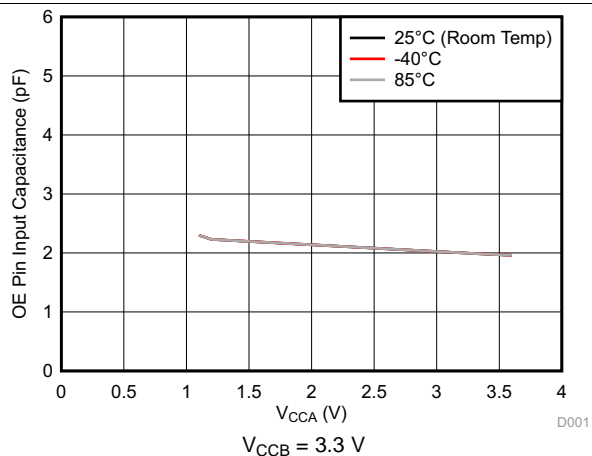


Figure 1. Input Capacitance for OE pin ( $C_i$ ) vs Power Supply ( $V_{CCA}$ )

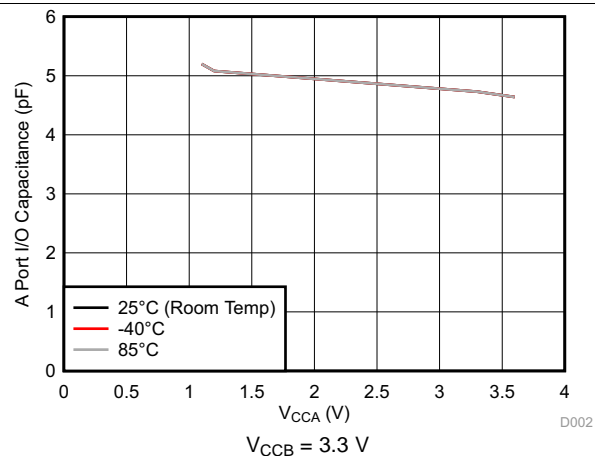


Figure 2. Capacitance for A Port I/O Pins ( $C_{IO}$ ) vs Power Supply ( $V_{CCA}$ )

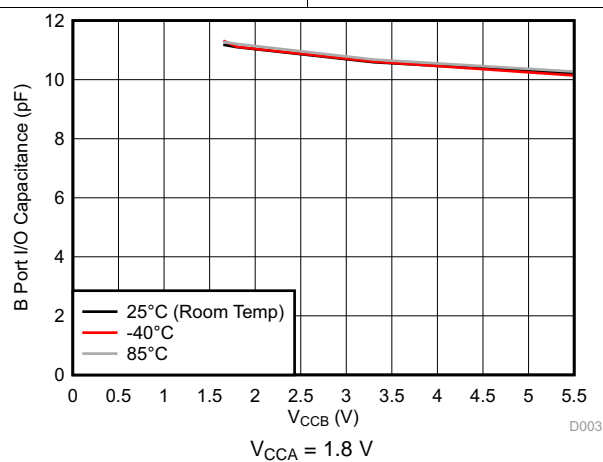
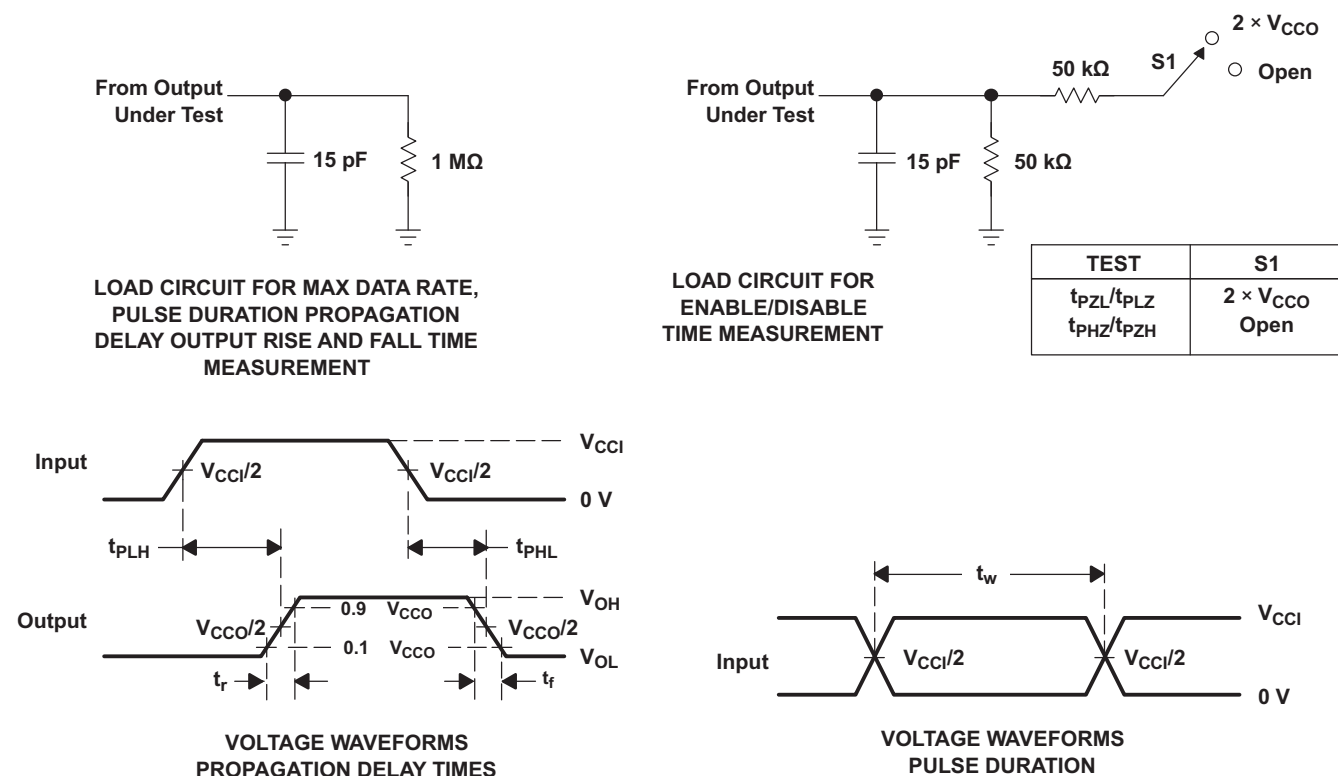


Figure 3. Capacitance for B Port I/O Pins ( $C_{IO}$ ) vs Power Supply ( $V_{CCB}$ )

## 7 Parameter Measurement Information



- A. C<sub>L</sub> includes probe and jig capacitance.
- B. All input pulses are supplied by generators having the following characteristics: PRR = 10 MHz, Z<sub>O</sub> = 50 Ω, dv/dt ≥ 1 V/ns.
- C. The outputs are measured one at a time, with one transition per measurement.
- D. t<sub>PLH</sub> and t<sub>PHL</sub> are the same as t<sub>pd</sub>.
- E. V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.
- F. V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.
- G. All parameters and waveforms are not applicable to all devices.

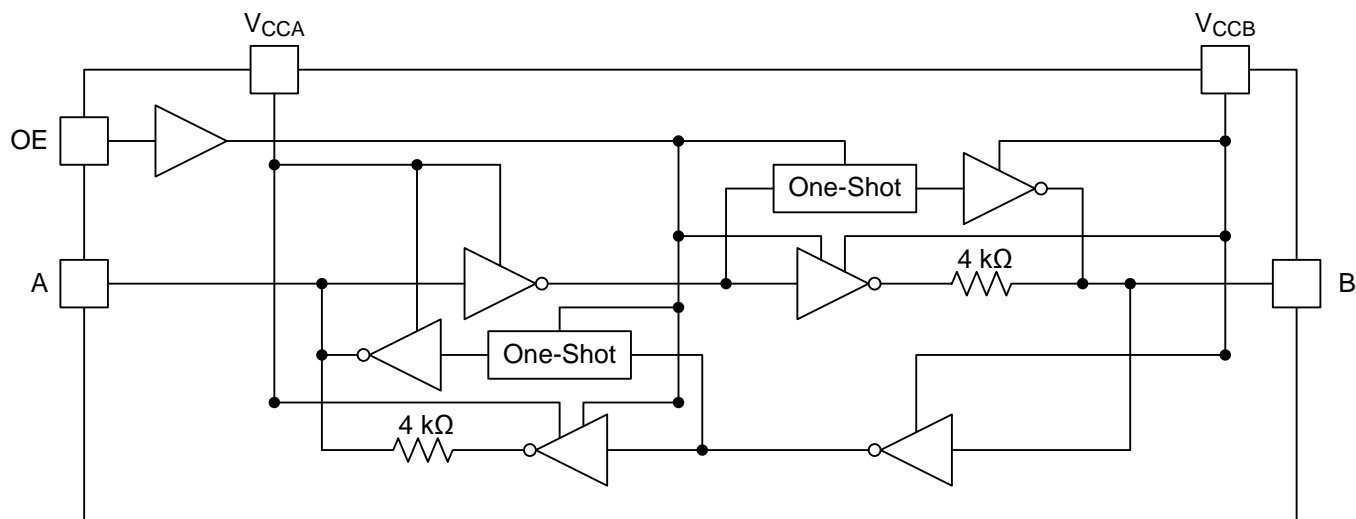
**Figure 4. Load Circuits and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The TXB0101 device is a 1-bit directionless level-shifting and voltage translator specifically designed for translating logic voltage levels. The A port accepts I/O voltages ranging from 1.2 V to 3.6 V, while the B port is able to accept I/O voltages from 1.65 V to 5.5 V. The device is a buffered architecture with edge rate accelerators (one-shots) to improve the overall data rate. This device can only translate push-pull CMOS logic outputs. If for open-drain signal translation, see TI [TXS010X](#) products.

### 8.2 Functional Block Diagram

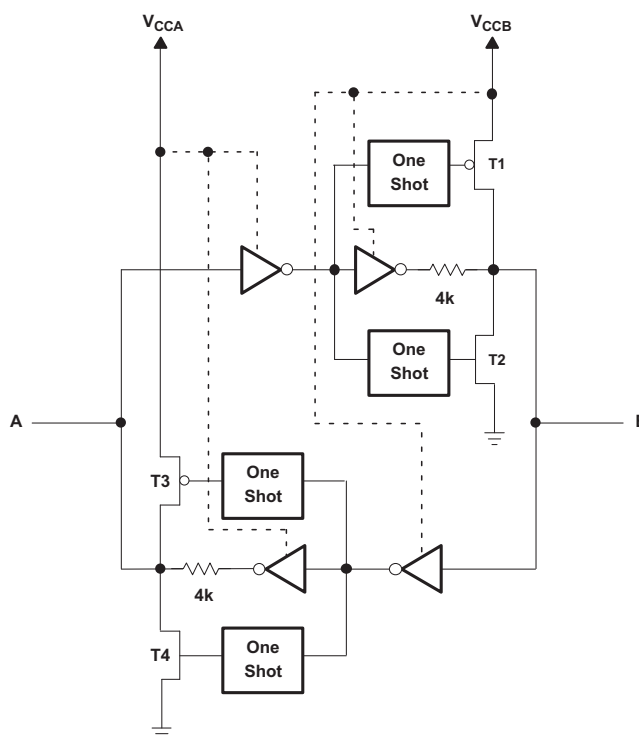


### 8.3 Feature Description

#### 8.3.1 Architecture

The TXB0101 architecture (see [Figure 5](#)) does not require a direction-control signal to control the direction of data flow from A to B or from B to A. In a DC state, the output drivers of the TXB0101 can maintain a high or low, but are designed to be weak, so that they can be overdriven by an external driver when data on the bus starts flowing the opposite direction.

The output one-shots detect rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (T1, T3) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (T2, T4) for a short duration, which speeds up the high-to-low transition. The typical output impedance during output transition is 70  $\Omega$  at  $V_{CCO} = 1.2$  V to 1.8 V, 50  $\Omega$  at  $V_{CCO} = 1.8$  V to 3.3 V, and 40  $\Omega$  at  $V_{CCO} = 3.3$  V to 5 V.



The TXB0101 device has two functional modes, enabled and disabled. To disable the device set the OE input low, which places all I/Os in a high-impedance state. Setting the OE input high will enable the device.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TXB0101 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. It can only translate push-pull CMOS logic outputs. If for open-drain signal translation, see TI [TXS010X](#) products. Any external pulldown or pullup resistors are recommended larger than 50 k $\Omega$ .

### 9.2 Typical Application

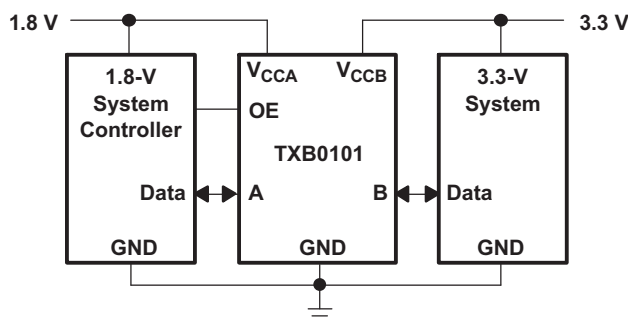


Figure 6. Typical Application Circuit

#### 9.2.1 Design Requirements

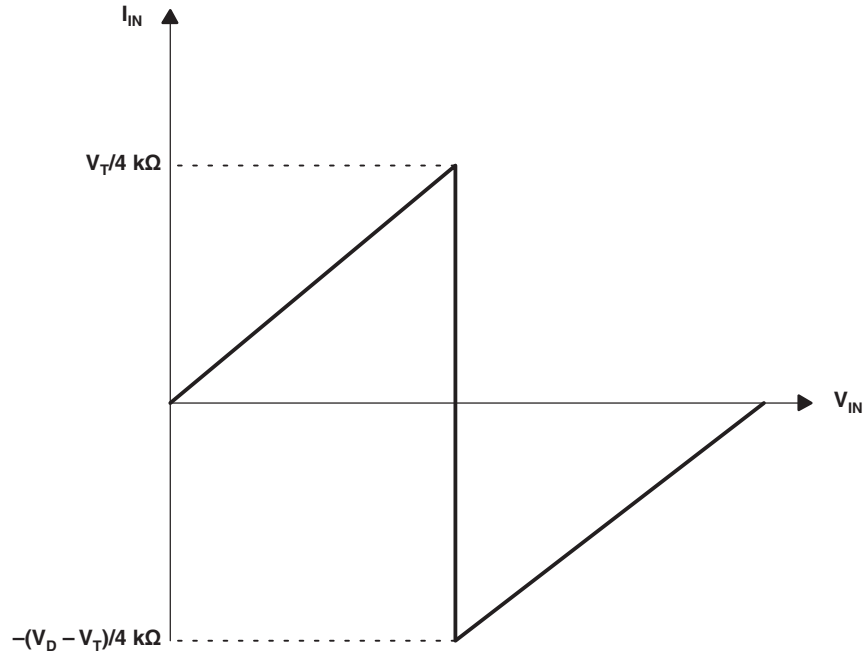
For this design example, use the parameters listed in [Table 1](#). And make sure that  $V_{CCA} \leq V_{CCB}$ .

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2 V to 3.6 V
Output voltage range	1.65 V to 5.5 V

### 9.2.1.1 Input Driver Requirements

Typical  $I_{IN}$  vs  $V_{IN}$  characteristics of the TXB0101 are shown in Figure 7. For proper operation, the device driving the data I/Os of the TXB0101 must have drive strength of at least  $\pm 2$  mA.



- A.  $V_T$  is the input threshold voltage of the TXB0101 (typically  $V_{CC}/2$ ).  
 B.  $V_D$  is the supply voltage of the external driver.

Figure 7. Typical  $I_{IN}$  vs  $V_{IN}$  Curve

### 9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the TXB0101 device to determine the input voltage range. For a valid logic HIGH the value must exceed the  $V_{IH}$  of the input port. For a valid logic LOW the value must be less than the  $V_{IL}$  of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXB0101 device is driving to determine the output voltage range.
  - External pullup or pulldown resistors are not recommended. If mandatory, TI recommends the value should be larger than 50 kΩ.
- An external pulldown or pullup resistor decreases the output  $V_{OH}$  and  $V_{OL}$ . Use Equation 1 and Equation 2 to draft estimate the  $V_{OH}$  and  $V_{OL}$  as a result of an external pulldown and pullup resistor.

$$V_{OH} = V_{CCX} \times R_{PD} / (R_{PD} + 4.5 \text{ k}\Omega) \quad (1)$$

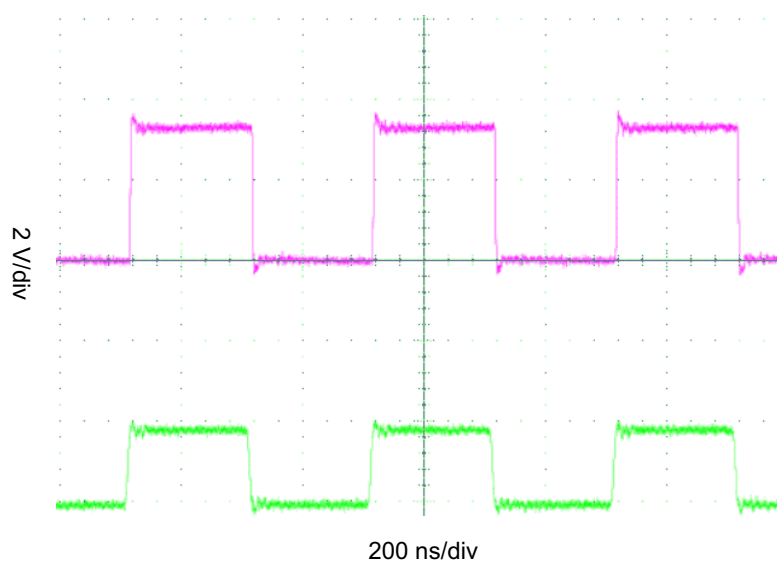
$$V_{OL} = V_{CCX} \times 4.5 \text{ k}\Omega / (R_{PU} + 4.5 \text{ k}\Omega)$$

where

- $V_{CCX}$  is the output port supply voltage on either  $V_{CCA}$  or  $V_{CCB}$
- $R_{PD}$  is the value of the external pulldown resistor
- $R_{PU}$  is the value of the external pullup resistor
- 4.5 kΩ is the counting the variation of the serial resistor 4 kΩ in the I/O line.

(2)

### 9.2.3 Application Curve



$V_{CCA} = 1.8 \text{ V}$  (waveform captured at pin 3)

$V_{CCB} = 3.3 \text{ V}$  (Waveform captured at pin 4)

**Figure 8. Level-Translation of a 2.5-MHz Signal**

## 10 Power Supply Recommendations

During operation, ensure that  $V_{CCA} \leq V_{CCB}$  at all times. During power up sequencing,  $V_{CCA} \geq V_{CCB}$  does not damage the device, so any power supply can be ramped up first. The TXB0101 has circuitry that disables all output ports when either  $V_{CC}$  is switched off ( $V_{CCA/B} = 0$  V). The output-enable (OE) input circuit is designed so that it is supplied by  $V_{CCA}$  and when the (OE) input is low, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the OE input pin must be tied to GND through a pulldown resistor and must not be enabled until  $V_{CCA}$  and  $V_{CCB}$  are fully ramped and stable. The minimum value of the pulldown resistor to ground is determined by the current-sourcing capability of the driver

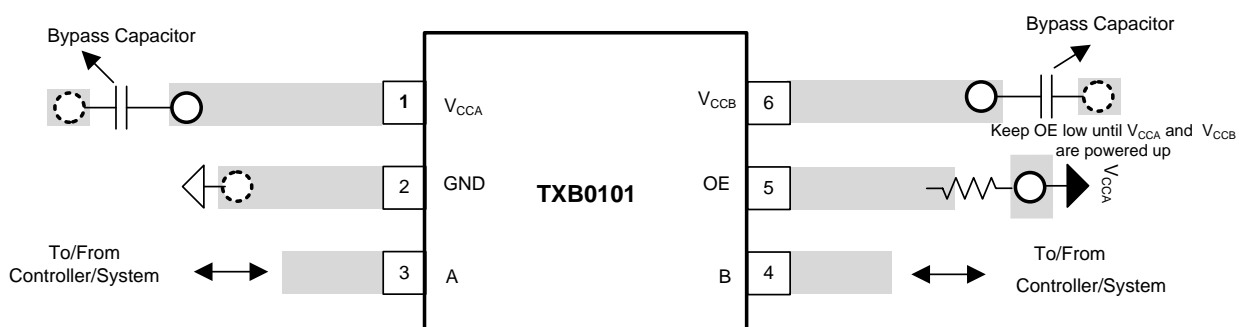
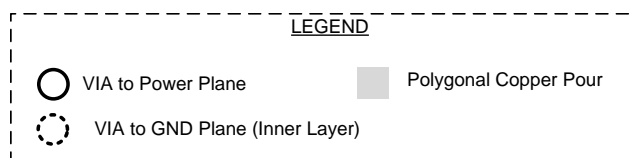
## 11 Layout

### 11.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. And should be placed as close as possible to the  $V_{CCA}$ ,  $V_{CCB}$  pin and GND pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 10 ns, ensuring that any reflection encounters low impedance at the source driver.

### 11.2 Layout Example



**Figure 9. Layout Example Recommendation**



## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXB0101DBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFCF, NFCR)	<a href="#">Samples</a>
TXB0101DBVT	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFCF, NFCR)	<a href="#">Samples</a>
TXB0101DBVTG4	ACTIVE	SOT-23	DBV	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(NFCF, NFCR)	<a href="#">Samples</a>
TXB0101DCKR	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27O	<a href="#">Samples</a>
TXB0101DCKRG4	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27O	<a href="#">Samples</a>
TXB0101DCKT	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		27O	<a href="#">Samples</a>
TXB0101DCKTG4	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	27O	<a href="#">Samples</a>
TXB0101DRLR	ACTIVE	SOT-5X3	DRL	6	4000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	27R	<a href="#">Samples</a>
TXB0101DRLT	ACTIVE	SOT-5X3	DRL	6	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	27R	<a href="#">Samples</a>
TXB0101YZPR	ACTIVE	DSBGA	YZP	6	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	27N	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

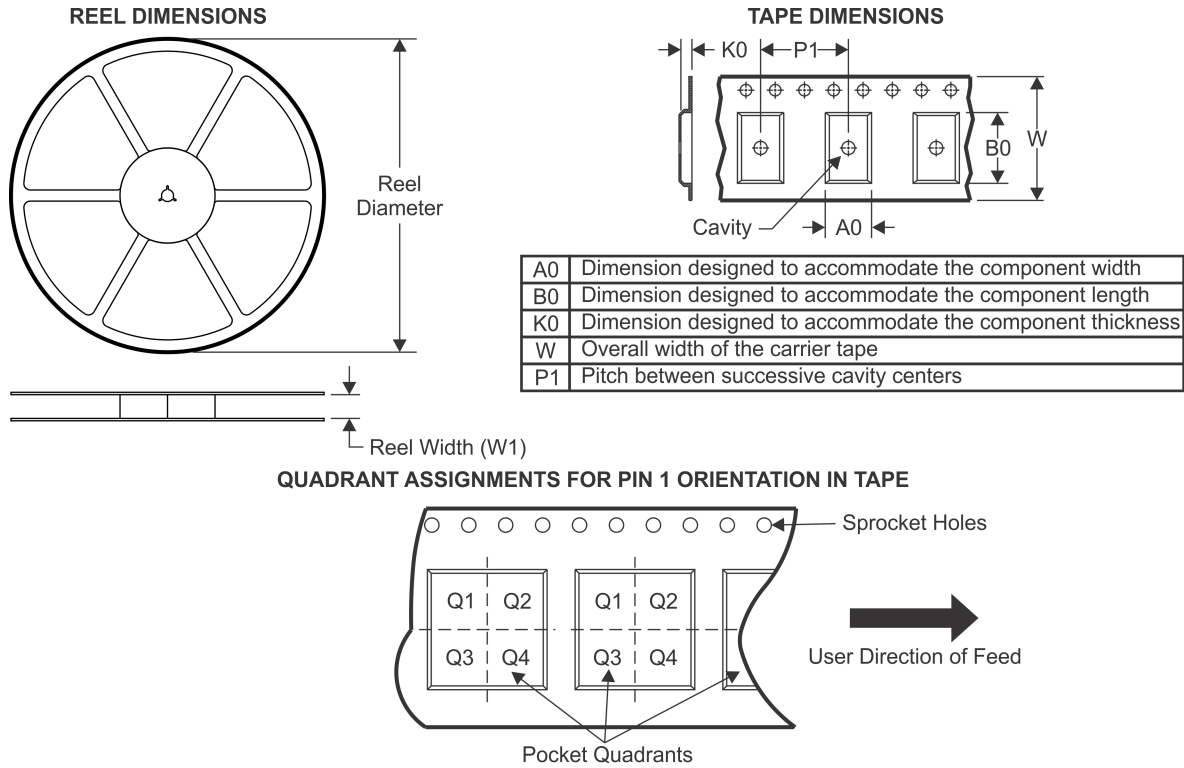
<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



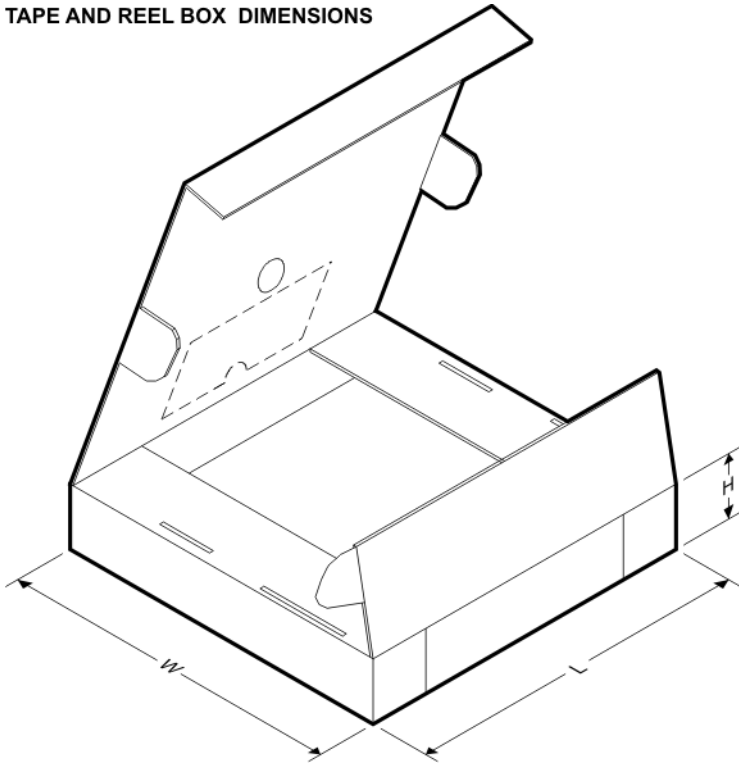
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXB0101DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TXB0101DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
TXB0101DCKR	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TXB0101DCKT	SC70	DCK	6	250	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
TXB0101DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TXB0101DRLT	SOT-5X3	DRL	6	250	180.0	8.4	1.98	1.78	0.69	4.0	8.0	Q3
TXB0101YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

# PACKAGE MATERIALS INFORMATION

5-Jan-2021

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXB0101DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
TXB0101DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
TXB0101DCKR	SC70	DCK	6	3000	200.0	183.0	25.0
TXB0101DCKT	SC70	DCK	6	250	203.0	203.0	35.0
TXB0101DRLR	SOT-5X3	DRL	6	4000	202.0	201.0	28.0
TXB0101DRLT	SOT-5X3	DRL	6	250	202.0	201.0	28.0
TXB0101YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

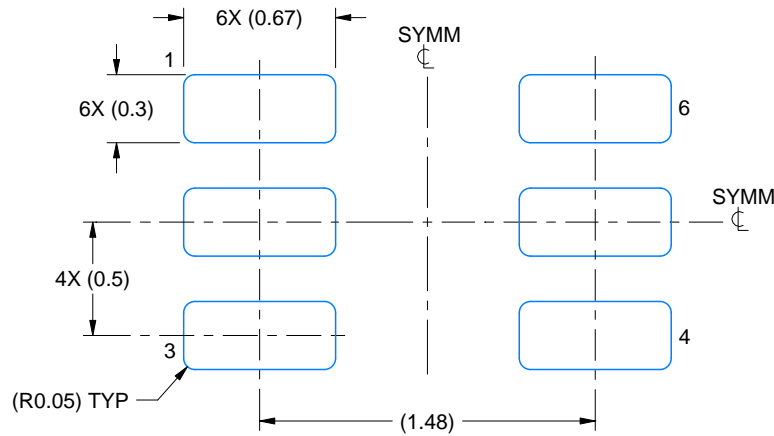
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

# EXAMPLE BOARD LAYOUT

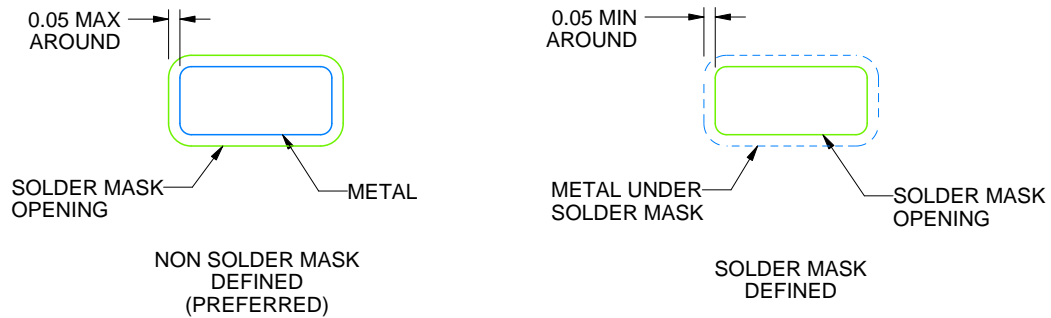
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4223266/B 12/2020

NOTES: (continued)

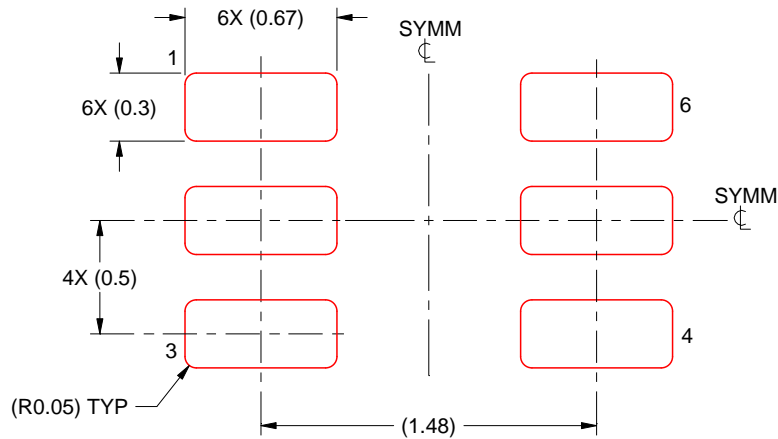
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4223266/B 12/2020

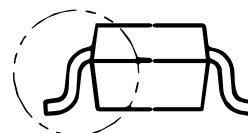
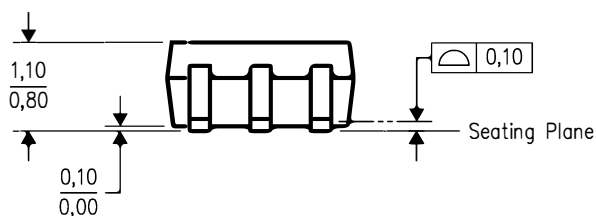
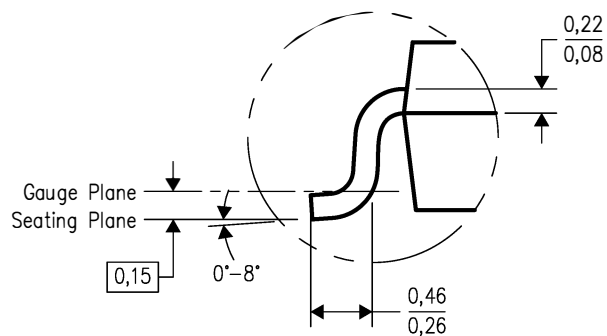
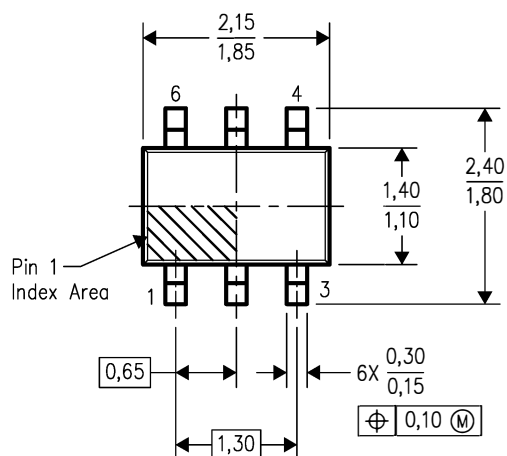
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



DCK (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

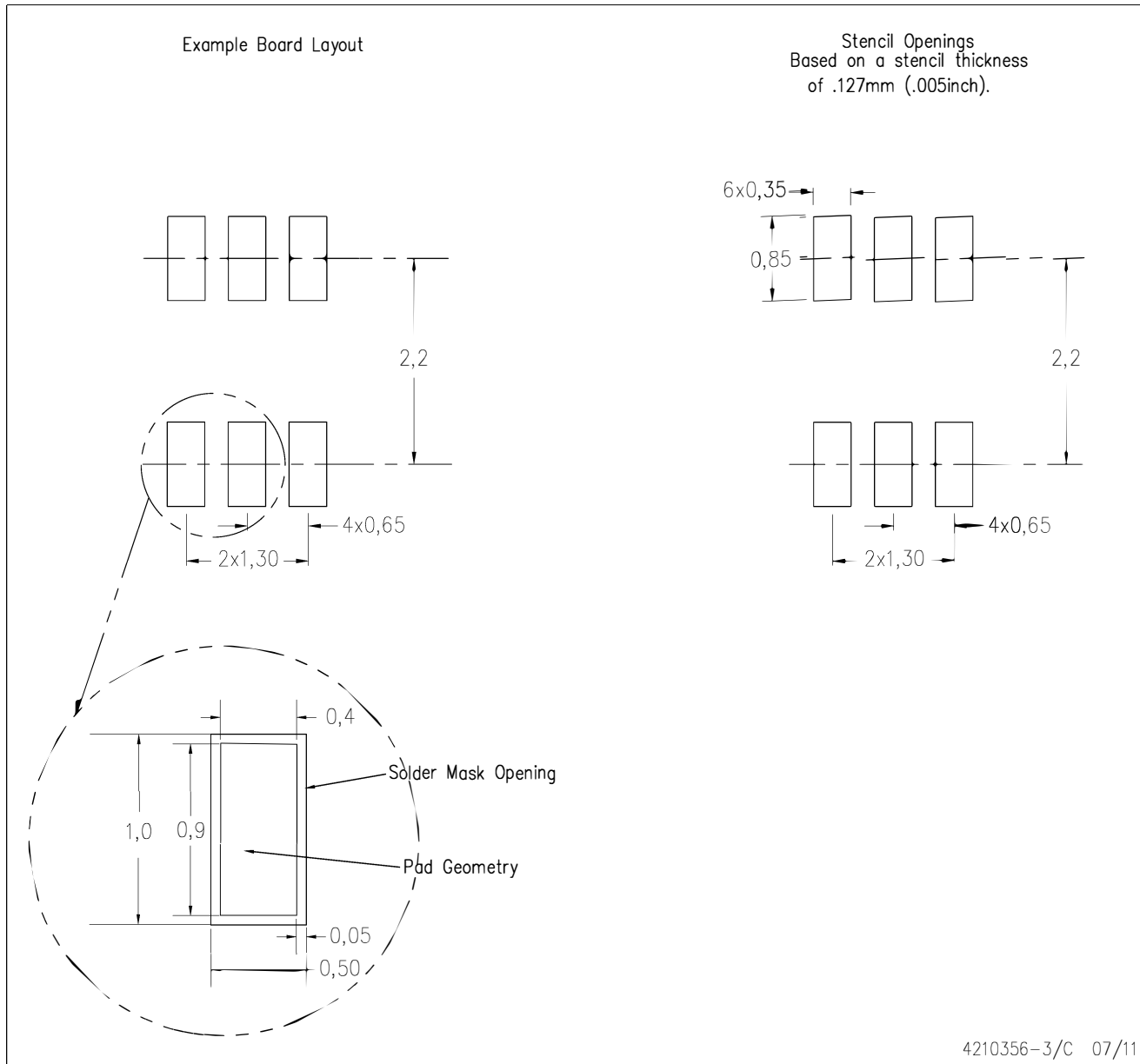


4093553-4/G 01/2007

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - Falls within JEDEC MO-203 variation AB.

DCK (R-PDSO-G6)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - D. Publication IPC-7351 is recommended for alternate designs.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.



## SOT-23 - 1.45 mm max height

## SMALL OUTLINE TRANSISTOR



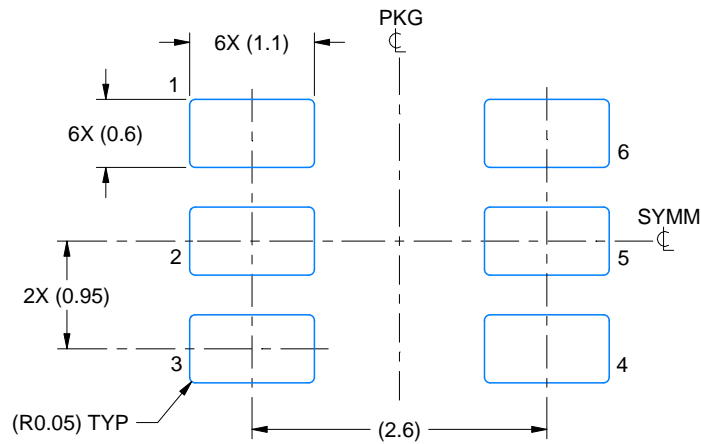
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

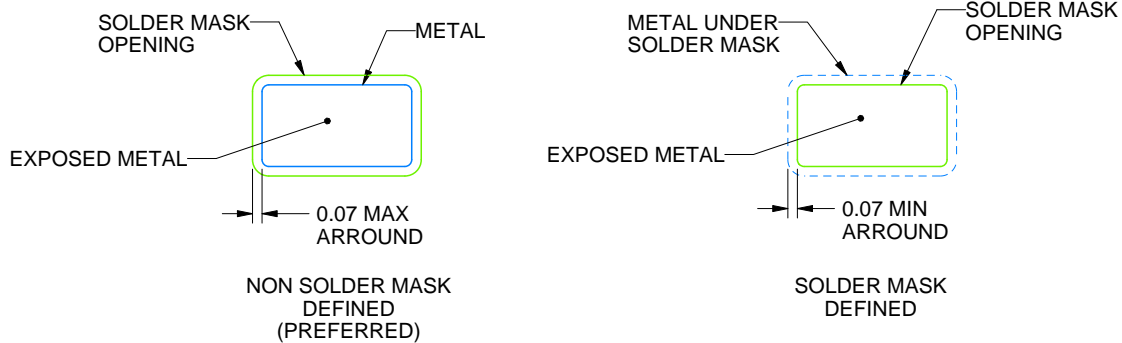
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

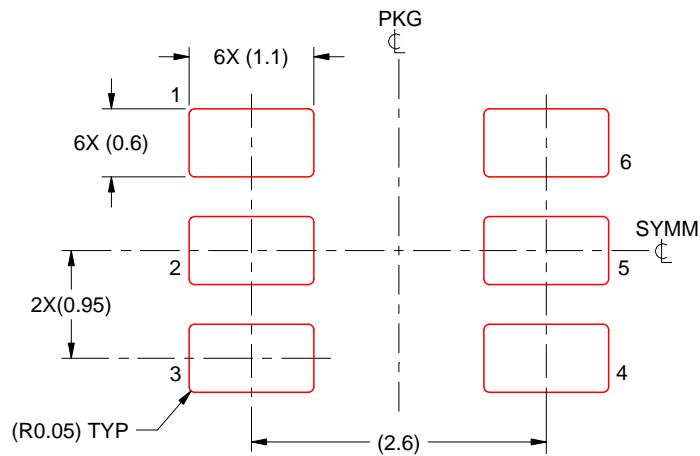
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



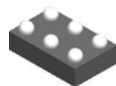
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

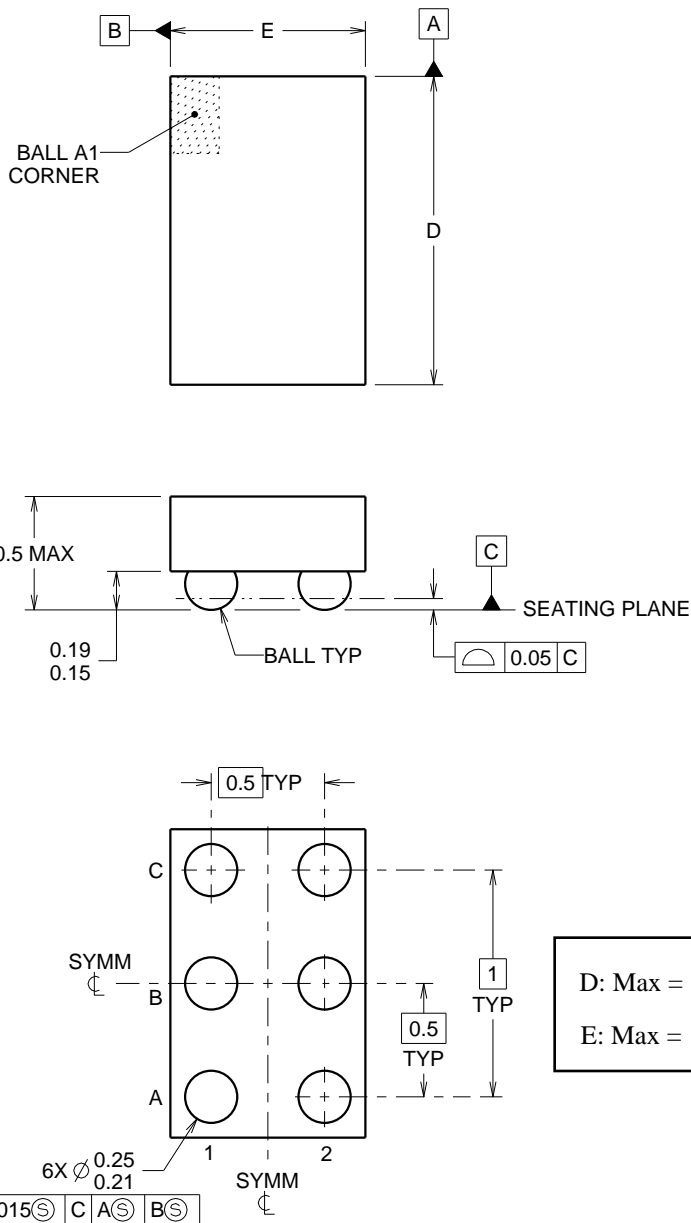
YZP0006



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219524/A 06/2014

## NOTES:

NanoFree Is a trademark of Texas Instruments.

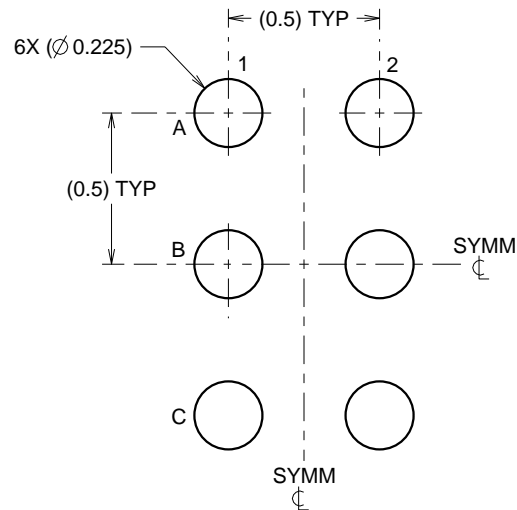
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

# EXAMPLE BOARD LAYOUT

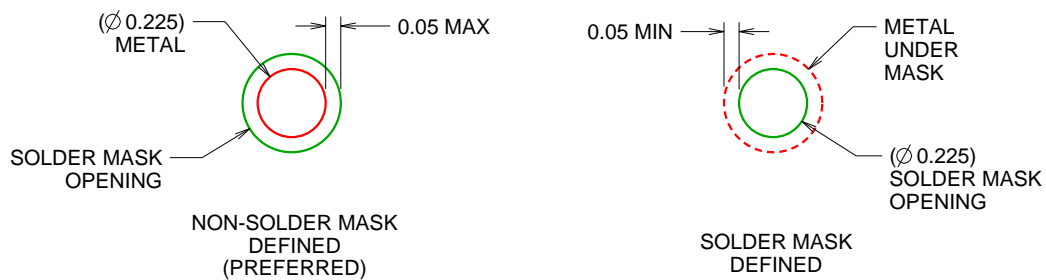
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

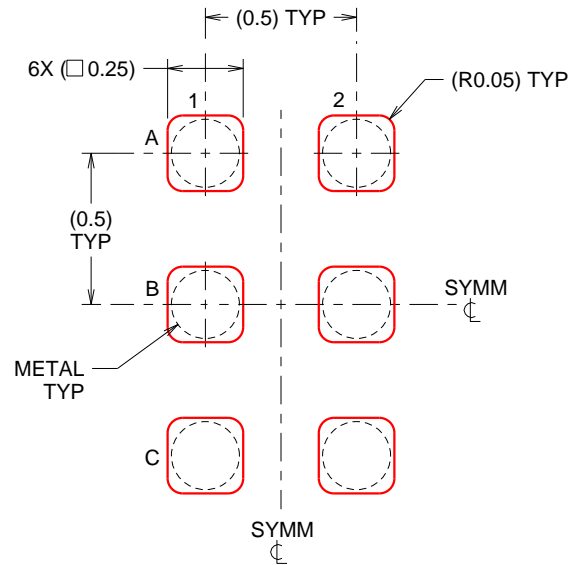
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 ([www.ti.com/lit/sbva017](http://www.ti.com/lit/sbva017)).

# EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.