DRV8844 Quad ½-H-Bridge Driver IC

1 Features

- Quad 1/2-H-Bridge DC Motor Driver
  - Can Drive Four Solenoids, Two DC Motors, One Stepper Motor, or Other Loads
  - Full Individual Half Bridge Control
  - Low MOSFET On-Resistance
- 2.5-A Maximum Drive Current at 24 V, 25°C
- Floating Input Buffers Allow Dual (Bipolar) Supplies (up to ±30 V)
- Built-In 3.3-V, 10-mA LDO Regulator
- Industry Standard IN/IN Digital Control Interface
- 8-V to 60-V Operating Supply Voltage Range
- Outputs Can Be Connected in Parallel
- Thermally Enhanced Surface Mount Package

2 Applications

- Textile Machines
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics

3 Description

The DRV8844 provides four individually controllable 1/2-H-bridge drivers. It can be used to drive two DC motors, one stepper motor, four solenoids, or other loads. The output driver channel for each channel consists of N-channel power MOSFET's configured in a 1/2-H-bridge configuration.

The DRV8844 can supply up to 2.5-A peak or 1.75-A RMS output current per channel (with proper PCB heatsinking at 24 V and 25°C) per H-bridge.

Separate inputs to independently control each 1/2-H-bridge are provided. To allow operation with split supplies, the logic inputs and nFAULT output are referenced to a separate floating ground pin.

Internal shutdown functions are provided for over current protection, short circuit protection, undervoltage lockout, and overtemperature.

The DRV8844 is available in a 28-pin HTSSOP package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8844	HTSSOP (28)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

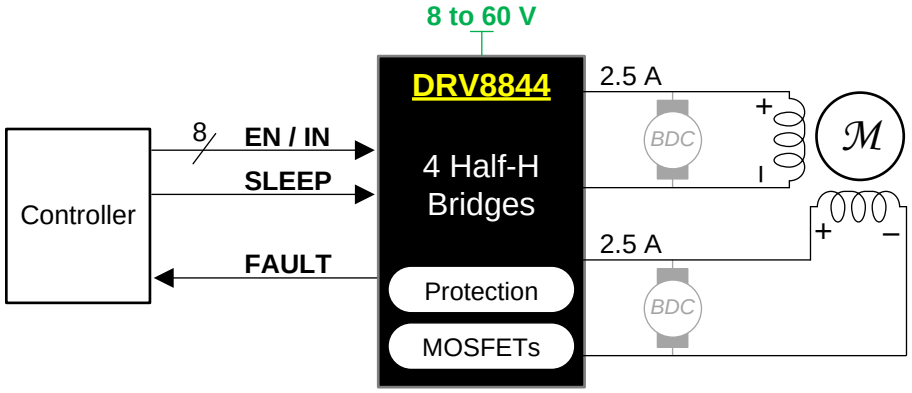


Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (May 2015) to Revision D **Page**

- Added parallel output connection to the *Features* section 1
- Changed pins 6 and 9 from VNEG to SRC12 and SRC34 (respectively) in the *Pin Configuration and Functions* section 3
- Added SRC12, SRC34 to VNEG pins parameter to the *Absolute Maximum Ratings* table 4
- Changed the *Functional Block Diagram* to show the change of pin 6 and 9 from VNEG to SRC12 and SRC34 8
- Added parallel output description and sense-resistor option to the *Application Information* section 12

Changes from Revision B (January 2015) to Revision C **Page**

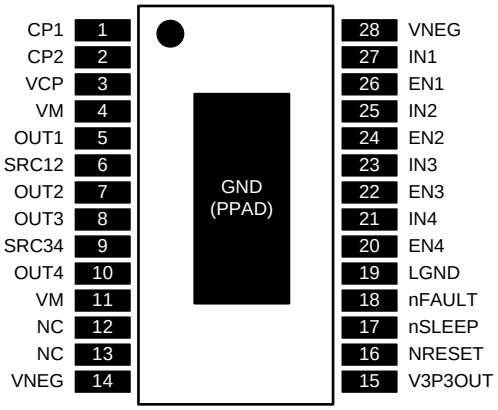
- Added ambient temperature to *Recommended Operating Conditions* 4

Changes from Revision A (October 2012) to Revision B **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 4

5 Pin Configuration and Functions

PWP Package
28-Pin HTSSOP
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
CP1	1	P	Charge pump flying capacitor	Connect a 0.01-µF 100-V capacitor between CP1 and CP2.
CP2	2	P	Charge pump flying capacitor	
LGND	19	P	Logic input reference ground	Connect to logic ground. This may be any voltage between VNEG and VM – 8 V.
V3P3OUT	15	P	3.3-V regulator output	Bypass to VNEG with a 0.47-µF 6.3-V ceramic capacitor. Can be used to supply VREF.
VCP	3	P	High-side gate drive voltage	Connect a 0.1-µF 16-V ceramic capacitor to VM.
VM	4, 11	P	Main power supply	Connect to motor supply (8 V to 60 V). Both pins must be connected to same supply. Bypass to VNEG with a 10-µF (minimum) capacitor.
SRC12	6	P	Low-side FET source for OUT1 and OUT2	Connect to VNEG directly or through optional current-sense resistor
SRC34	9	P	Low-side FET source for OUT3 and OUT4	
VNEG	14, 28, PPAD	P	Negative power supply (dual supplies) or ground (single supply)	
CONTROL				
EN1	26	I	Channel 1 enable	Logic high enables OUT1. Internal pulldown.
EN2	24	I	Channel 2 enable	Logic high enables OUT2. Internal pulldown.
EN3	22	I	Channel 3 enable	Logic high enables OUT3. Internal pulldown.
EN4	20	I	Channel 4 enable	Logic high enables OUT4. Internal pulldown.
IN1	27	I	Channel 1 input	Logic input controls state of OUT1. Internal pulldown.
IN2	25	I	Channel 2 input	Logic input controls state of OUT2. Internal pulldown.
IN3	23	I	Channel 3 input	Logic input controls state of OUT3. Internal pulldown.
IN4	21	I	Channel 4 input	Logic input controls state of OUT4. Internal pulldown.
nRESET	16	I	Reset input	Active-low reset input initializes internal logic and disables the H-bridge outputs. Internal pulldown.
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode. Internal pulldown.

(1) I = input, O = output, OD = open-drain output, P = power

Pin Functions (continued)

PIN		TYPE[1]	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
STATUS				
nFAULT	18	OD	Fault	Logic low when in fault condition (overtemperature, overcurrent, UVLO). Open-drain output.
OUTPUT				
OUT1	5	O	Output 1	Connect to loads
OUT2	7	O	Output 2	
OUT3	8	O	Output 3	
OUT4	10	O	Output 4	
NO CONNECT				
NC	12, 13	—	No connect	No connection to these pins

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
VM	Power supply voltage	–0.3	65	V
	Logic ground voltage (LGND)	–0.5	VM - 8	V
	Digital pin voltage	LGND – 0.5	LGND + 7	V
	SRC12, SRC34 (pins 6 and 9 with optional sense resistor) to VNEG pins (pins 14 and 28)	–0.6	0.6	V
	Peak motor drive output current, t < 1 µs	Internally limited		A
	Continuous motor drive output current[2]		2.5	A
T_J	Operating virtual junction temperature	–40	150	°C
T_{stg}	Storage temperature	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range, all voltages relative to VNEG terminal (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage[1]	8		60	V
I_{V3P3}	V3P3OUT load current	0		10	mA
T_A	Ambient temperature	–40		125	°C

(1) All V_M pins must be connected to the same supply voltage.

6.4 Thermal Information

THERMAL METRIC[1]		DRV8844 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	31.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = 25°C, over operating free-air temperature range, all voltages relative to VNEG terminal (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	V_M = 24 V, f_{PWM} < 50 kHz		1	5	mA
I_{VMQ}	VM sleep mode supply current	V_M = 24 V		500	800	µA
V_{UVLO}	VM undervoltage lockout voltage	V_M rising		6.3	8	V
V3P3OUT REGULATOR						
V_{3P3}	V3P3OUT voltage	IOUT = 0 to 1 mA	3.18	3.3	3.52	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage			LGND + 0.6	LGND + 0.7	V
V_{IH}	Input high voltage		LGND + 2.2		LGND + 5.25	V
V_{HYS}	Input hysteresis		50		600	mV
I_{IL}	Input low current	VIN = LGND	–5		5	µA
I_{IH}	Input high current	VIN = LGND + 3.3 V			100	µA
R_{PD}	Internal pulldown resistance			100		kΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)						
V_{OL}	Output low voltage	I_O = 5 mA			LGND + 0.5	V
I_{OH}	Output high leakage current	V_O = LGND + 3.3 V			1	µA
H-BRIDGE FETS						
$R_{DS(ON)}$	HS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.24		Ω
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.29	0.39	
	LS FET on resistance	V_M = 24 V, I_O = 1 A, T_J = 25°C		0.24		
		V_M = 24 V, I_O = 1 A, T_J = 85°C		0.29	0.39	
I_{OFF}	Off-state leakage current		–2		2	µA
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		3	5		A
t_{DEAD}	Output dead time			90		ns
t_{OCP}	Overcurrent protection deglitch time			5		µs
T_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	°C

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)(1) (see Figure 1)

NUMBER	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
1	t_1	Delay time, ENx high to OUTx high, INx = 1	130	330	ns
2	t_2	Delay time, ENx low to OUTx low, INx = 1	275	475	ns
3	t_3	Delay time, ENx high to OUTx low, INx = 0	100	300	ns
4	t_4	Delay time, ENx low to OUTx high, INx = 0	200	400	ns
5	t_5	Delay time, INx high to OUTx high	300	500	ns
6	t_6	Delay time, INx low to OUTx low	275	475	ns
7	t_R	Output rise time, resistive load to VNEG	30	150	ns
8	t_F	Output fall time, resistive load to VNEG	30	150	ns

(1) Not production tested – specified by design

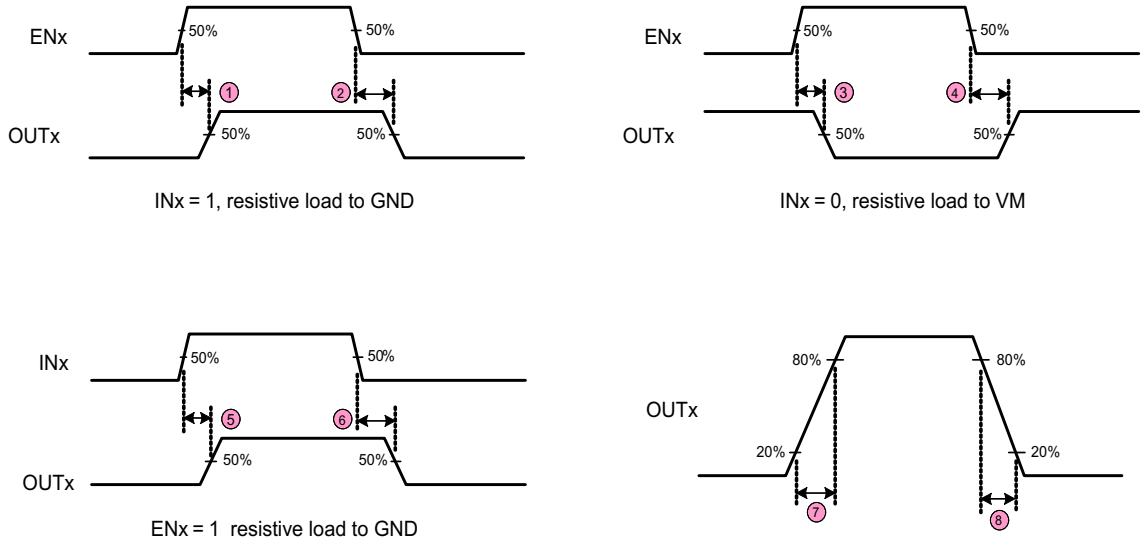


Figure 1. DRV8844 Switching Characteristics

6.7 Typical Characteristics

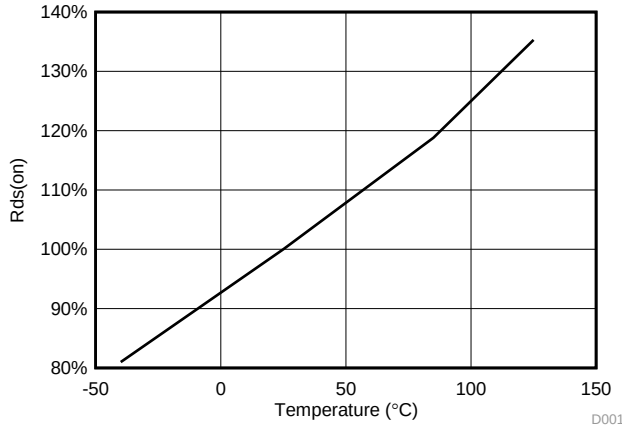


Figure 2. $R_{DS(ON)}$ vs Temperature

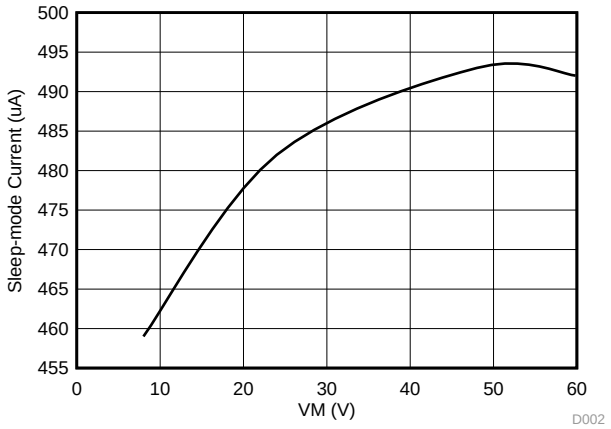


Figure 3. Sleep-Mode Current vs VM

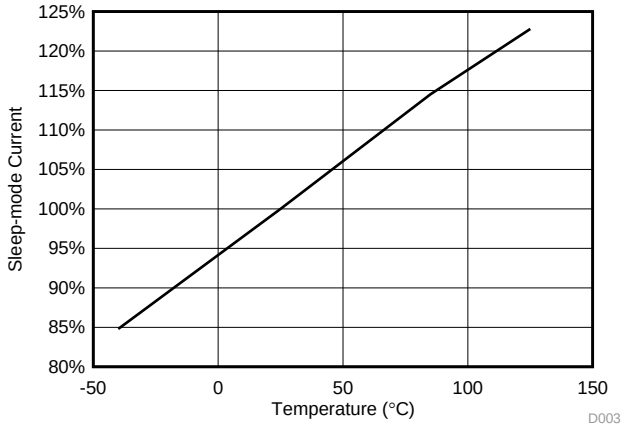


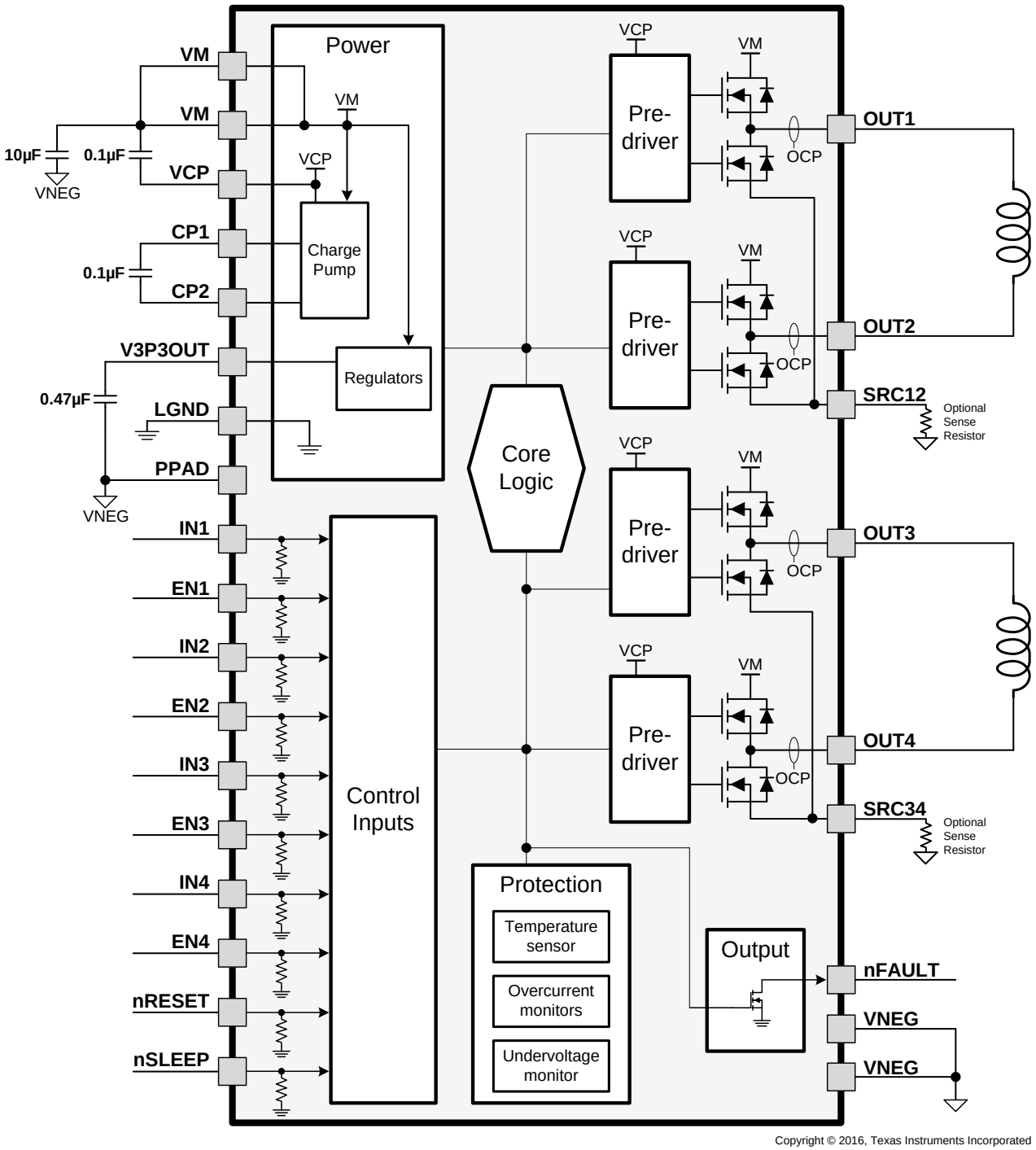
Figure 4. Sleep-Mode Current vs Temperature

7 Detailed Description

7.1 Overview

The DRV8844 integrates four independent 2.5-A half-H bridges, protection circuits, sleep mode, and fault reporting. Its single power supply supports a wide 8 to 60 V, making it well-suited for motor drive applications, including brushed DC, steppers, and solenoids.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Output Stage

The DRV8844 contains four 1/2-H-bridge drivers using N-channel MOSFETs. A block diagram of the output circuitry is shown in Figure 5.

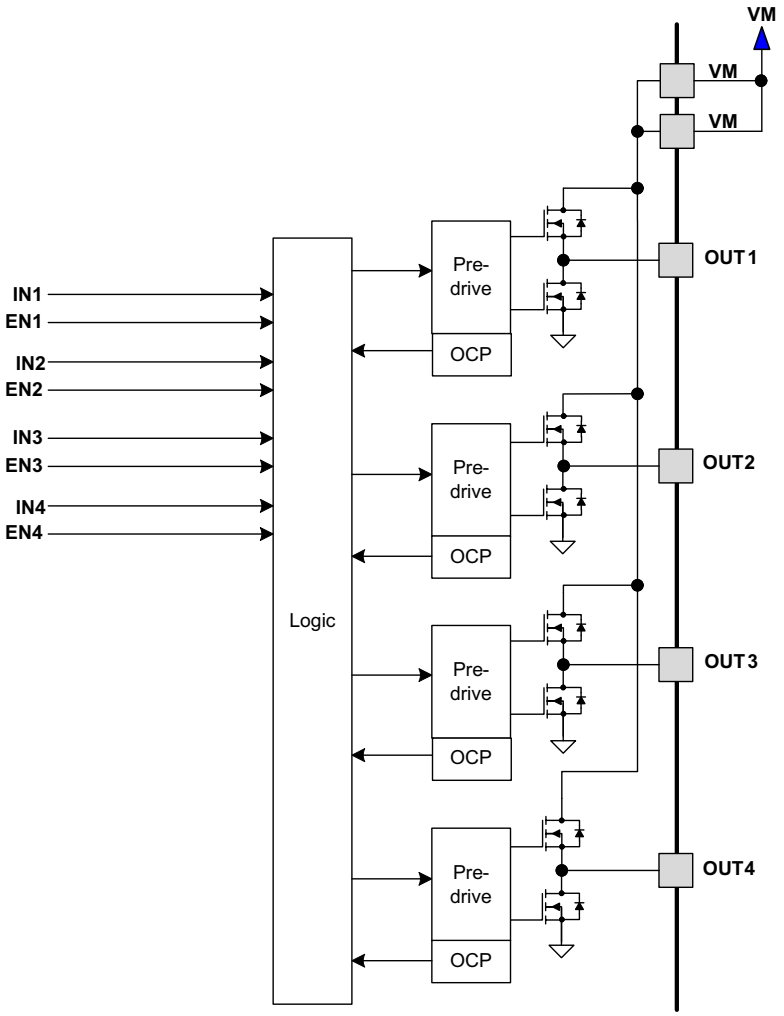


Figure 5. Motor Control Circuitry

The output pins are driven between VM and VNEG. VNEG is normally ground for single supply applications, and a negative voltage for dual supply applications.

Note that there are multiple VM motor power supply pins. All VM pins must be connected together to the motor supply voltage.

7.3.2 Logic Inputs

The logic inputs and nFAULT output are referenced to the LGND pin. This pin would be connected to the logic ground of the source of the logic signals (for example, microcontroller). This allows LGND to be at a different voltage than VNEG; for example, the designer can drive a load with bipolar power supplies by driving VM with +24 V and VNEG with -24 V, and connect LGND to 0 V (ground).

Feature Description (continued)

7.3.3 Bridge Control

The INx input pins directly control the state (high or low) of the OUTx outputs; the ENx input pins enable or disable the OUTx driver. Table 1 shows the logic.

Table 1. H-Bridge Logic

INx	ENx	OUTx
X	0	Z
0	1	L
1	1	H

The inputs can also be used for PWM control of, for example, the speed of a DC motor. When controlling a winding with PWM, when the drive current is interrupted, the inductive nature of the motor requires that the current must continue to flow. This is called recirculation current. To handle this recirculation current, the H-bridge can operate in two different states, fast decay or slow decay. In fast decay mode, the H-bridge is disabled and recirculation current flows through the body diodes; in slow decay, the motor winding is shorted.

To PWM using fast decay, the PWM signal is applied to the ENx pin; to use slow decay, the PWM signal is applied to the INx pin. Table 2 is an example of driving a DC motor using OUT1 and OUT2 as an H-bridge:

Table 2. PWM Function

IN1	EN1	IN2	EN2	FUNCTION
PWM	1	0	1	Forward PWM, slow decay
0	1	PWM	1	Reverse PWM, slow decay
1	PWM	0	PWM	Forward PWM, fast decay
0	PWM	1	PWM	Reverse PWM, fast decay

Figure 6 shows the current paths in different drive and decay modes:

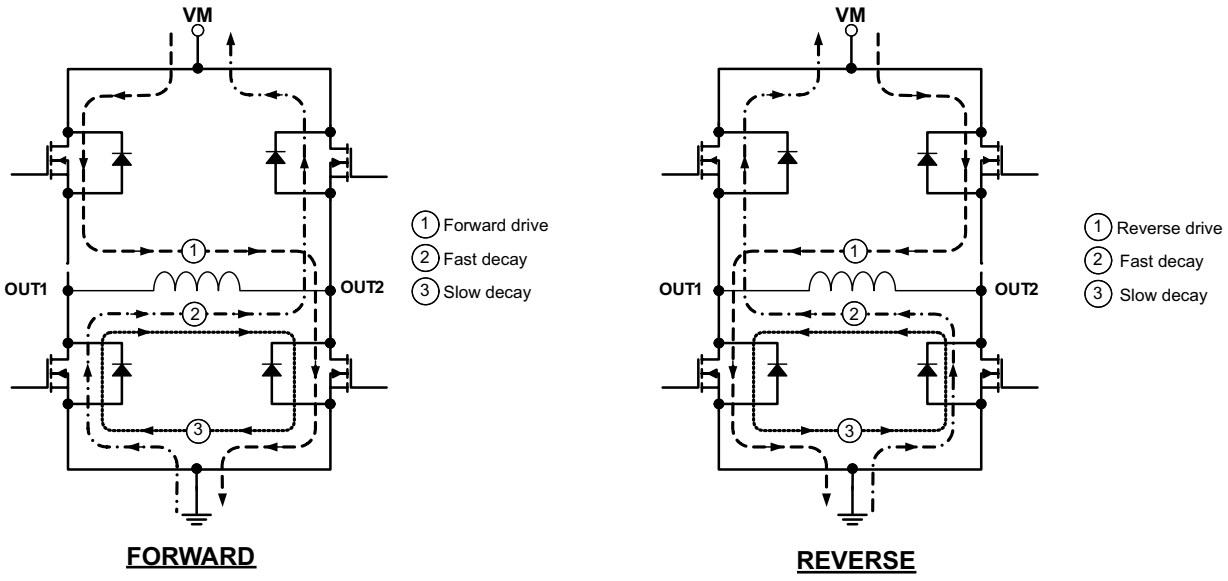


Figure 6. Current Paths

7.3.4 Charge Pump

Because the output stages use N-channel FETs, a gate drive voltage higher than the VM power supply is needed to fully enhance the high-side FETs. The DRV8844 integrates a charge pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. Refer to the block diagram and pin descriptions for details on these capacitors (value, connection, and so forth).

The charge pump is shut down when nSLEEP is low.

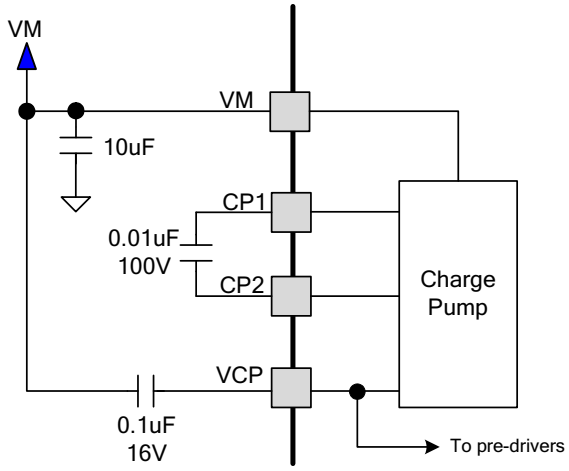


Figure 7. Charge Pump

7.3.5 Protection Circuits

The DRV8844 is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.5.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP deglitch time, the channel experiencing the overcurrent will be disabled and the nFAULT pin will be driven low. The driver will remain off until either RESET is asserted or VM power is cycled.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown.

7.3.5.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

7.3.5.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all outputs will be disabled, internal logic will be reset, and the nFAULT pin will be driven low. Operation will resume when VM rises above the UVLO threshold.

7.4 Device Functional Modes

7.4.1 nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge drivers. All inputs are ignored while nRESET is active.

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridges are disabled, the gate drive charge pump is stopped and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational. Note that nRESET and nSLEEP have internal pulldown resistors of approximately 100 kΩ. These signals need to be driven to logic high for device operation.

The V3P3OUT LDO regulator remains operational in sleep mode.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8844 can be used to drive one stepper motor, multiple brushed DC motors, or multiple other inductive loads.

The outputs can be connected in parallel to increase the drive current. If connecting the outputs as in a full-bridge configuration, any two outputs can be connected in parallel. If configured as two independent half bridges, OUT1 and OUT2 must be paired, and OUT3 and OUT4 must be paired. This pairing is because pin 6 (SRC12) is the source for the low-side FETs of OUT1 and OUT2, and pin 9 (SRC34) is the source for the low-side FETs of OUT3 and OUT4.

An optional sense resistor can be used to monitor the current. If using sense resistors, place the resistor between the SRC12 or SRC34 pins and the VNEG pins.

8.2 Typical Application

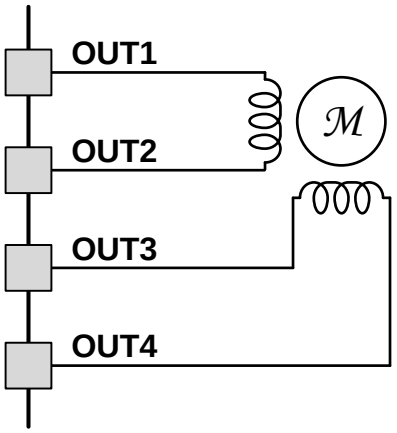


Figure 8. Stepper Motor Connections

Typical Application (continued)

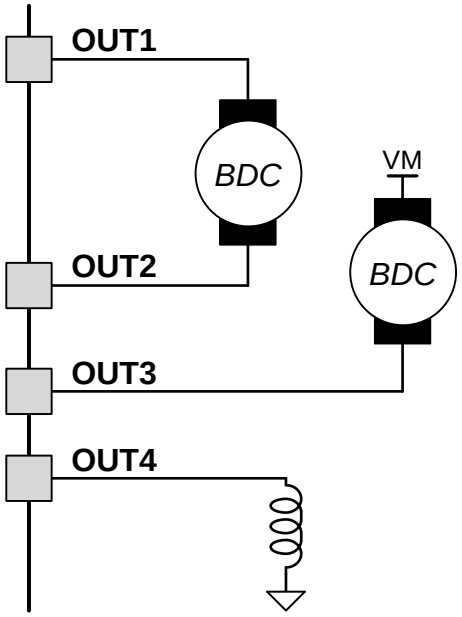


Figure 9. Example Showing a Bidirectional Brushed DC Motor, Single-Direction Brushed DC Motor, and an Inductive Load

8.2.1 Design Requirements

The following truth tables describe how to control the arrangement in Figure 8.

Table 3. Brushed DC Motor

FUNCTION	EN1	EN2	IN1	IN2	OUT1	OUT2
Forward	1	1	PWM	0	H	L
Reverse	1	1	0	PWM	L	H
Brake	1	1	0	0	L	L
Brake	1	1	1	1	H	H
Coast	0	X	X	X	Z	X
Coast	X	0	X	X	X	Z

Table 4. Single-Direction Brushed DC Motor

FUNCTION	EN3	IN3	OUT3
On	1	$\overline{\text{PWM}}$	L
Brake	1	1	H
Coast	0	X	Z

Table 5. Inductive Loads

FUNCTION	EN4	IN4	OUT4
On	1	PWM	H
Off or slow decay	1	0	L
Off or coast	0	X	Z

8.2.2 Detailed Design Procedure

8.2.2.1 Motor Voltage

The ratings of the motor selected and the desired RPM determine the motor voltage the designer should use. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

8.2.3 Application Curves

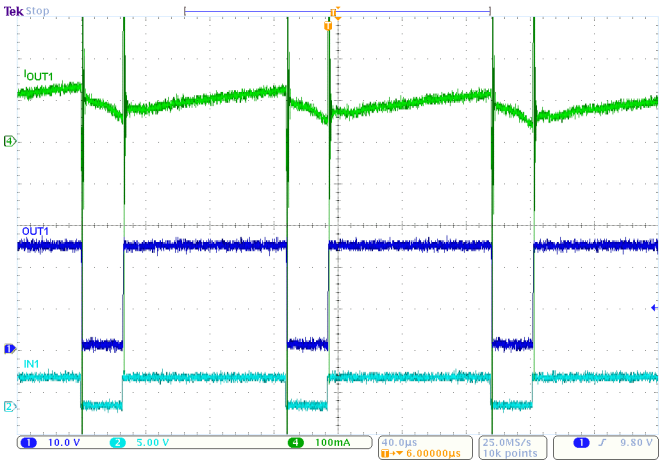


Figure 10. DC Motor With 80 PWM

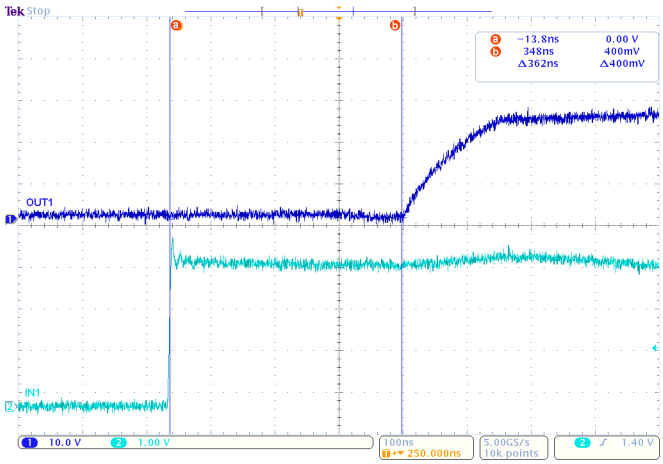


Figure 11. IN1 to OUT1 Propagation Delay

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (Brushed DC, Brushless DC, Stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

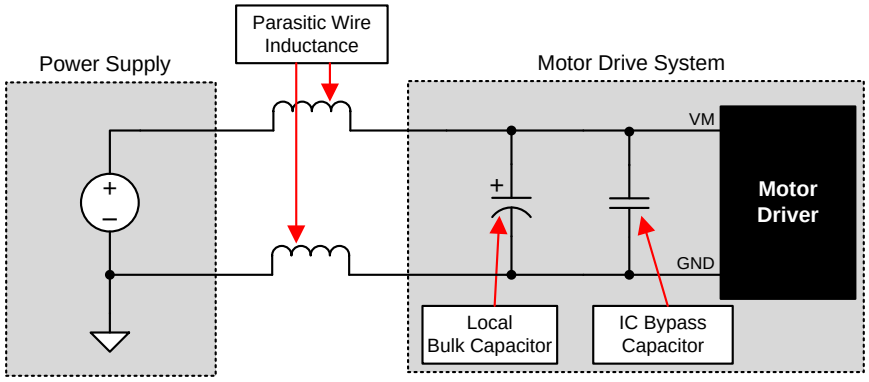


Figure 12. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors should be ceramic, and placed closely to device pins.

The high-current device outputs should use wide metal traces.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias help dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

10.2 Layout Example

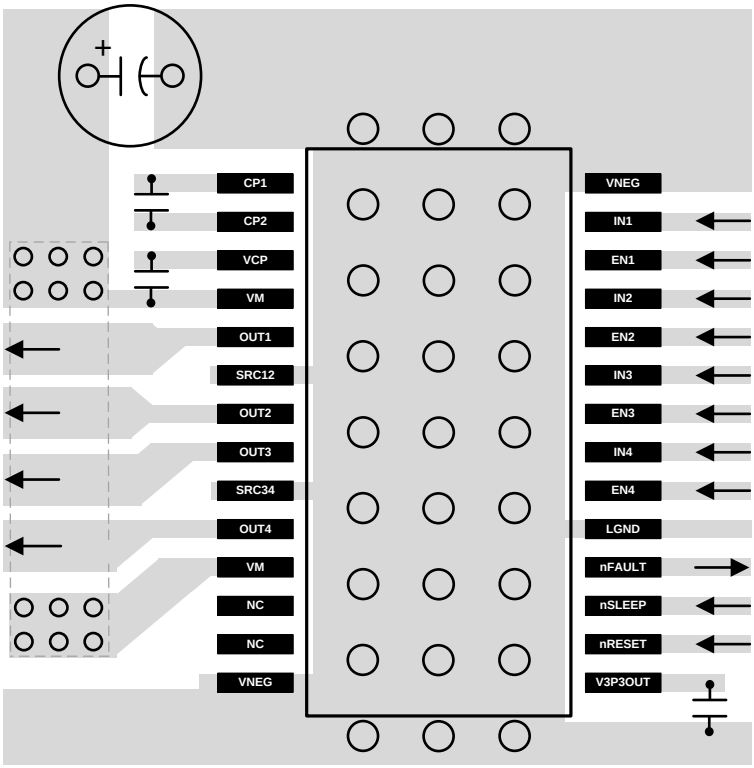


Figure 13. Layout Schematic

10.3 Thermal Considerations

The DRV8844 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

Thermal Considerations (continued)

10.3.1 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report SLMA002, *PowerPAD™ Thermally Enhanced Package* and TI application brief SLMA004, *PowerPAD™ Made Easy*, available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

10.4 Power Dissipation

Power dissipation in the DRV8844 is dominated by the power dissipated in the output FET resistance, or $R_{DS(ON)}$. Average power dissipation of each H-bridge when running a DC motor can be roughly estimated by Equation 1.

$$P = 2 \times R_{DS(ON)} \times \left(I_{OUT}\right)^2 \quad (1)$$

where

- P is the power dissipation of one H-bridge
- $R_{DS(ON)}$ is the resistance of each FET
- I_{OUT} is the RMS output current being applied to each winding

I_{OUT} is equal to the average current drawn by the DC motor. Note that at start-up and fault conditions this current is much higher than normal running current; these peak currents and their duration also need to be taken into consideration. The factor of 2 comes from the fact that at any instant two FETs are conducting winding current (one high-side and one low-side).

The total device dissipation will be the power dissipated in each of the two H-bridges added together.

The maximum amount of power that can be dissipated in the device is dependent on ambient temperature and heatsinking.

Note that $R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Calculating Motor Driver Power Dissipation*, SLVA504
- *DRV8844 Evaluation Module*, SLVU762
- *Understanding Motor Driver Current Ratings*, SLVA505

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8844PWP	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8844	Samples
DRV8844PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8844	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

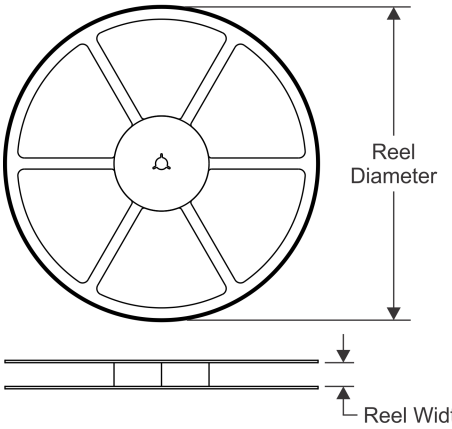
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE MATERIALS INFORMATION

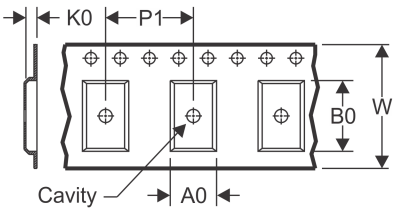
5-Jan-2022

TAPE AND REEL INFORMATION

REEL DIMENSIONS

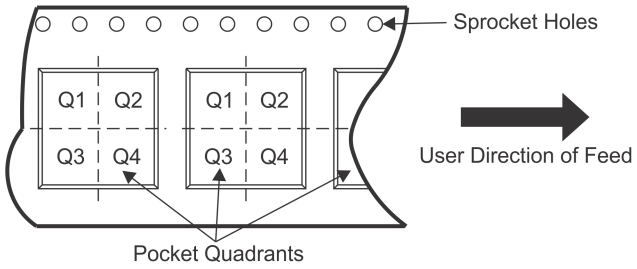


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



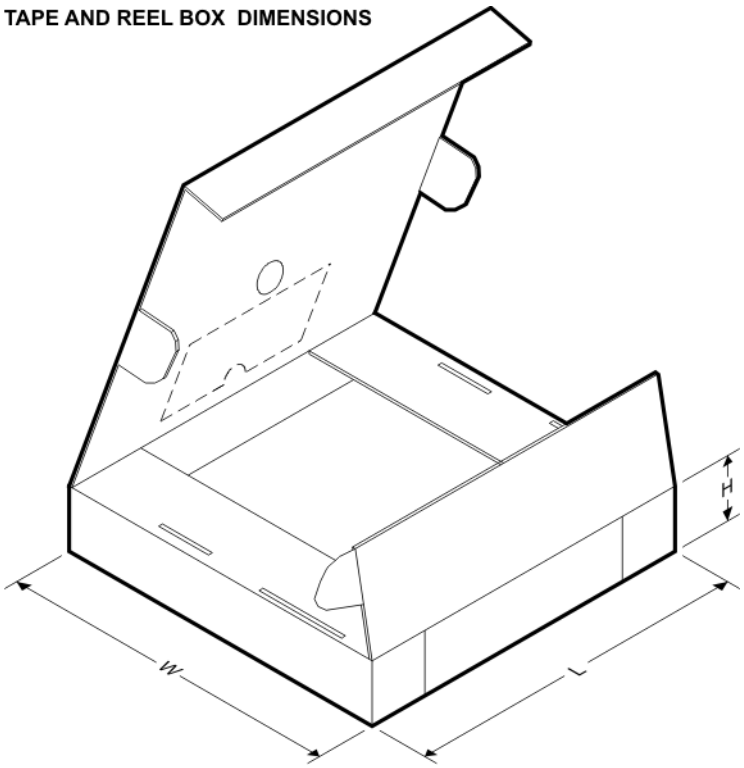
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8844PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

PACKAGE MATERIALS INFORMATION

5-Jan-2022

TAPE AND REEL BOX DIMENSIONS



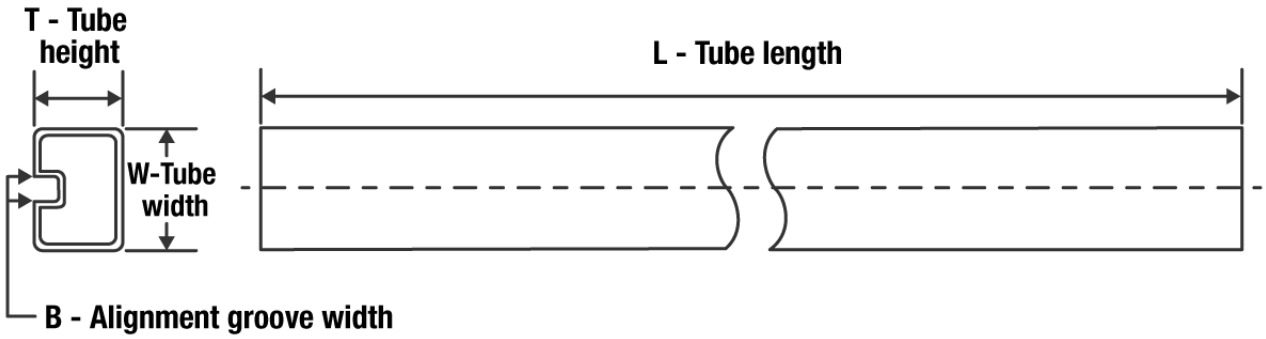
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8844PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

PACKAGE MATERIALS INFORMATION

5-Jan-2022

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DRV8844PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

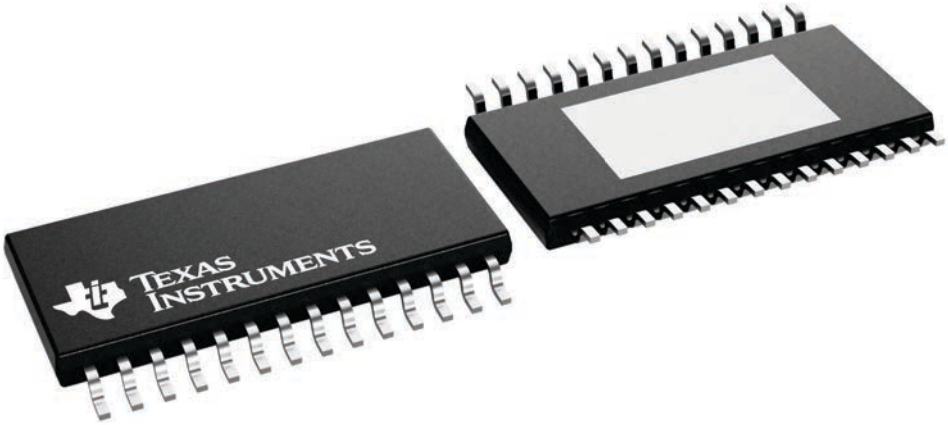
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 9.7, 0.65 mm pitch

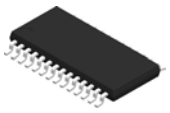
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



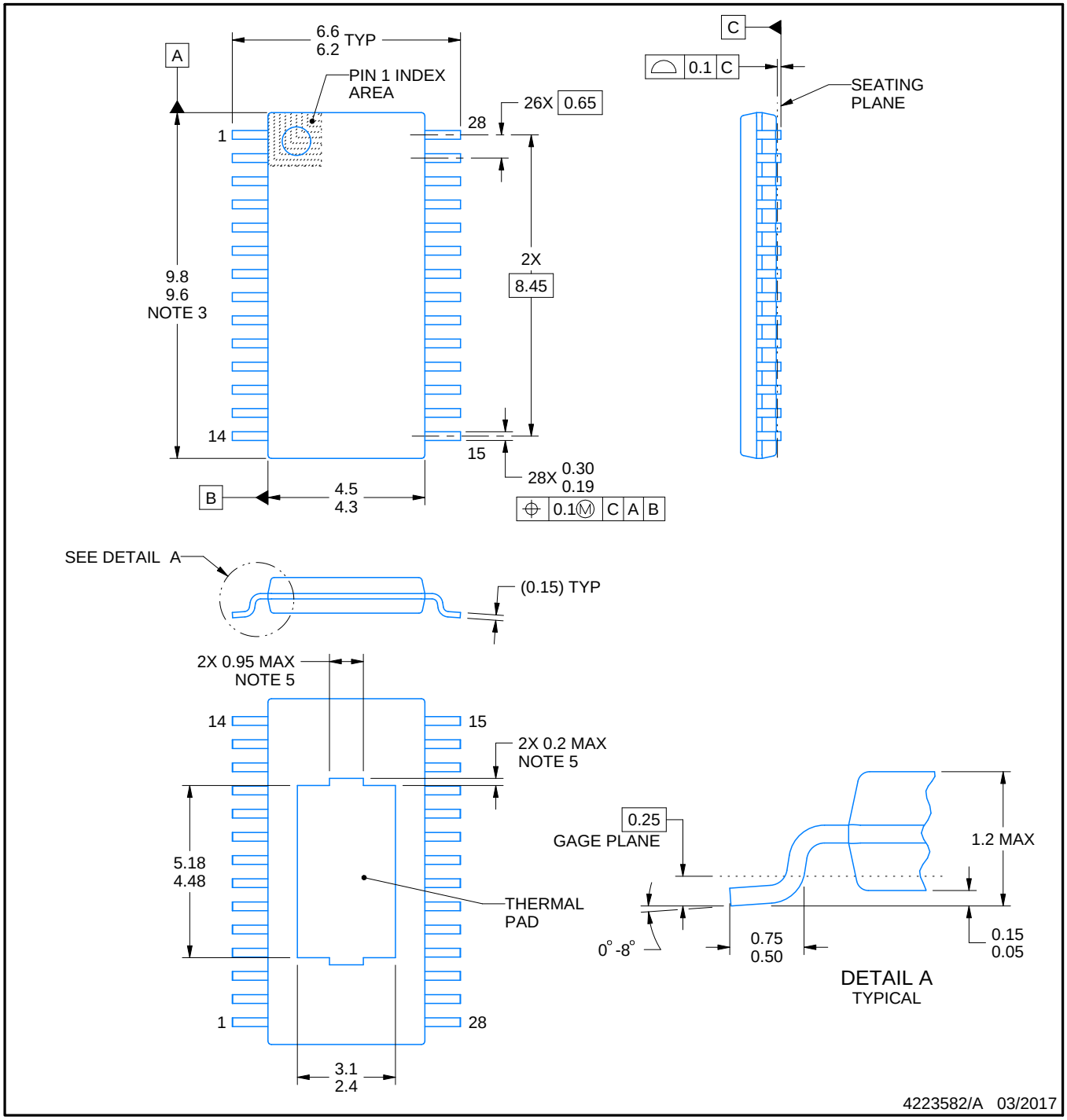
PACKAGE OUTLINE

PWP0028C



PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

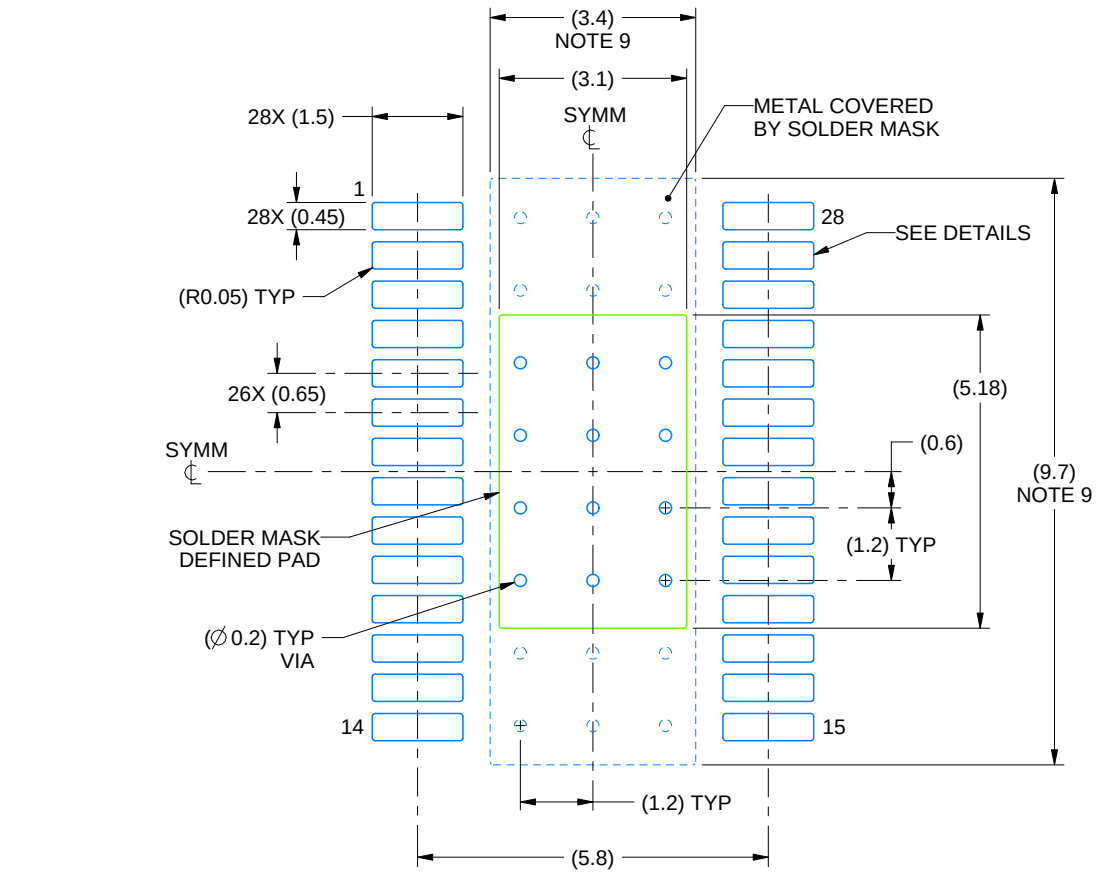
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

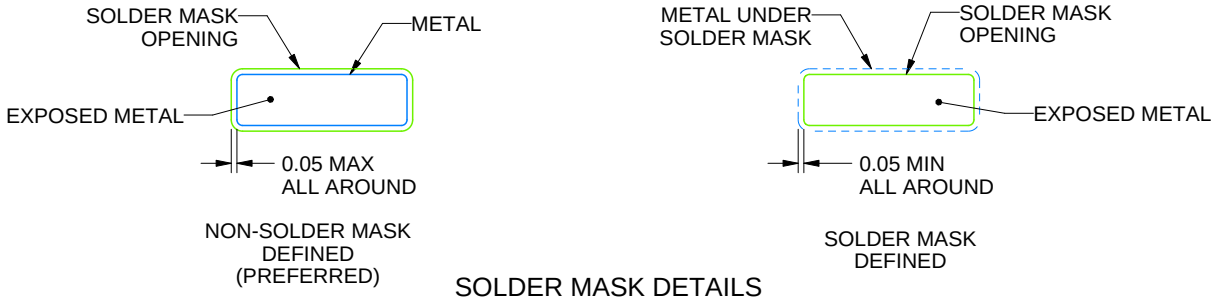
PWP0028C

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

4223582/A 03/2017

NOTES: (continued)

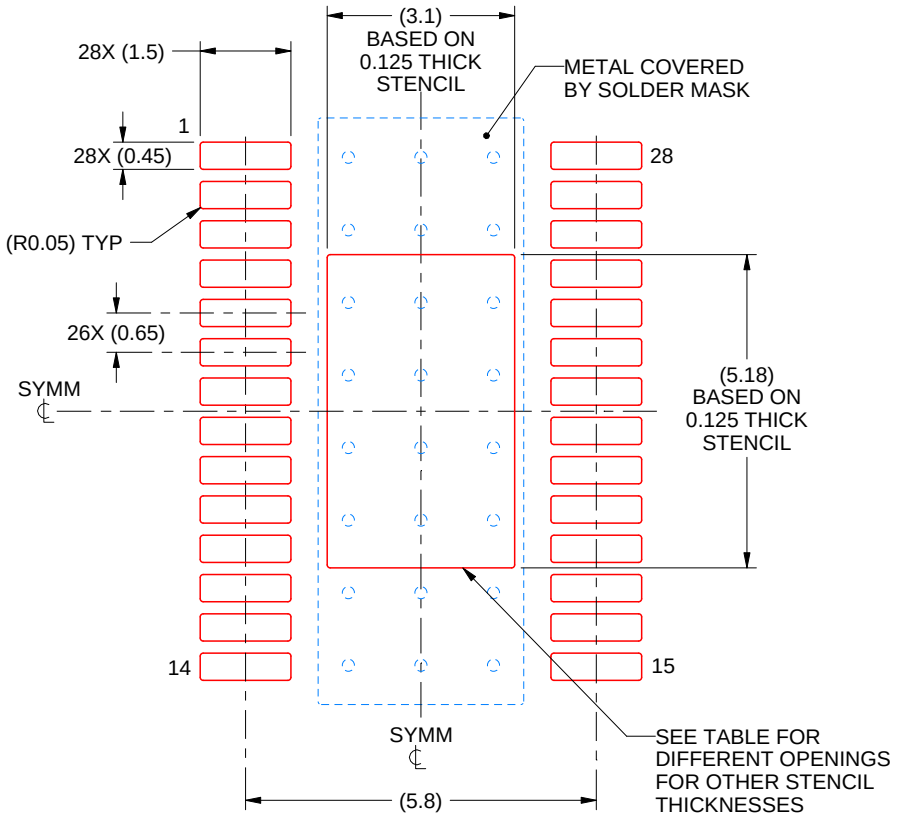
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0028C

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.47 X 5.79
0.125	3.10 X 5.18 (SHOWN)
0.15	2.83 X 4.73
0.175	2.62 X 4.38

4223582/A 03/2017

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.