SGM48510
Single 10A High Speed Low-Side MOSFET Driver

GENERAL DESCRIPTION

The SGM48510 is a single low-side MOSFET driver. It is capable of providing large peak currents into capacitive loads. This driver can deliver a 7A peak current at the Miller plateau region to help reduce the Miller effect during MOSFETs switching transitions.

It exhibits a split output configuration allowing the user to control the turn-on and turn-off slew rates. The SGM48510 is available in Green SOIC-8 and TDFN-2×2-8L packages.

FEATURES

- **High Current Drive Capability: ±10A**
- **TTL/CMOS Compatible Inputs Independent of Supply Voltage**
- **High Reverse Current Capability (10A) Peak**
- **4ns Typical Rise and 4ns Typical Fall Times with 1.8nF Load**
- **Fast Propagation Delay Times of 13ns with Input Falling and 13ns with Input Rising**
- **Input Voltage Range: 4.5V to 24V**
- **Split Output Configuration**
- **Dual Input Design Offering Drive Flexibility**
- **Available in Green SOIC-8 and TDFN-2×2-8L Packages**

APPLICATIONS

Server Power
Telecommunication, Datacenter Power
Synchronous Rectifier
Switch Mode Power Supply
DC/DC Converter
Power Factor Correction
Motor Drive
Renewable Energy, Solar Inverter

TYPICAL APPLICATION

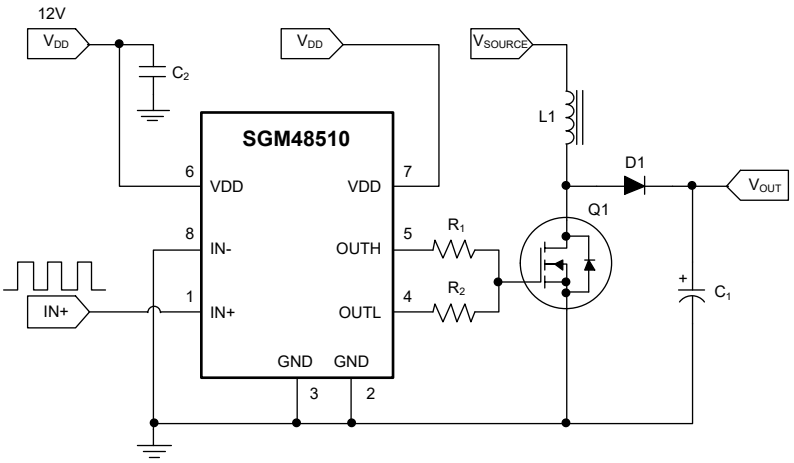


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM48510 (Fixed Digital Threshold)	SOIC-8	-40℃ to +125℃			
	TDFN-2×2-8L	-40℃ to +125℃			

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD} ..... -0.3V to 28V
Output Current (DC), I_{OUT_DC} 0.6A
Reverse Current (Pulse < 1μs) 10A
Output Current (Pulse < 0.5μs), I_{OUT_PULSE} 10A
Input Voltages, IN+, IN- ..... -6V to 24V
Output Voltages, OUTH, OUTL ..... -0.3V to V_{DD} + 0.3V
Output Voltages (Pulse < 0.5μs), OUTH, OUTL
..... -3.0V to V_{DD} + 3.0V
Package Thermal Resistance
SOIC-8, θ_{JA} ..... ℃/W
TDFN-2×2-8L, θ_{JA} ..... ℃/W
OUT Latch-Up Protection 500mA
Junction Temperature ..... +150℃
Storage Temperature Range ..... -65℃ to +150℃
Lead Temperature (Soldering, 10s) ..... +260℃
ESD Susceptibility
HBM 4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, VDD ..... 4.5V to 24V
Input Voltages, IN+, IN- ..... -5V to 24V
Junction Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

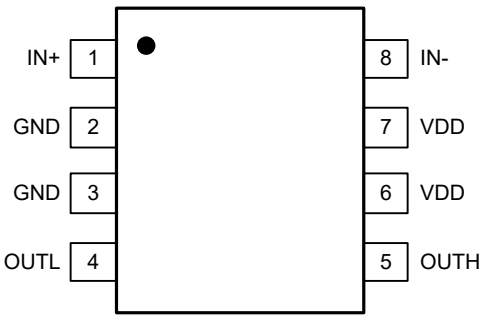
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

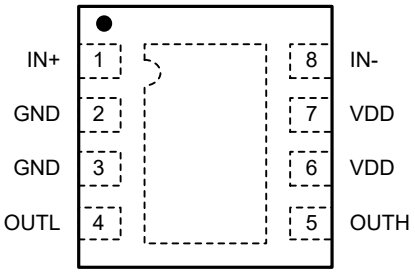
PIN CONFIGURATIONS

(TOP VIEW)



SOIC-8

(TOP VIEW)



TDFN-2×2-8L

PIN DESCRIPTION

PIN	NAME	I/O	FUNCTION
1	IN+	I	Non-Inverting Input. The input has logic compatible threshold and hysteresis. If not used, this pin should be connected to either VDD or GND. It should not be left unconnected.
2, 3	GND	G	Common Ground. This ground should be connected very closely to the source of the power MOSFET.
4	OUTL	O	Sink Pin. Connect to gate of MOSFET.
5	OUTH	O	Source Pin. Connect to gate of MOSFET.
6, 7	VDD	P	Power Supply Input Pin.
8	IN-	I	Inverting Input. The input has logic compatible threshold and hysteresis. If not used, this pin should be connected to either VDD or GND. It should not be left unconnected.

NOTE: I: input; O: output; G: ground; P: power for the circuit.

Table 1. Logic Truth Table

IN+	IN-	OUTH	OUTL	OUT (OUTH & OUTL Connected Together)
L	L	High-Z	L	L
L	H	High-Z	L	L
H	L	H	High-Z	H
H	H	High-Z	L	L

ELECTRICAL CHARACTERISTICS

(Typical values: V_{DD} = 12V, 1μF from VDD to GND, T_A = T_J = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage						
VDD Under Voltage Lockout (Rising)	V_{CCR}	VDD rising	3.7	3.9	4.1	V
VDD Under Voltage Lockout (Falling)	V_{CCF}	VDD falling	3.4	3.6	3.8	V
VDD Under Voltage Lockout (Hysteresis)	V_{CCH}			300		mV
Operating Current (No Switching)	I_{DD}			1	1.5	mA
VDD Under Voltage Lockout to Output Delay		VDD rising		10		μs
Inputs						
High Threshold	V_{THH}	Input rising from logic low	1.9	2.1	2.3	V
Low Threshold	V_{THL}	Input falling from logic high	1.1	1.3	1.5	V
Input Signal Hysteresis	V_{IN_HYS}			0.8		V
IN- Pull-Up Resistor	R_{IN-}			200		kΩ
IN+ Pull-Down Resistor	R_{IN+}			200		kΩ
Outputs						
Output Resistance High	R_{OH}	I_{OUT} = -10mA		0.4	0.8	Ω
Output Resistance Low	R_{OL}	I_{OUT} = +10mA		0.4	0.8	Ω
Peak Source Current	I_{SOURCE}	OUT = GND, 200ns Pulse		10		A
Miller Plateau Source Current	I_{SOURCE}	OUT = 5.0V, 200ns Pulse		7		A
Peak Sink Current	I_{SINK}	OUT = VDD, 200ns Pulse		10		A
Miller Plateau Sink Current	I_{SINK}	OUT = 5.0V, 200ns Pulse		7		A
Switching Characteristics						
Propagation Delay Time Low to High, IN Rising (IN to OUT)	t_{D1}	C_{LOAD} = 1.8nF		13	22	ns
Propagation Delay Time High to Low, IN Falling (IN to OUT)	t_{D2}	C_{LOAD} = 1.8nF		13	22	ns
Rise Time	t_R	C_{LOAD} = 1.8nF		4	7	ns
Fall Time	t_F	C_{LOAD} = 1.8nF		4	7	ns

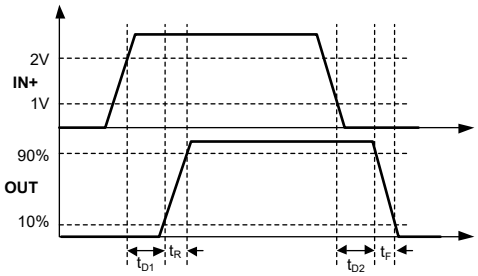


Figure 2. Non-Inverting Input Driver Operation

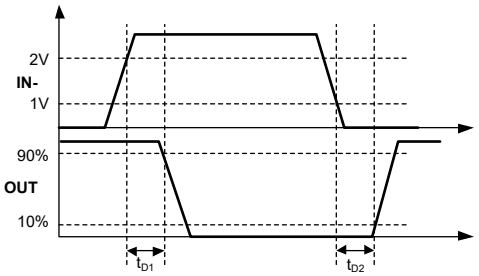


Figure 3. Inverting Input Driver Operation

FUNCTIONAL BLOCK DIAGRAM

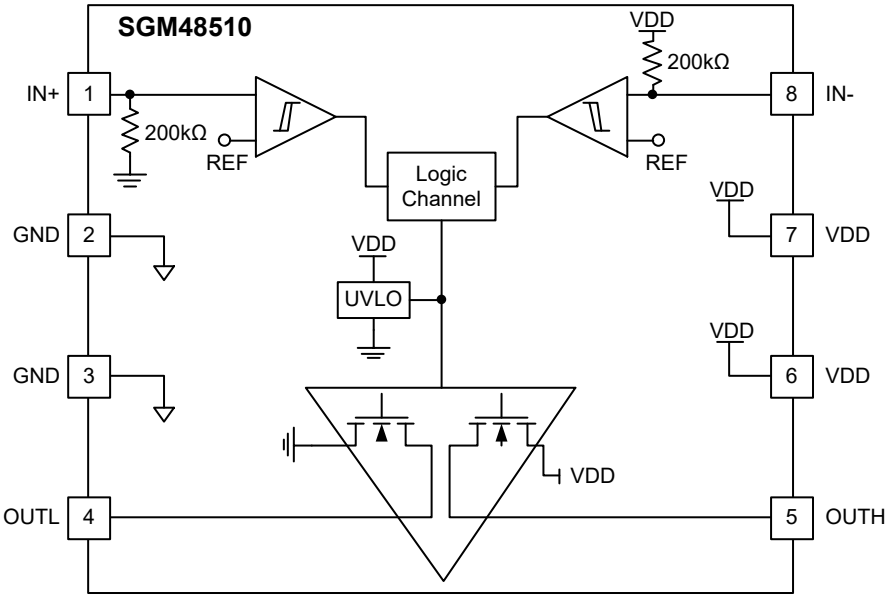


Figure 4. SGM48510 Block Diagram

PCB LAYOUT RECOMMENDATION

Proper component placement is extremely important in high current, fast switching applications to provide appropriate device operation and design robustness. The SGM48510 gate driver exhibits a powerful output stage enabling large peak currents with fast rise and fall times. Even though the SGM48510 provides a split output configuration for slew rate control, a proper PCB layout is crucial to ensure maximum performance. The following circuit layout guidelines are strongly recommended when designing with the SGM48510.

Place the driver close to the power MOSFET in order to have a low impedance path between the output pins and the gate. Keep the traces short and wide to minimize the parasitic inductance and accommodate for high peak currents.

Place the decoupling capacitor close to the gate drive IC. Placing the VDD capacitor close to the pin and ground improves noise filtering. This capacitor supplies high peak currents during the turn−on transition of the MOSFET. Using a low ESL chip capacitor is highly recommended.

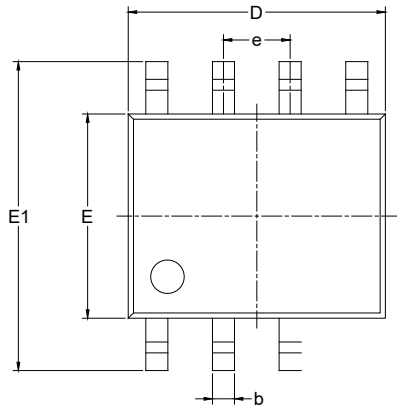
Keep a tight turn-on turn-off current loop path to minimize parasitic inductance. High di/dt will induce voltage spikes on the output pin and the MOSFET gate. Parallel the source and return signals taking advantage of flux cancellation.

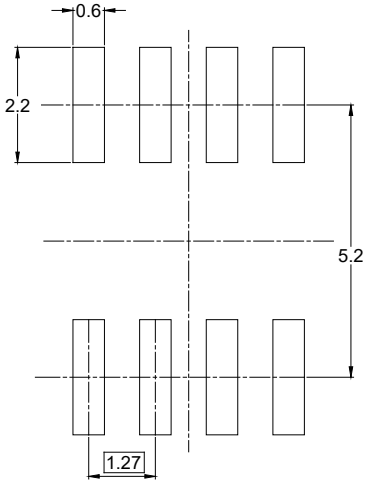
Since the SGM48510 is a 2mm × 2mm package driving high peak currents into capacitive loads, adding a shielding ground plane helps in power dissipation and noise blocking. The ground plane should not be a current carrying path to any of the current loops.

Any unused pin should be pulled to either rail depending on the functionality of the pin to avoid any malfunction on the output. Please refer to the pin description table for more information.

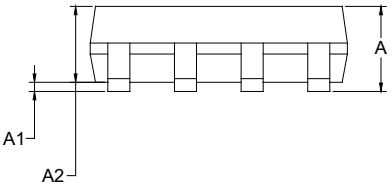
PACKAGE OUTLINE DIMENSIONS

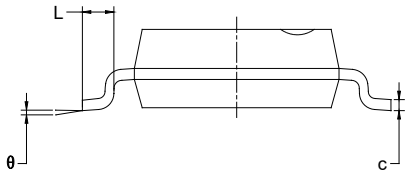
SOIC-8





RECOMMENDED LAND PATTERN (Unit: mm)

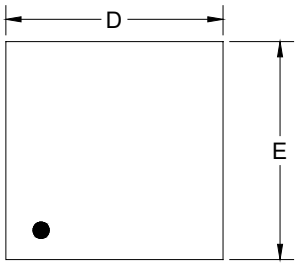




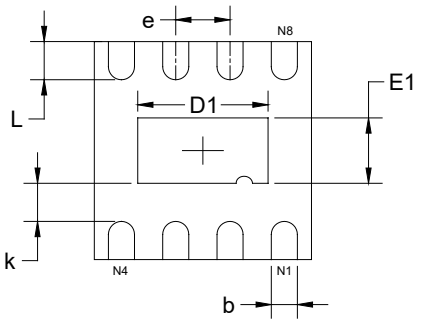
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.27 BSC		0.050 BSC	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGE OUTLINE DIMENSIONS

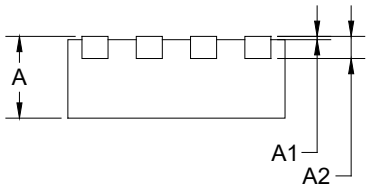
TDFN-2×2-8L



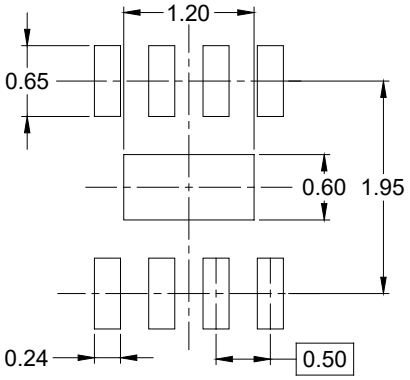
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN (Unit: mm)

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E	1.900	2.100	0.075	0.083
E1	0.500	0.700	0.020	0.028
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.250	0.450	0.010	0.018