FC4B22070L

Gate resistor installed Dual N-channel MOS FET

For lithium-ion secondary battery protection circuits

■ Features

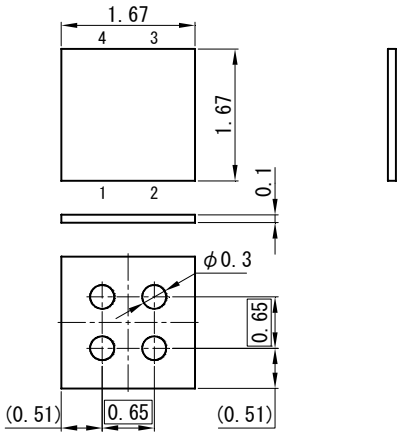
- Low source-source ON resistance:Rss(on) typ. = 17.5 mΩ（VGS = 4.5 V)
- CSP package:smallest & thinnest size
- RoHS compliant (EU RoHS / MSL:Level 1 compliant)

■ Marking Symbol: 14

■ Packaging

Embossed type (Thermo-compression sealing) : 8 000 pcs / reel (standard)

Unit: mm



1. Source (FET1) 3. Gate (FET2)
2. Gate (FET1) 4. Source (FET2)

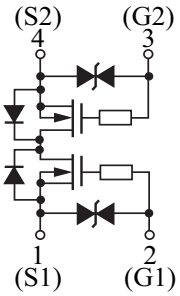
Panasonic	MLGA004-W-1717-RA
JEITA	—
Code	—

■ Absolute Maximum Ratings Ta = 25 °C

Parameter		Symbol	Rating	Unit
Source-source Voltage		VSS	24	V
Gate-source Voltage		VGS	±12	V
Source Current	DC[*1]	IS1	3.5	A
	DC[*2]	IS2	6	
	Pulse[*2,*3]	Isp	60	
Total Power Dissipation	DC[*1]	PD1	0.4	W
	DC[*2]	PD2	1.5	
Channel Temperature		Tch	150	°C
Storage Temperature Range		Tstg	-55 to +150	°C
Thermal Resistance	Channel to Case[*1]	Rth(ch-a)1	312	°C/W
	Channel to Case[*2]	Rth(ch-a)2	83	

Note *1 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm)
using the minimum recommended pad size (36μm Copper).
*2 Mounted on Ceramic substrate (70 mm × 70 mm × t1.0 mm).
*3 t = 10 μs, Duty Cycle ≤ 1 %

Equivalent circuit



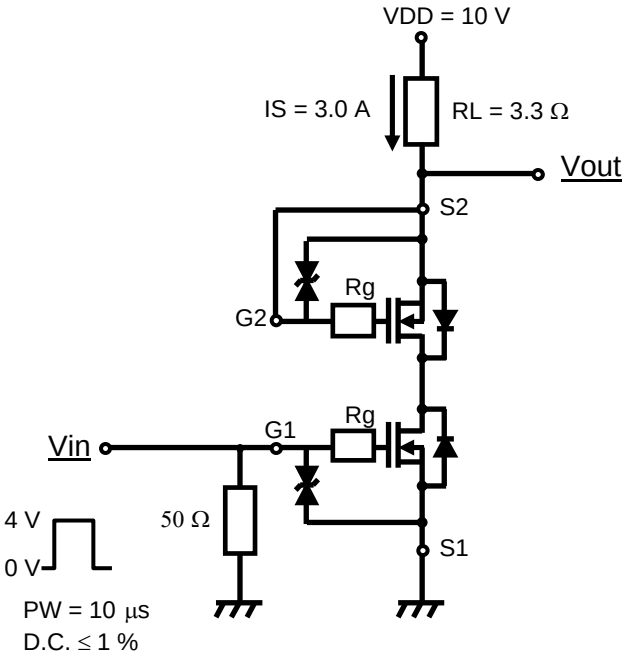
■ Electrical Characteristics Ta = 25 °C ± 3 °C

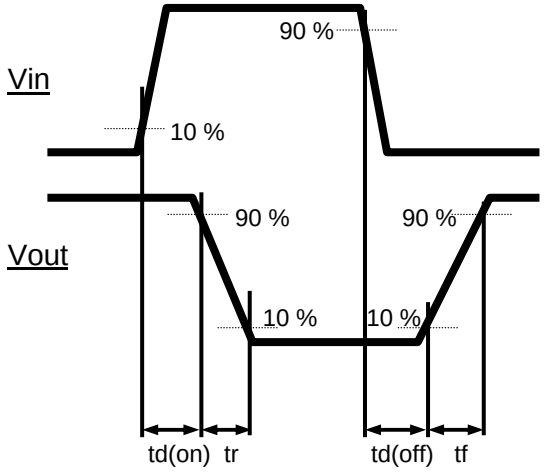
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	24			V
Zero Gate Voltage Source Current	ISSS	VSS = 24 V, VGS = 0 V			1.0	μA
Gate-source Leakage Current	IGSS	VGS = ±8 V, VSS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	IS = 1.0 mA, VSS = 10 V	0.4	0.9	1.4	V
Source-source On-state Resistance	RSS(on)1	IS = 3.0 A, VGS = 4.5 V	12	17.5	22	mΩ
	RSS(on)2	IS = 3.0 A, VGS = 3.1 V	13	20	28	
	RSS(on)3	IS = 3.0 A, VGS = 2.5 V	15	23	37	
Body Diode Forward Voltage	VF(S-S)	IF = 6.0 A, VGS = 0 V		0.8	1.2	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 MHz		1780		pF
Output Capacitance *1	Coss			410		
Reverse Transfer Capacitance *1	Crss			407		
Turn-on delay Time *1,*2	td(on)	VDD = 10 V, VGS = 0 to 4.0 V, IS = 3.0 A		0.8		μs
Rise Time *1,*2	tr			1.5		
Turn-off delay Time *1,*2	td(off)	VDD = 10 V, VGS = 4.0 to 0 V, IS = 3.0 A		6.0		μs
Fall Time *1,*2	tf			3.0		
Total Gate Charge *1	Qg	VDD = 10 V, VGS = 0 to 4.0 V, IS = 6.0 A		15.0		nC
Gate-source Charge *1	Qgs			4.1		
Gate-drain Charge *1	Qgd			3.8		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Assured by design

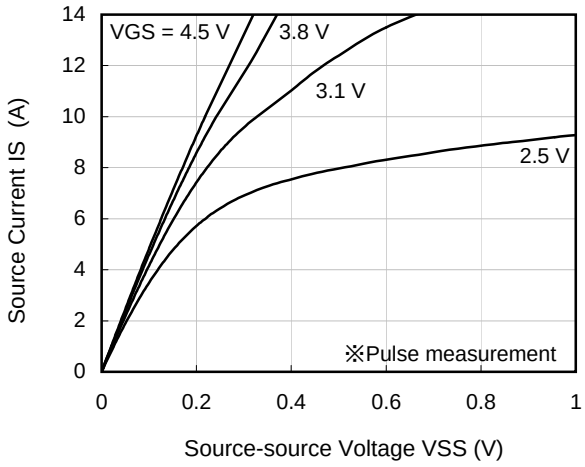
*2 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time



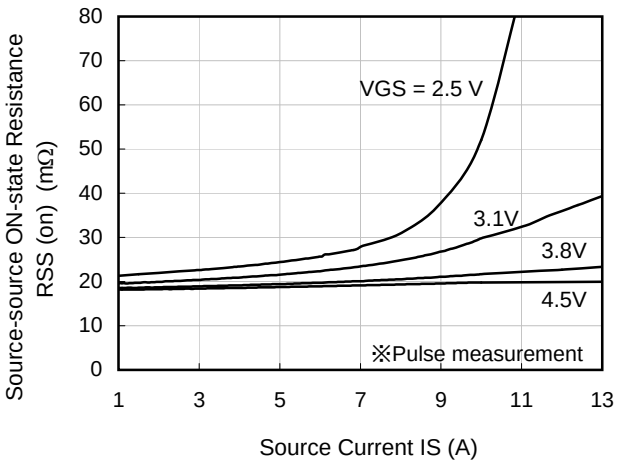


Technical Data (reference)

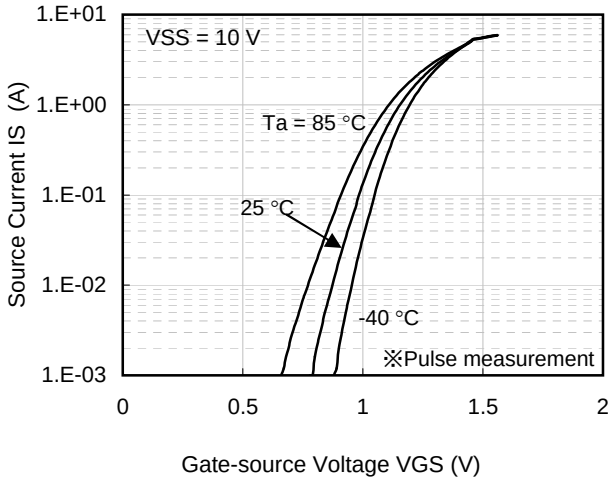
IS - VSS



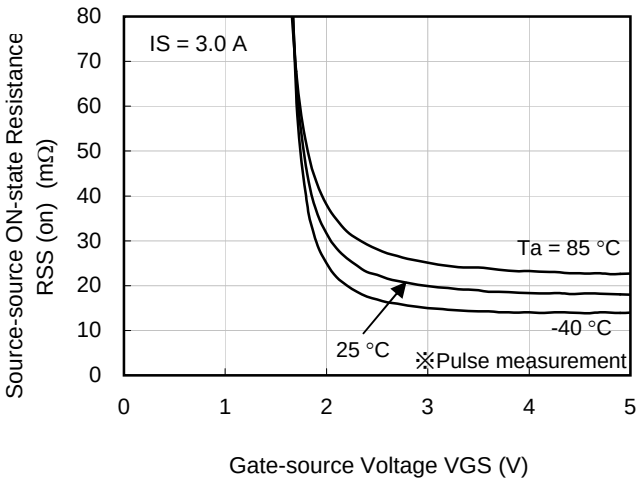
RSS(on) - IS



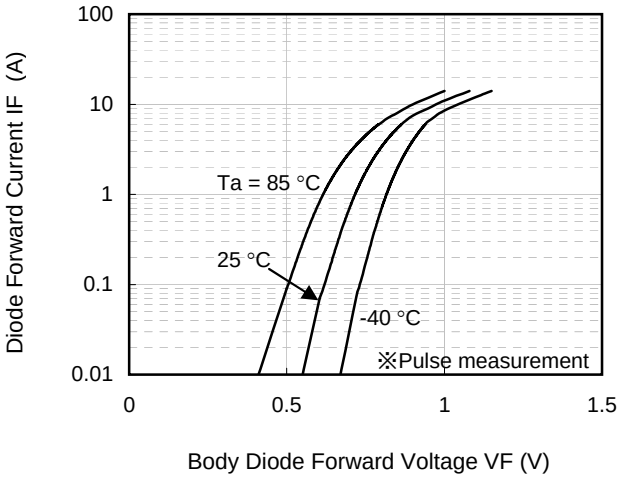
IS - VGS



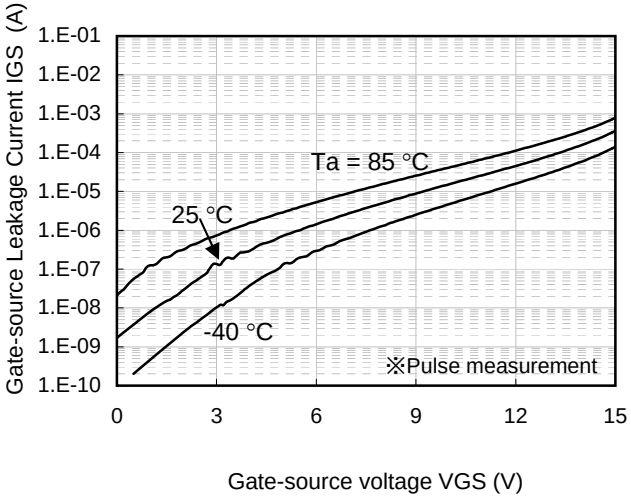
RSS(on) - VGS



IF - VF

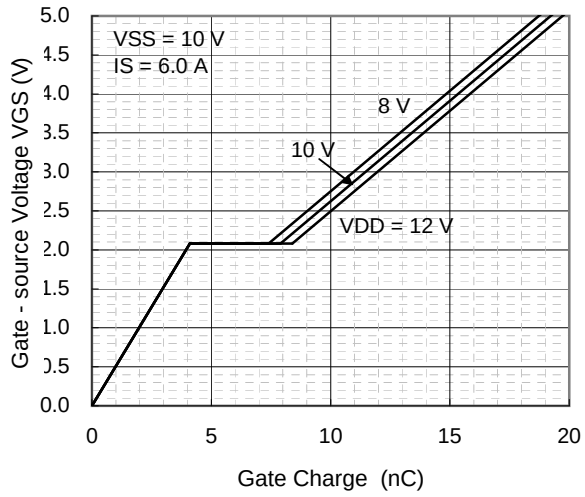


IGS - VGS

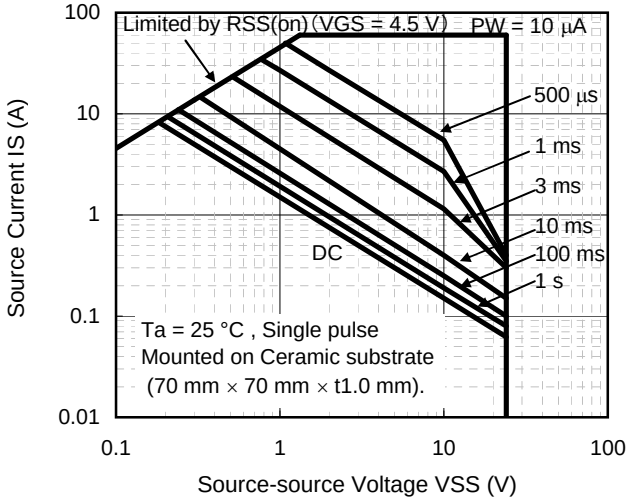


Technical Data (reference)

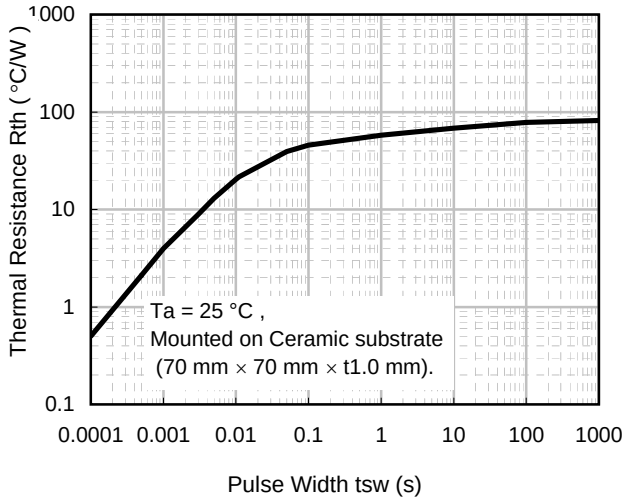
Dynamic Input/Output Characteristics



Safe Operating Area

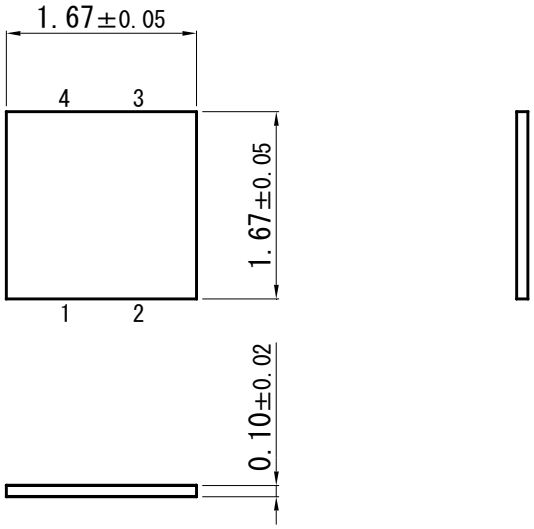


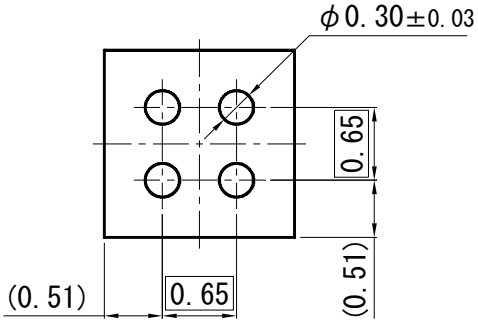
Rth - tsw



MLGA004-W-1717-RA

Unit: mm





■ Land Pattern (Reference) (Unit: mm)