CSD87501L 30V 双路共漏极 N 沟道 NexFET™功率金属氧化物半导体场效应晶体管 (MOSFET)

1 特性

- 低导通电阻
- 3.37mm × 1.47mm 的小尺寸
- 超薄 – 高 0.2mm
- 无铅
- 符合 RoHS
- 无卤素
- 栅极 ESD 保护

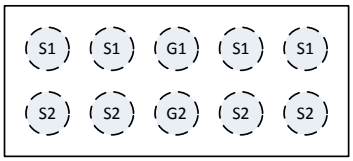
2 应用

- 电池管理
- 电池保护
- USB Type-C/PD

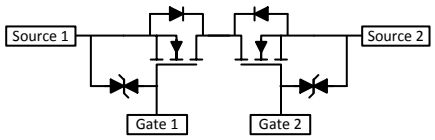
3 说明

此 30V、6.6mΩ、3.37mm × 1.47mm LGA 双路 NexFET™功率 MOSFET 旨在以小外形封装最大程度地降低电阻和栅极电荷。该器件具有小尺寸和共漏极配置，非常适用于多节电池组 应用 和小型手持设备。

俯视图



配置



产品概要

T_A = 25°C		典型值		单位
V_{S1S2}	源源电压	30		V
Q_g	总栅极电荷 (4.5V)	15		nC
Q_{gd}	栅极电荷（栅极到漏极）	6.0		nC
$R_{S1S2(on)}$	源源导通电阻	V_{GS} = 4.5V	9.3	mΩ
		V_{GS} = 10V	6.6	
$V_{GS(th)}$	阈值电压	1.8		V

器件信息(1)

器件	介质	数量	封装	配送
CSD87501L	7 英寸卷带	3000	3.37mm × 1.47mm 基板栅格阵列 封装	卷带 封装
CSD87501LT	7 英寸卷带	250		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

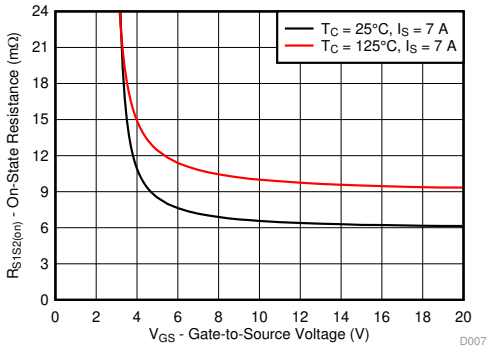
绝对最大额定值

T_A = 25°C		值	单位
V_{S1S2}	源源电压	30	V
V_{GS}	栅源电压	±20	V
I_S	持续源极电流(1)	14	A
I_{SM}	脉冲源极电流(2)	72	A
P_D	功率耗散	2.5	W
$V_{(ESD)}$	人体放电模型 (HBM)	2	kV
T_J、T_{stg}	工作结温、贮存温度	–55 至 150	°C

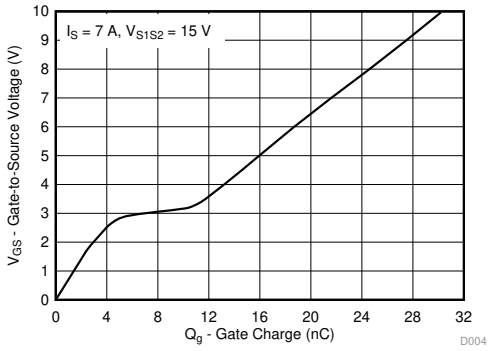
(1) $R_{\theta JA}$ = 50°C/W，这是在 0.06 英寸厚 FR4 PCB 上的 1 平方英寸、2oz 铜焊盘上测得的典型值。

(2) $R_{\theta JA}$ = 135°C/W（覆铜面积最小时的典型值），脉冲持续时间 ≤ 100µs，占空比 ≤ 1%。

$R_{S1S2(on)}$ 与 V_{GS} 间的关系



栅极电荷



目录

4 修订历史记录

Changes from Revision A (April 2015) to Revision B **Page**

- 已添加 添加了*接收文档更新通知* 部分和*社区资源* 部分 7
- 已添加 在*机械、封装和可订购信息* 部分添加了“引脚配置”表 8

Changes from Original (February 2015) to Revision A **Page**

- Extended Y axis in Figure 9 down to 0.01 A 4

5 Specifications

5.1 Electrical Characteristics

T_A = 25°C unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{S1S2}	Source-to-source voltage	V_{GS} = 0 V, I_S = 250 µA	30			V
I_{S1S2}	Source-to-source leakage current	V_{GS} = 0 V, V_{S1S2} = 24 V			1	µA
I_{GSS}	Gate-to-source leakage current	V_{S1S2} = 0 V, V_{GS} = 20 V			10	µA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{S1S2} = V_{GS}, I_S = 250 µA	1.3	1.8	2.3	V
$R_{S1S2(on)}$	Source-to-source on-resistance	V_{GS} = 4.5 V, I_S = 7 A		9.3	11.0	mΩ
		V_{GS} = 10 V, I_S = 7 A		6.6	7.8	
g_{fs}	Transconductance	V_{S1S2} = 3 V, I_S = 7 A		48		S
DYNAMIC CHARACTERISTICS(1)						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{S1S2} = 15 V, f = 1 MHz		1620	2110	pF
C_{oss}	Output capacitance			189	246	pF
C_{rss}	Reverse transfer capacitance			152	198	pF
R_G	Series gate resistance			300	450	Ω
Q_g	Gate charge total (4.5 V)	V_{S1S2} = 15 V, I_S = 7 A		15	20	nC
Q_g	Gate charge total (10 V)			31	40	nC
Q_{gd}	Gate charge gate-to-drain			6.0		nC
Q_{gs}	Gate charge gate-to-source			5.0		nC
$Q_{g(th)}$	Gate charge at V_{th}			2.5		nC
Q_{oss}	Output charge	V_{S1S2} = 15 V, V_{GS} = 0 V		7.6		nC
$t_{d(on)}$	Turn on delay time	V_{S1S2} = 15 V, V_{GS} = 10 V, I_{S1S2} = 7 A, R_G = 0 Ω		164		ns
t_r	Rise time			260		ns
$t_{d(off)}$	Turn off delay time			709		ns
t_f	Fall time			712		ns

(1) Dynamic characteristics values specified are per single FET.

5.2 Thermal Information

T_A = 25°C unless otherwise stated

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)		135		°C/W
	Junction-to-ambient thermal resistance(2)		50		

(1) Device mounted on FR4 material with minimum Cu mounting area.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C unless otherwise stated

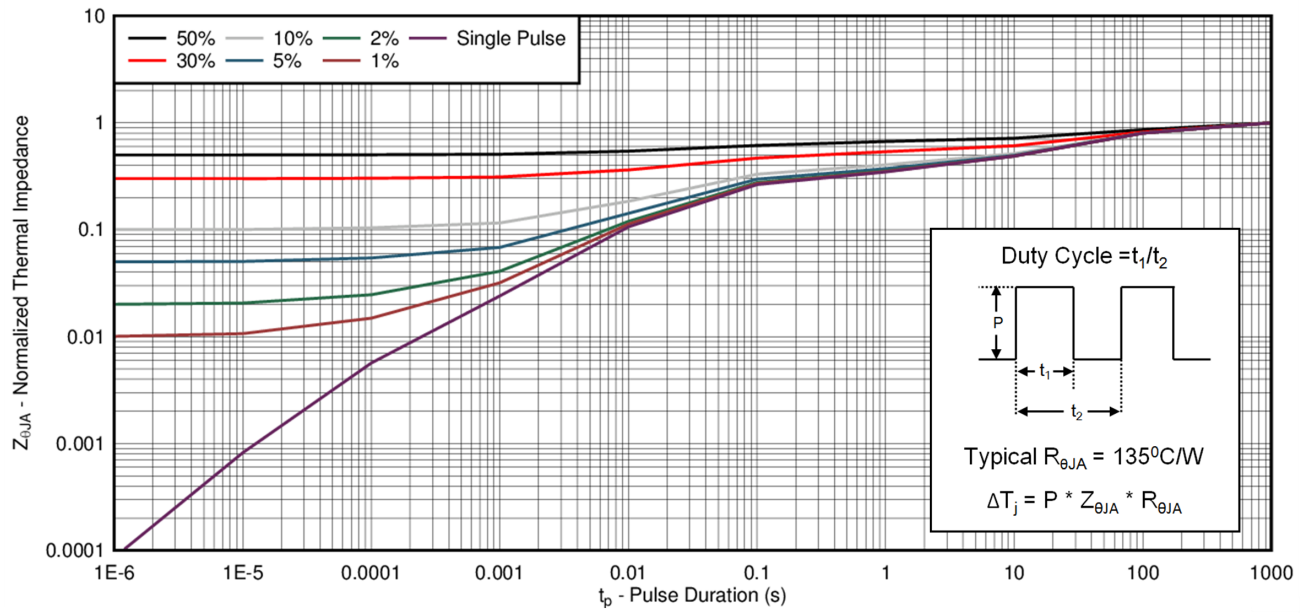


Figure 1. Transient Thermal Impedance

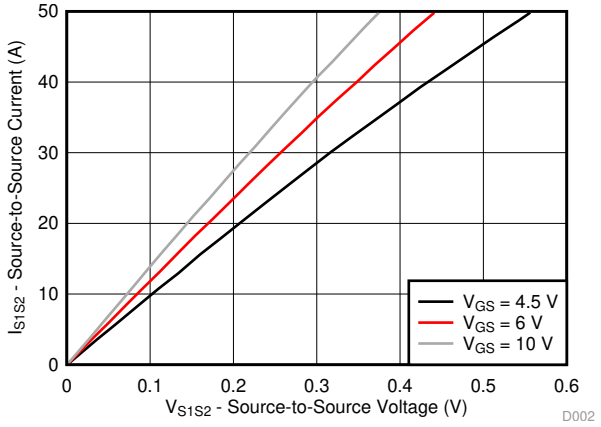


Figure 2. Saturation Characteristics

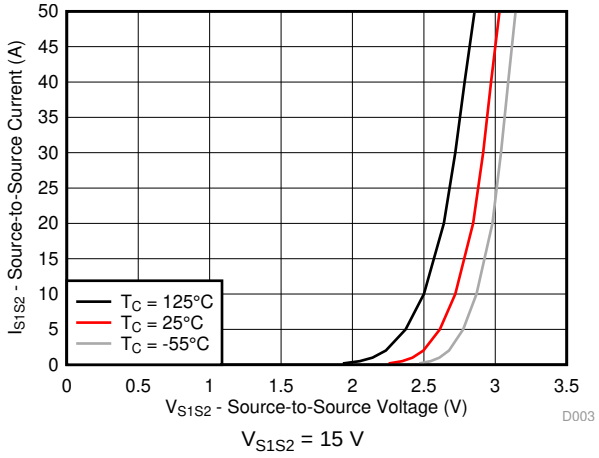


Figure 3. Transfer Characteristics

Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated

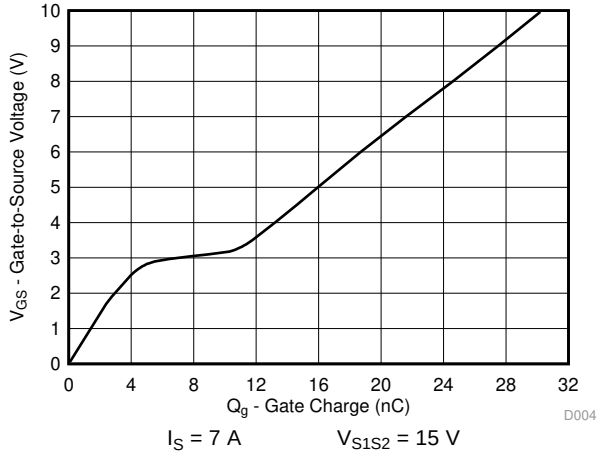


Figure 4. Gate Charge

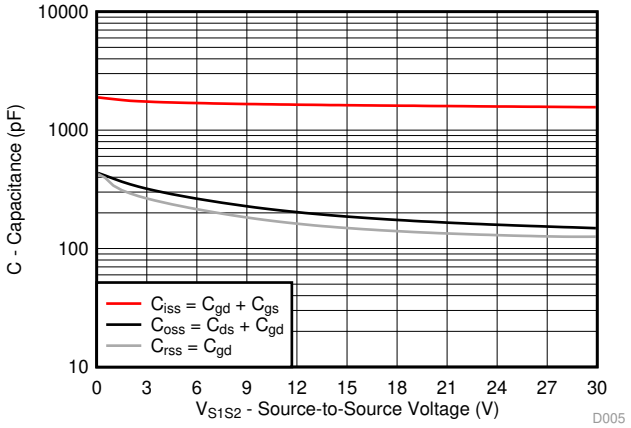


Figure 5. Capacitance

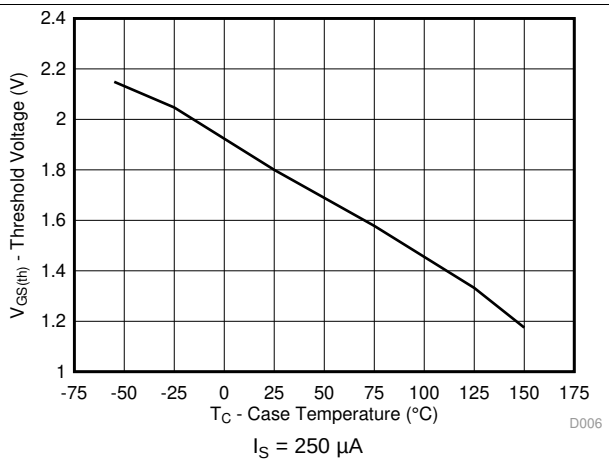


Figure 6. Threshold Voltage vs Temperature

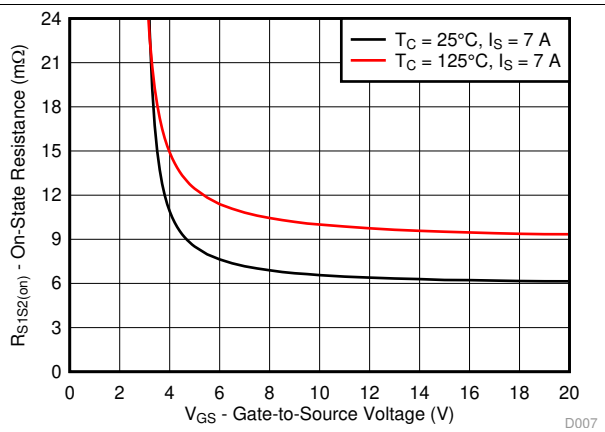


Figure 7. On-State Source-to-Source Resistance vs Gate-to-Source Voltage

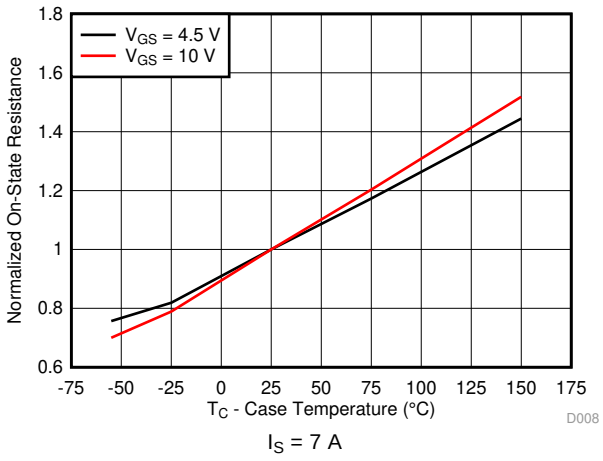


Figure 8. Normalized On-State Resistance vs Temperature

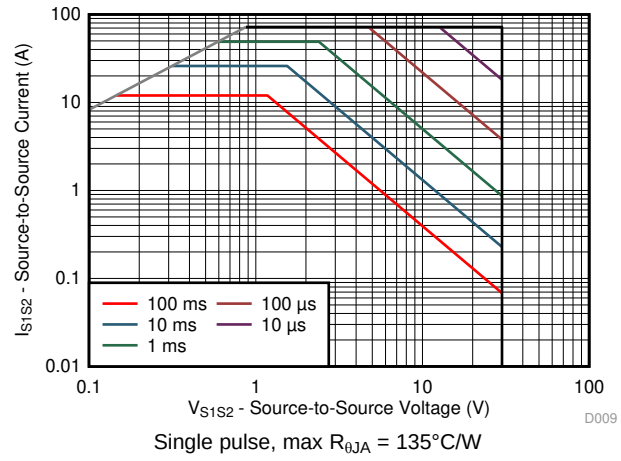


Figure 9. Maximum Safe Operating Area

Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated

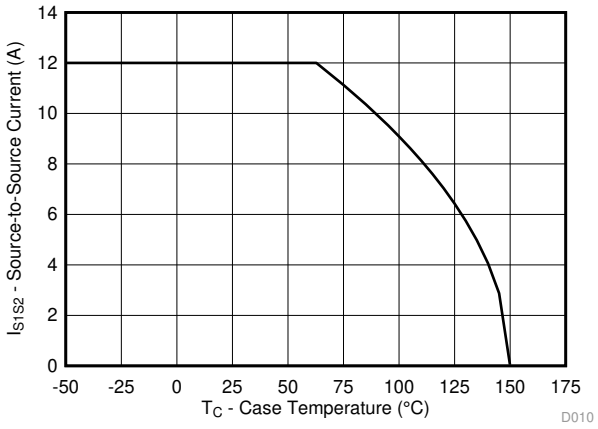


Figure 10. Maximum Source Current vs Temperature

6 器件和文档支持

6.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 商标

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

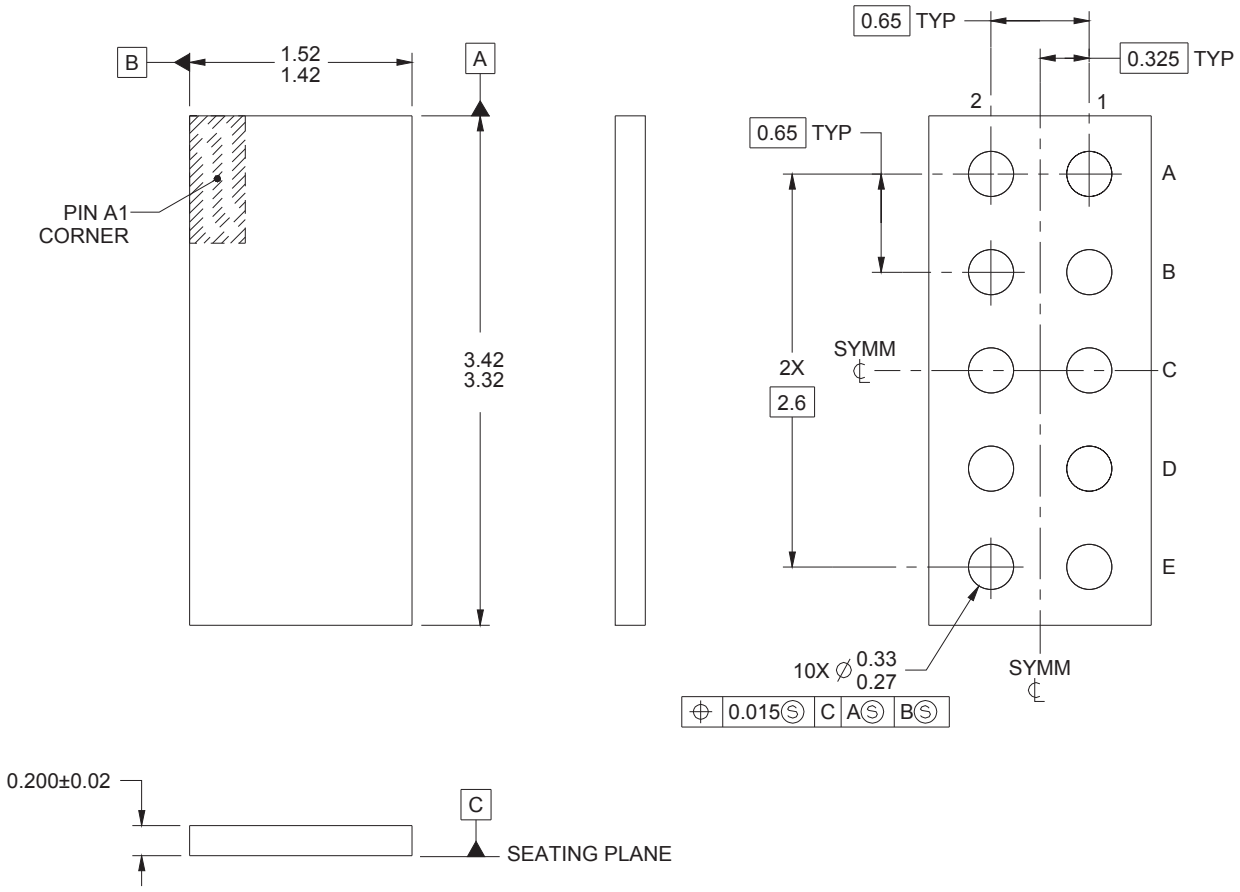
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

7.1 封装尺寸

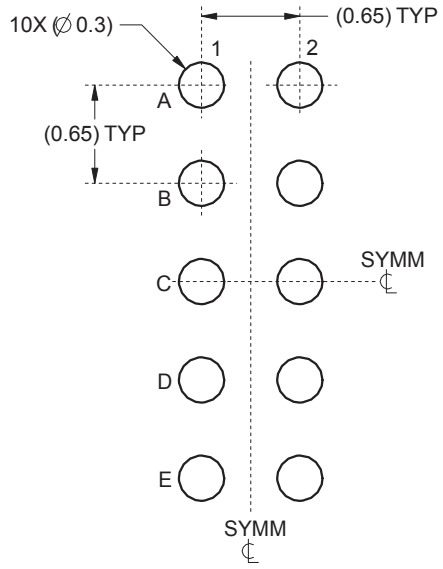


所有尺寸均以毫米为单位。

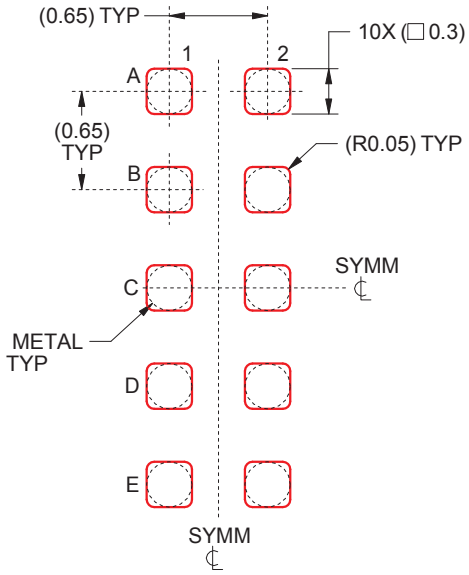
表 **1.** 引脚配置

位置	名称
A1、B1、D1、E1	源极 1
C1	栅极 1
A2、B2、D2、E2	源极 2
C2	栅极 2

7.2 推荐的 PCB 布局



7.3 推荐的模板布局



所有尺寸均以毫米为单位（除非另外注明）。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD87501L	ACTIVE	PICOSTAR	YJG	10	3000	RoHS & Green	NIAU	Level-1-260C-UNLIM		CSD87501	Samples
CSD87501LT	ACTIVE	PICOSTAR	YJG	10	250	RoHS & Green	NIAU	Level-1-260C-UNLIM	-55 to 150	CSD87501	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

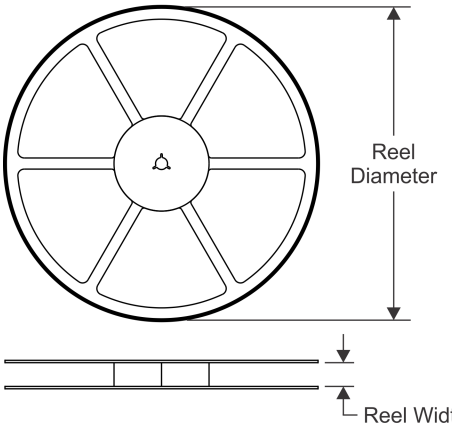
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

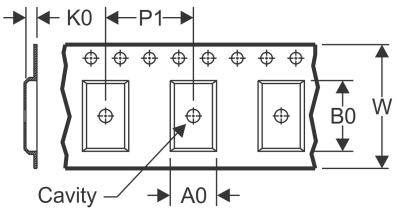
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

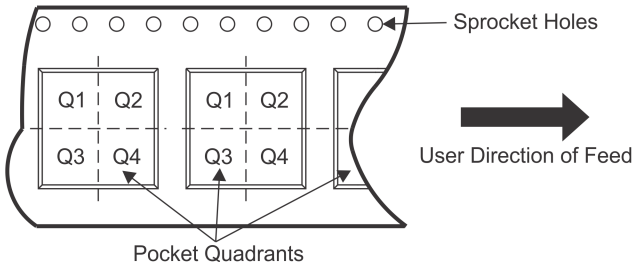


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



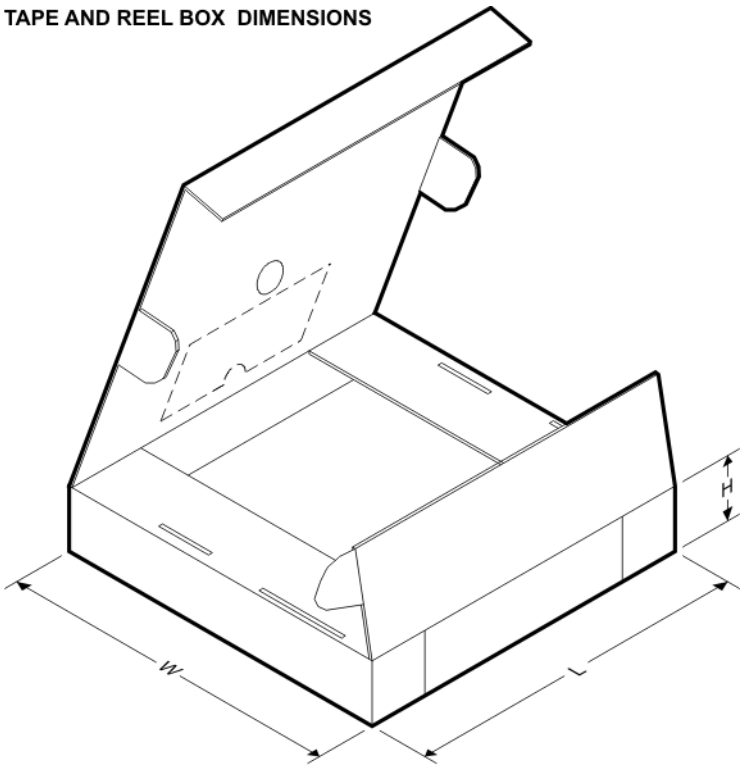
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD87501L	PICOSTAR	YJG	10	3000	178.0	13.4	1.62	3.62	0.37	8.0	12.0	Q1
CSD87501LT	PICOSTAR	YJG	10	250	178.0	13.4	1.62	3.62	0.37	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

18-Jan-2020

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD87501L	PICOSTAR	YJG	10	3000	220.0	220.0	35.0
CSD87501LT	PICOSTAR	YJG	10	250	220.0	220.0	35.0