

EFC4612R

N-Channel Power MOSFET 24V, 6A, 45mΩ, Dual EFCP

Features

- 2.5V drive
- Built-in gate protection resistor
- Best suited for LiB charging and discharging switch
- Common-drain type
- Halogen free compliance

Specifications

Absolute Maximum Ratings at Ta=25°C

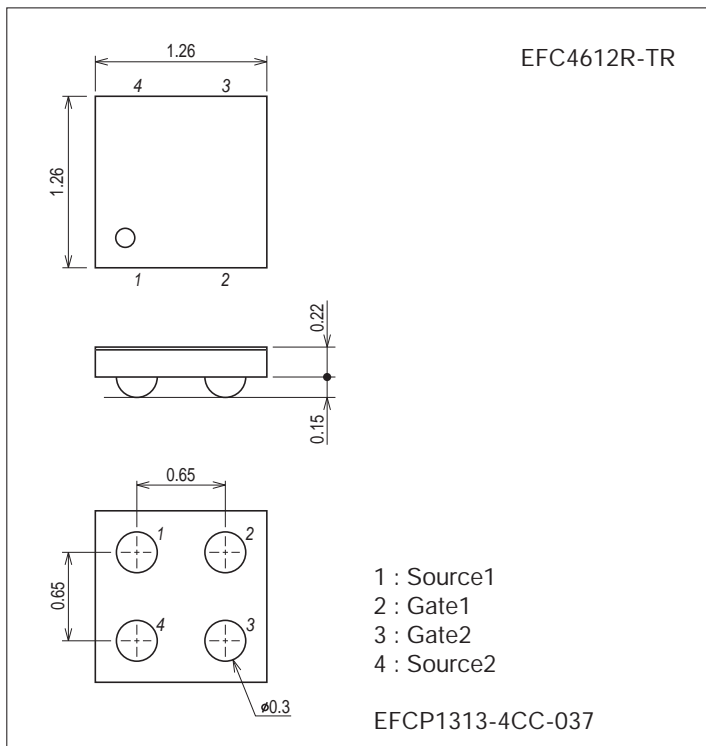
Parameter	Symbol	Conditions	Ratings	Unit
Source-to-Source Voltage	V _{SSS}		24	V
Gate-to-Source Voltage	V _{GSS}		±12	V
Source Current (DC)	I _S		6	A
Source Current (Pulse)	I _{SP}	PW≤10μs, duty cycle≤1%	60	A
Total Dissipation	P _T	When mounted on ceramic substrate (5000mm ² ×0.8mm)	1.6	W
Channel Temperature	T _{ch}		150	°C
Storage Temperature	T _{stg}		-55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

unit : mm (typ)

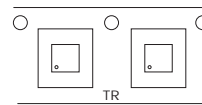
7064-001



Product & Package Information

- Package : EFCP
- JEITA, JEDEC : -
- Minimum Packing Quantity : 5,000 pcs./reel

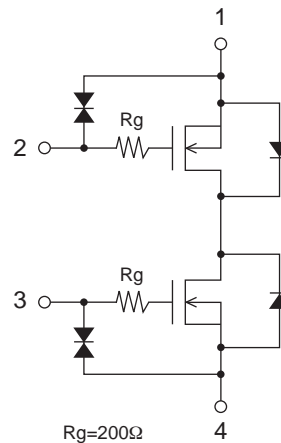
Taping Type : TR



Marking



Electrical Connection



EFC4612R

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Source-to-Source Breakdown Voltage	V(BR)SSS	IS=1mA, VGS=0V Test Circuit 1	24			V
Zero-Gate Voltage Source Current	ISSS	VSS=20V, VGS=0V Test Circuit 1			1	μA
Gate-to-Source Leakage Current	IGSS	VGS=±8V, VSS=0V Test Circuit 2			±10	μA
Cutoff Voltage	VGS(off)	VSS=10V, IS=1mA Test Circuit 3	0.5		1.3	V
Forward Transfer Admittance	yfs	VSS=10V, IS=3A Test Circuit 4		3.1		S
Static Source-to-Source On-State Resistance	RSS(on)1	IS=3A, VGS=4.5V Test Circuit 5	24	39	45	mΩ
	RSS(on)2	IS=3A, VGS=4.0V Test Circuit 5	25	41	48	mΩ
	RSS(on)3	IS=3A, VGS=3.7V Test Circuit 5	27.5	43	50	mΩ
	RSS(on)4	IS=3A, VGS=3.1V Test Circuit 5	31.5	48	57	mΩ
	RSS(on)5	IS=3A, VGS=2.5V Test Circuit 5	33.5	58	72	mΩ
Turn-ON Delay Time	td(on)	See specified Test Circuit. Test Circuit 7		20		ns
Rise Time	tr			230		ns
Turn-OFF Delay Time	td(off)			130		ns
Fall Time	tf			210		ns
Total Gate Charge	Qg		VSS=10V, VGS=4.5V, IS=6A		7	
Forward Source-to-Source Voltage	VF(S-S)	IS=3A, VGS=0V Test Circuit 6		0.8	1.2	V

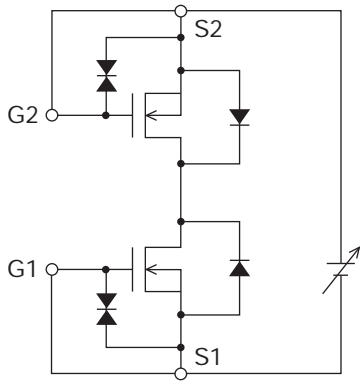
Ordering Information

Device	Package	Shipping	memo
EFC4612R-TR	EFCP	5,000pcs./reel	Pb Free and Halogen Free

Test circuits are example of measuring FET1 side

Test Circuit 1

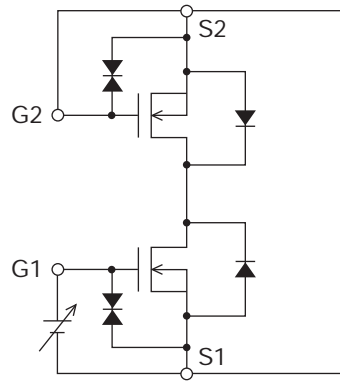
V_{SSS} / I_{SSS}



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Test Circuit 2

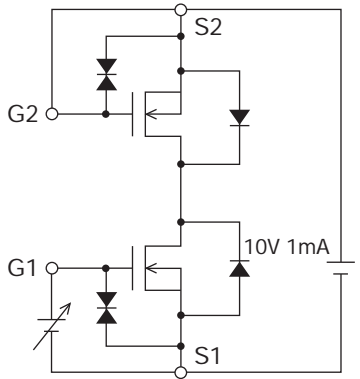
$I_{GSS(+)} / (-)$



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Test Circuit 3

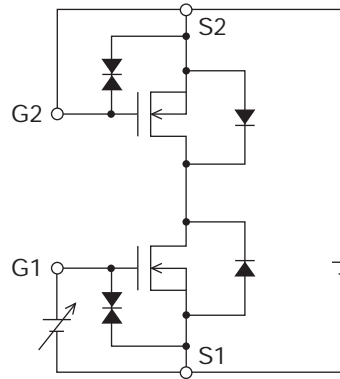
$V_{GS(off)}$



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Test Circuit 4

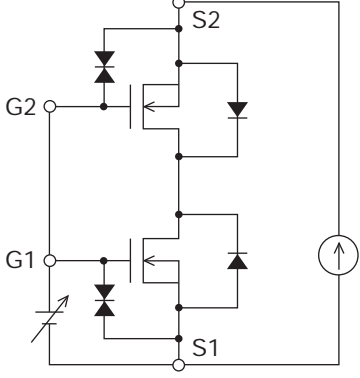
$|y_{fs}|$



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Test Circuit 5

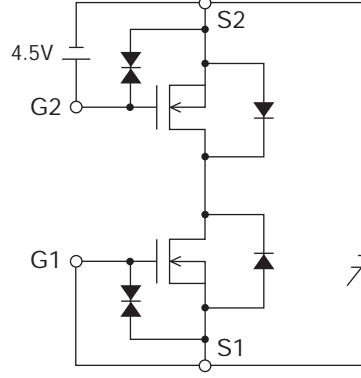
$R_{SS(on)}$



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Test Circuit 6

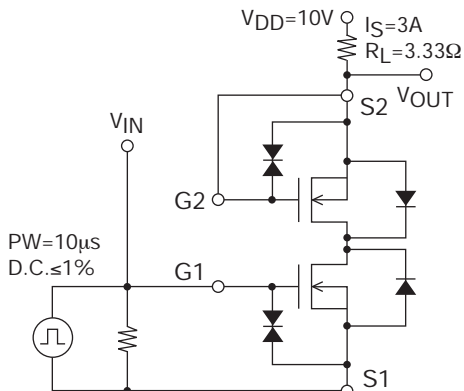
$V_{F(S-S)}$



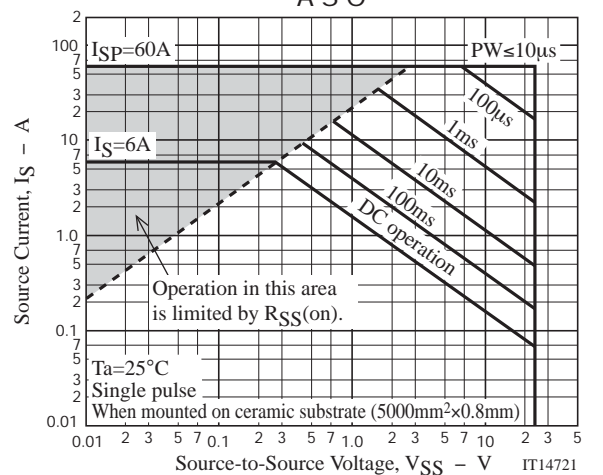
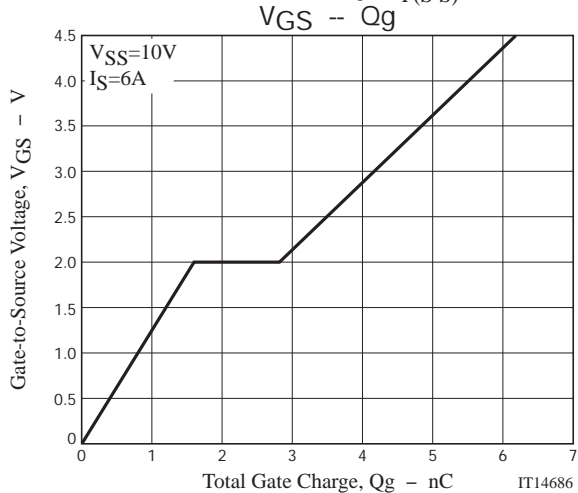
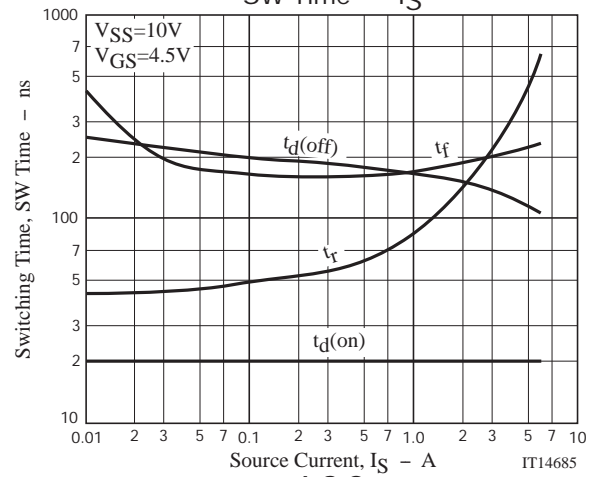
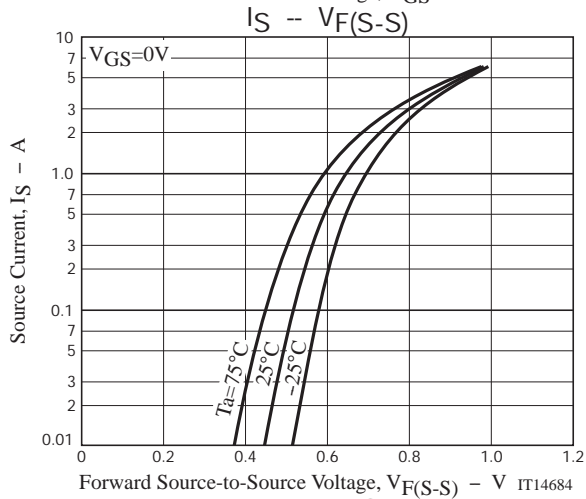
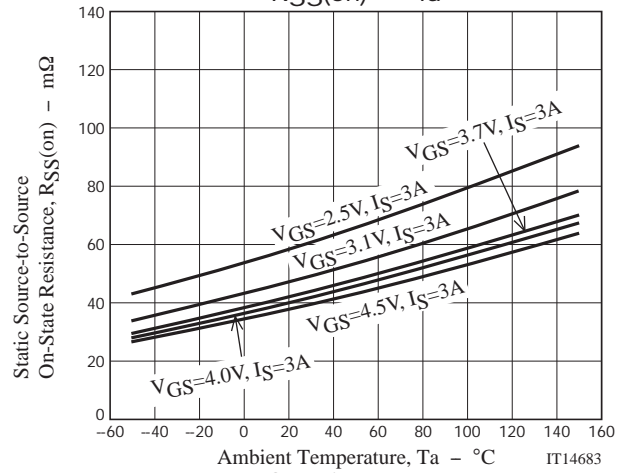
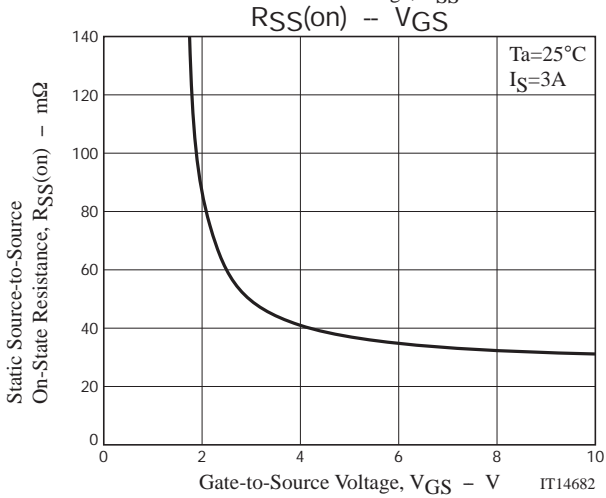
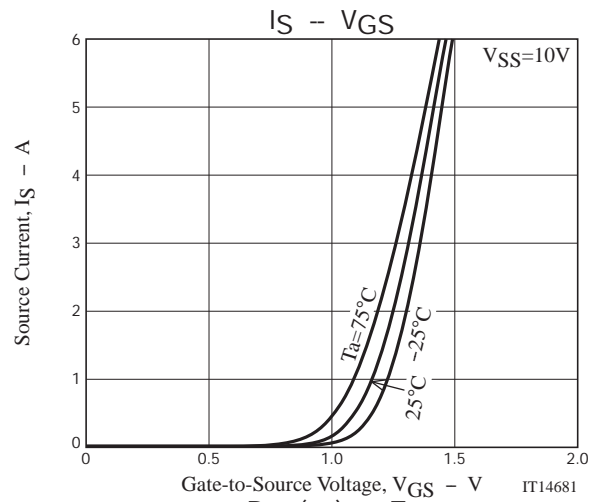
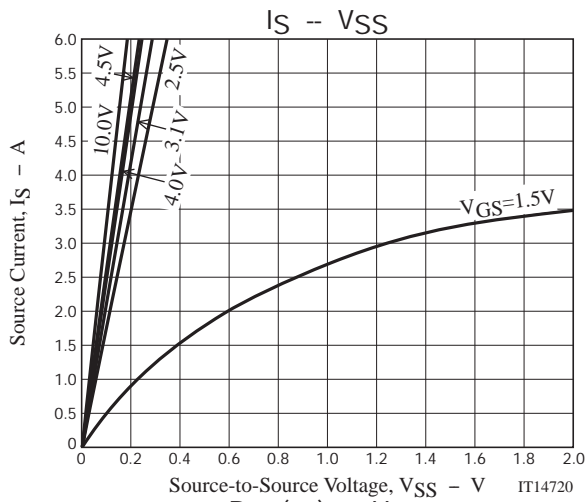
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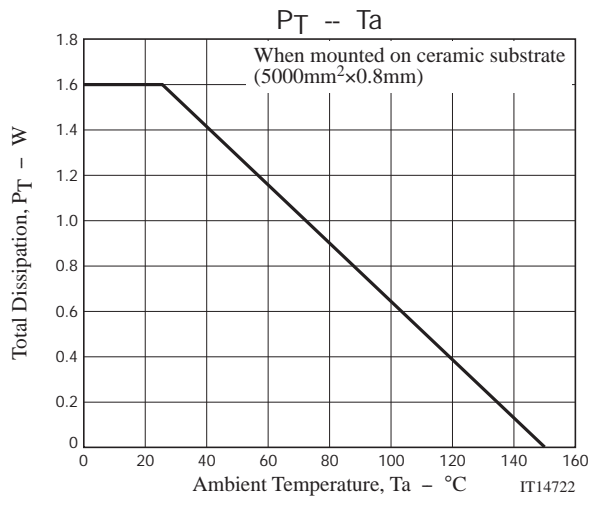
Test Circuit 7

$t_{d(on)}, t_r, t_{d(off)}, t_f$



* Note: Connect the measurement terminal reversely if you want to measure the FET2 side.





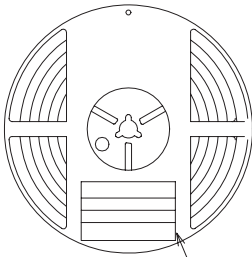
Taping Specification

EFC4612R-TR

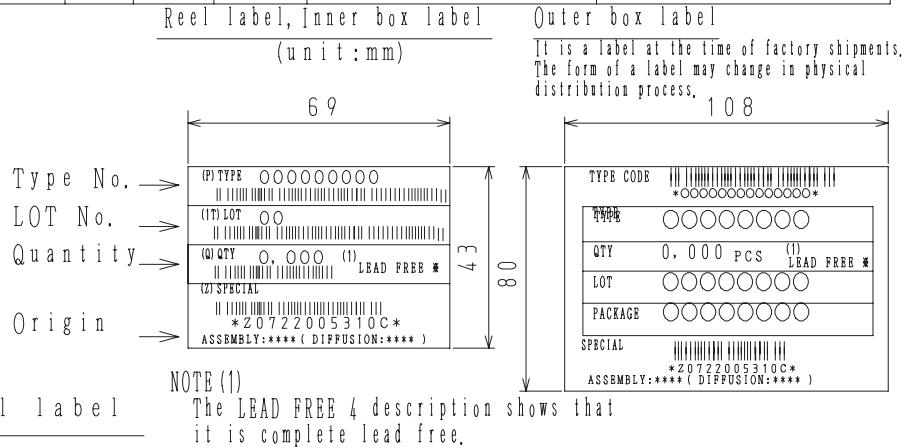
1. Packing Format

Package Name	Carrier Tape Type	Maximum Number of devices contained (pcs)			Packing format	
		Reel	Inner box	Outer box	Inner BOX (C-1)	Outer BOX (A-7)
EFCP1313 -4CC-037	145145×055	5,000	25,000	150,000	5 reels contained Dimensions:mm (external) 183×72×185	6 inner boxes contained Dimensions:mm (external) 440×195×210

Packing method



Reel label

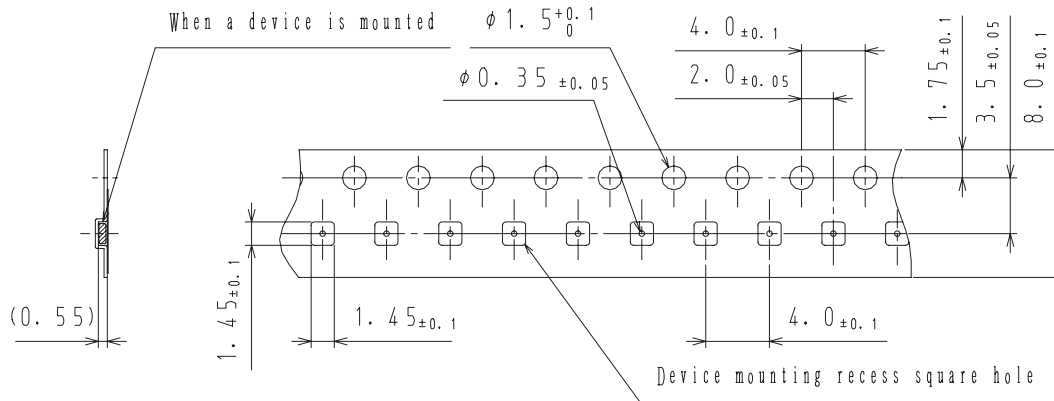


NOTE (1)
The LEAD FREE 4 description shows that it is complete lead free.

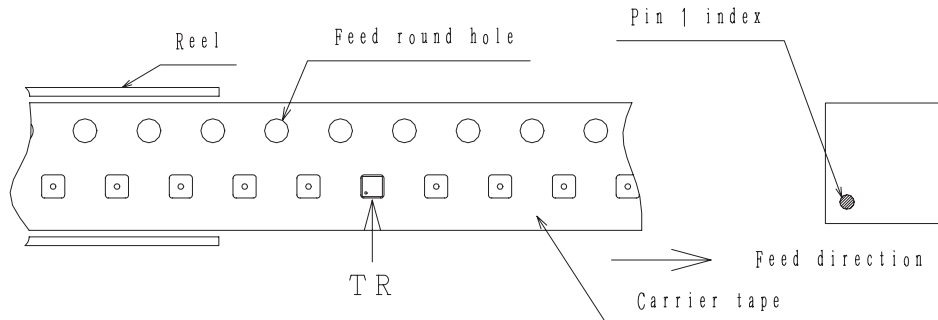
Label	JEITA Phase
LEAD FREE 4	JEITA Phase 3

2. Taping configuration

2-1. Carrier tape size (unit:mm)



2-2. Device placement direction

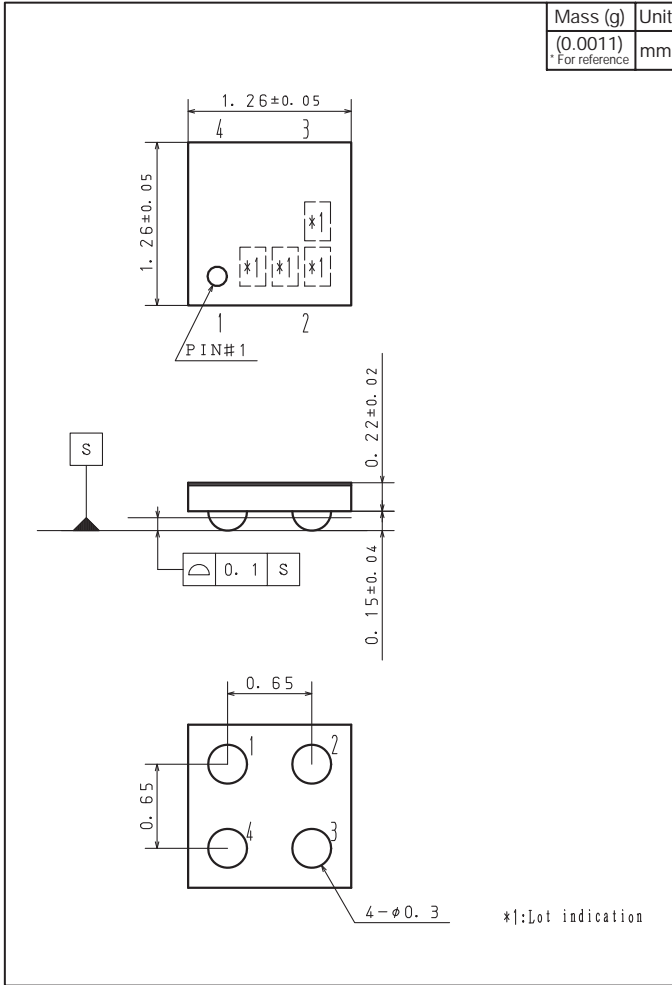


Those with pin 1 index on the opposite of feed hole.....TR

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Outline Drawing

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Land Pattern Example

