

INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

INN040W048A

1. General Description

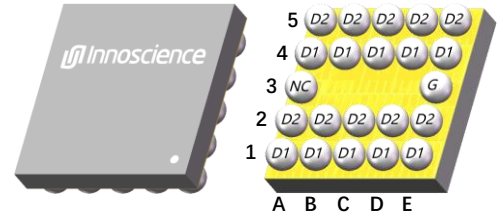
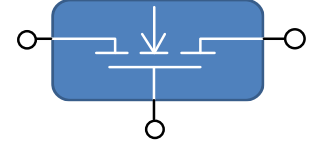
Bi-directional GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in WLCSP with 2.1 mm x 2.1 mm package size.

2. Features

- Bi-directional blocking capability
- GaN-on-Silicon E-mode HEMT technology
- Ultra-low on resistance

3. Applications

- High side load switch
- OVP protection in smart phone USB port
- Switch circuits in multiple power suppliers system



4. Key Performance Parameters

Table 1 Key performance parameters at $T_J = 25\text{ }^\circ\text{C}$

Parameter	Value	Unit
$V_{DD,max}$	40	V
$R_{D1D2(on),max}$ @ $V_G = 5\text{ V}$	4.8	m Ω
$Q_{G,typ}$ @ $V_{DD} = 20\text{ V}$	15.8	nC
$I_{D,DC}$	20	A

5. Pin Information

Table 2 Pin information

Pin	Pin description	Pin function
A~E1, A~E4	Drain1	Power Drain1
A~E2, A~E5	Drain2	Power Drain2
E3	Gate	Driver Gate
A3	Not Connected	Dummy Pin

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN040W048A	WLCSP 2.1x2.1	D12

INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

Table of contents

1. General Description	1
2. Features	1
3. Applications	1
4. Key Performance Parameters	1
5. Pin Information	1
6. Maximum Ratings	3
7. Thermal Characteristics	4
8. Electric Characteristics	5
9. Electric Characteristics Diagrams	7
10. Package Outlines	12
11. Reel Information	13
12. Land Pattern	14
13. Revision History	15

INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

6. Maximum Ratings

at $T_J = 25\text{ °C}$ unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DD}	Drain1-to-Drain2 Voltage or Drain2-to-Drain1 Voltage	40	V
V_{DG}	Drain-to-Gate Voltage	40	V
V_{GD}	Gate-to-Drain Voltage	6	V
I_D	Continuous Drain current	20	A
I_{DM}	Pulsed Drain Current (25 °C , $T_{Pulse} = 300\text{ }\mu\text{s}$)	100	A
P_{tot}	Power dissipation ($T_{c, bottom} = 25\text{ °C}$)	13	W
T_J	Operating Temperature	-40 to 125	°C
T_{STG}	Storage Temperature	-40 to 150	°C

INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

7. Thermal Characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT
$R_{\theta JC_top}$	Thermal Resistance, Junction to Case (top)	12.6	$^{\circ}C/W$
$R_{\theta JC_bot}$	Thermal Resistance, Junction to Case (bottom)	7.6	$^{\circ}C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ¹	59.3	$^{\circ}C/W$

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

8. Electric Characteristics

at $T_J = 25\text{ }^\circ\text{C}$, unless specified otherwise

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
BV_{D1D2S}	Drain1-to-Drain2 Breakdown Voltage	40			V	$V_{D2} = V_G = 0\text{ V}$, $I_{D1D2} = 500\text{ }\mu\text{A}$
BV_{D2D1S}	Drain2-to-Drain1 Breakdown Voltage	40			V	$V_{D1} = V_G = 0\text{ V}$, $I_{D2D1} = 500\text{ }\mu\text{A}$
I_{D1D2S}	Zero Gate Voltage Drain Current			20	μA	$V_{D2} = V_G = 0\text{ V}$, $V_{D1} = 40\text{ V}$
I_{D2D1S}	Zero Gate Voltage Drain Current			20	μA	$V_{D1} = V_G = 0\text{ V}$, $V_{D2} = 40\text{ V}$
I_{GDS} ($T_J = 85\text{ }^\circ\text{C}$)	Gate-to-Drain Leakage		0.5	3	μA	$V_{D1} = V_{D2} = 0\text{ V}$, $V_G = 5\text{ V}$
	Gate-to-Drain Leakage	-30			μA	$V_{D1} = V_{D2} = 0\text{ V}$, $V_G = -5\text{ V}$
I_{GDS} ($T_J = 85\text{ }^\circ\text{C}$)	Gate-to-Drain Leakage		5	30	μA	$V_{D1} = V_{D2} = 0\text{ V}$, $V_G = 6\text{ V}$
	Gate-to-Drain Leakage	-40			μA	$V_{D1} = V_{D2} = 0\text{ V}$, $V_G = -6\text{ V}$
$V_{GD1(TH)}$	Gate Threshold Voltage	0.8		2.4	V	$V_{D1} = 0\text{ V}$, $V_{D2} = V_G$, $I_{D2D1} = 1\text{ mA}$
$V_{GD2(TH)}$	Gate Threshold Voltage	0.8		2.4	V	$V_{D2} = 0\text{ V}$, $V_{D1} = V_G$, $I_{D1D2} = 1\text{ mA}$
$R_{D1D2(on)}$	Drain1-to-Drain2 On-state Resistance		4	4.8	$\text{m}\Omega$	$V_{D2} = 0\text{ V}$, $V_{GD} = 5\text{ V}$, $I_{D1D2} = 10\text{ A}$
$R_{D2D1(on)}$	Drain2-to-Drain1 On-state Resistance		4	4.8	$\text{m}\Omega$	$V_{D1} = 0\text{ V}$, $V_{GD} = 5\text{ V}$, $I_{D2D1} = 10\text{ A}$

INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

Table 7 Dynamic characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C _{ISS}	Input Capacitance		887		pF	V _G = 0 V, V _D = 20 V
C _{OSS}	Output Capacitance		381			
C _{RSS}	Reverse Transfer Capacitance		226			
R _G	Gate Resistance		4.1		Ω	f = 1 MHz
Q _G	Total Gate Charge		15.8		nC	V _D = 20 V, V _G = 5 V, I _D = 10 A
Q _{GD1}	Gate-to-Drain1 Charge (V _{D2D1} =20V)		1.9			V _{D1} = 0, V _{D2} = 20 V, I _{D2D1} = 10 A
Q _{GD1}	Gate-to-Drain1 Charge (V _{D1D2} =20V)		8.6			V _{D2} = 0, V _{D1} = 20 V, I _{D1D2} = 10 A
Q _{GD2}	Gate-to-Drain2 Charge (V _{D1D2} =20V)		1.9			V _{D2} = 0, V _{D1} = 20 V, I _{D1D2} = 10 A
Q _{GD2}	Gate-to-Drain2 Charge (V _{D2D1} =20V)		8.6			V _{D1} = 0, V _{D2} = 20 V, I _{D2D1} = 10 A
Q _{OSS}	Output Charge		12.2			V _G = 0 V, V _D = 20 V

INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

9. Electric Characteristics Diagrams

at $T_J = 25\text{ }^\circ\text{C}$, unless specified otherwise

Note: In Charts, VD1D2 can be VD2D1 with same characteristic chart due to Bi-directional feature.

Figure 1 Typical Output Characteristics ($T_J = 25\text{ }^\circ\text{C}$)

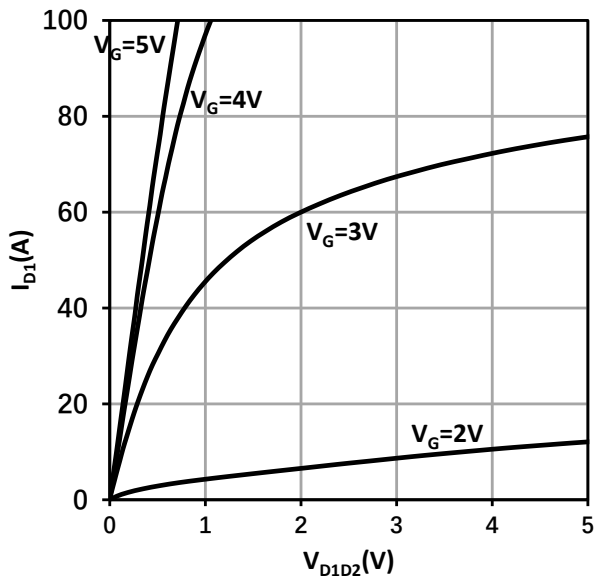


Figure 2 Typical Output Characteristics ($T_J = 125\text{ }^\circ\text{C}$)

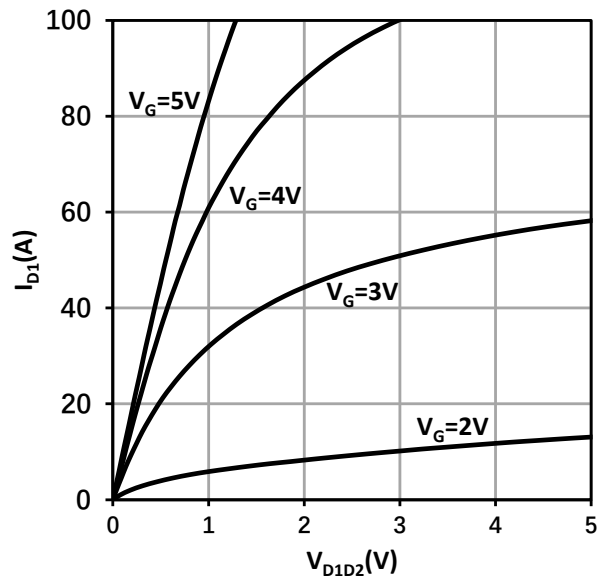


Figure 3 Typical Drain On-state Resistance ($T_J = 25\text{ }^\circ\text{C}$)

($T_J = 25\text{ }^\circ\text{C}$)

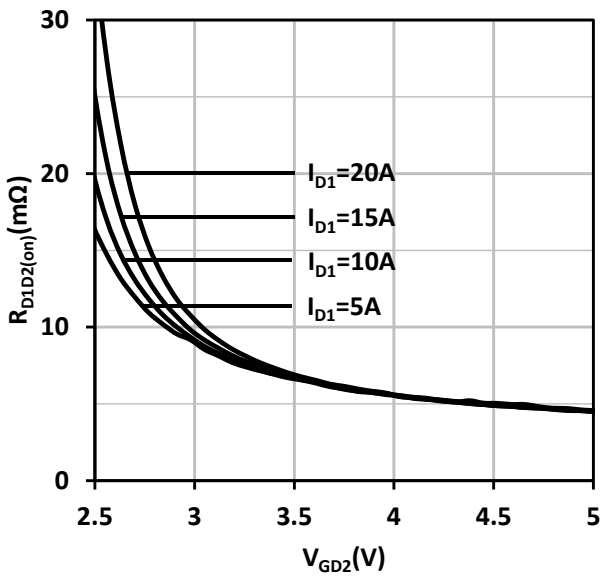
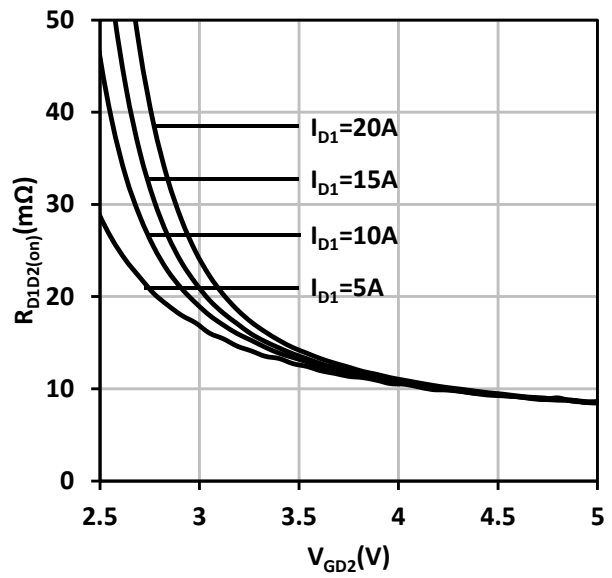


Figure 4 Typical Drain On-state Resistance ($T_J = 125\text{ }^\circ\text{C}$)

($T_J = 125\text{ }^\circ\text{C}$)



INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

Figure 5 Typical On Resistance vs. Temperature

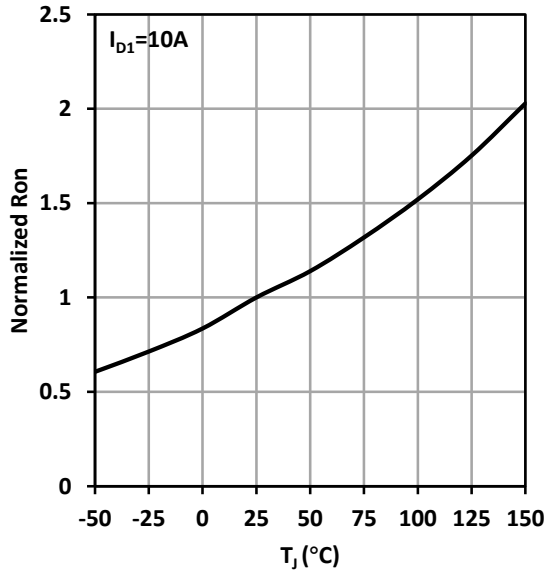


Figure 6 Typical Transfer Characteristics

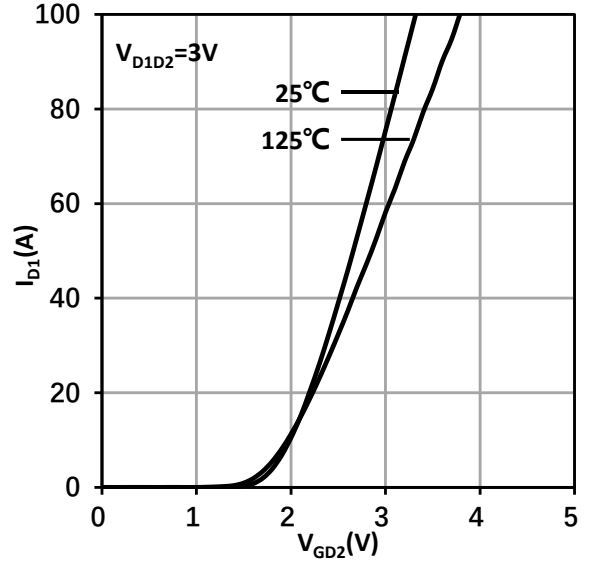


Figure 7 Typ. Reverse Drain1- Drain2 Characteristics ($V_{GD2} \leq 0V$, $T_J = 25^\circ C$)

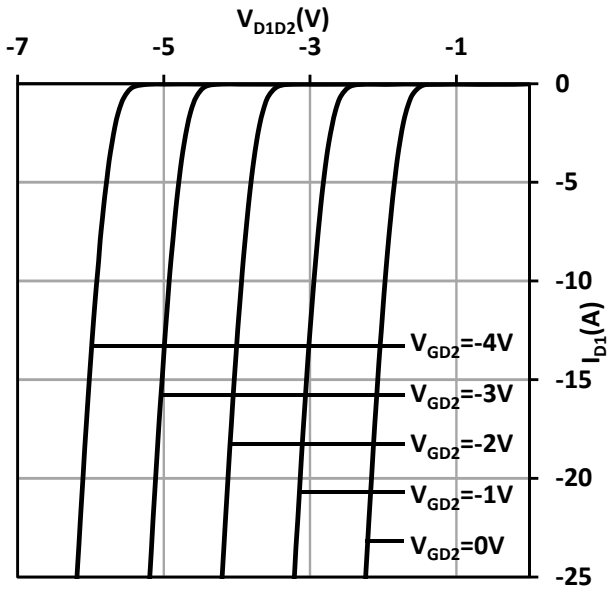
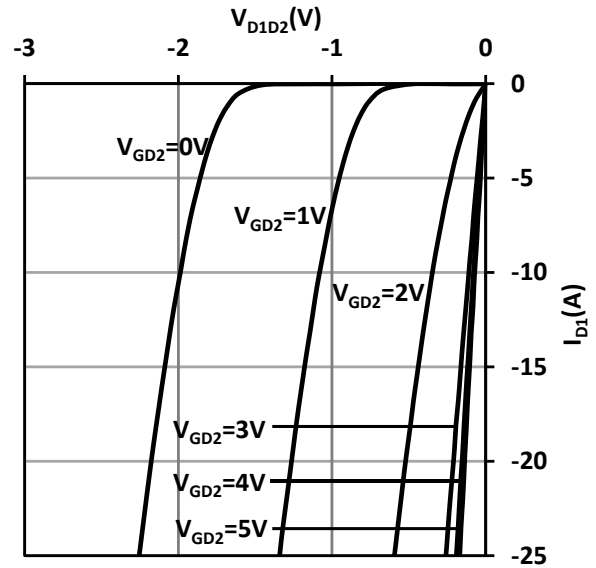


Figure 8 Typ. Reverse Drain1- Drain2 Characteristics ($V_{GD2} \geq 0V$, $T_J = 25^\circ C$)



INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

Figure 9 Typ. Reverse Drain1- Drain2 Characteristics ($V_{GD2} \leq 0V$, $T_J = 125^\circ C$)

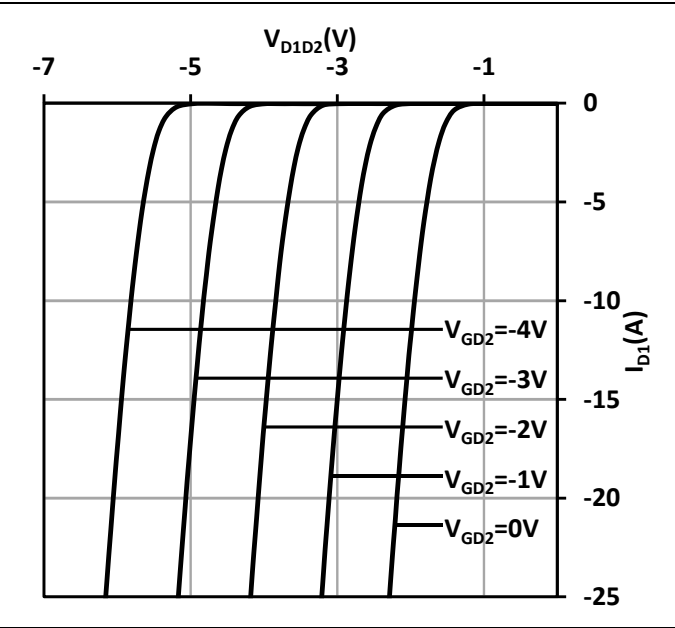


Figure 10 Typ. Reverse Drain1-Drain2 Characteristics ($V_{GD2} \geq 0V$, $T_J = 125^\circ C$)

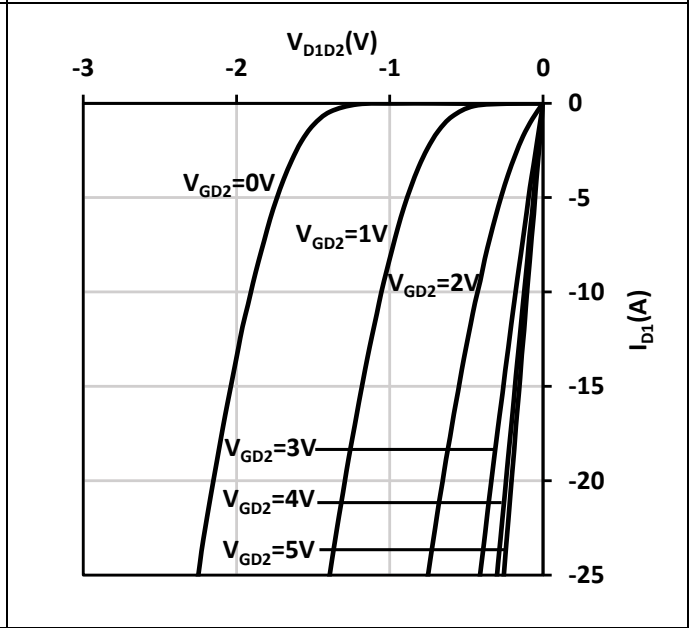


Figure 11 Typical Capacitances Characteristics

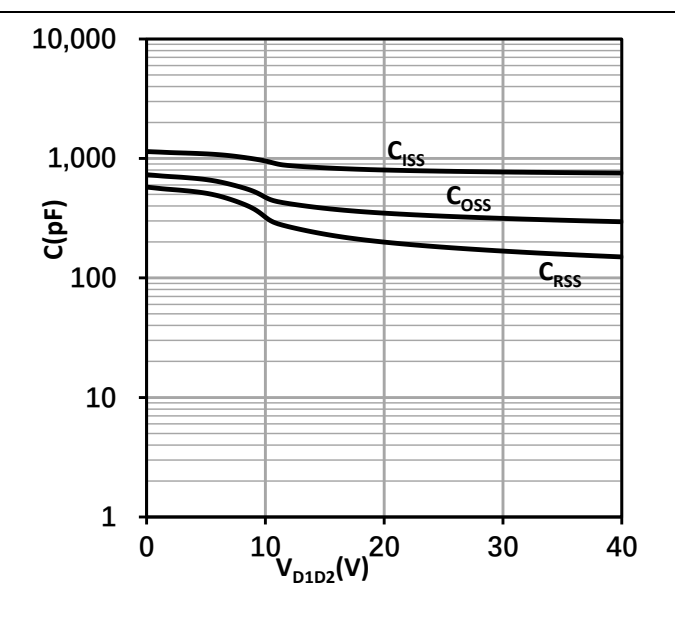
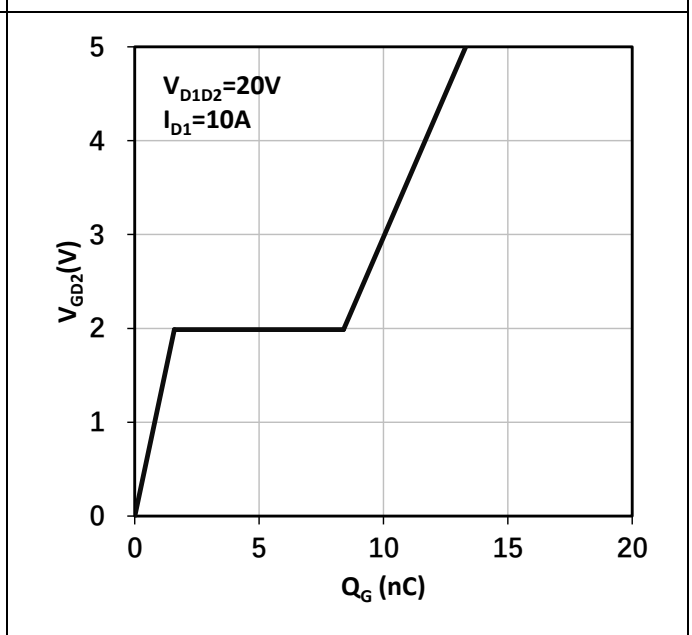


Figure 12 Typical Gate Charge



INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

Figure 13 Normalized Threshold Voltage vs. Temp.

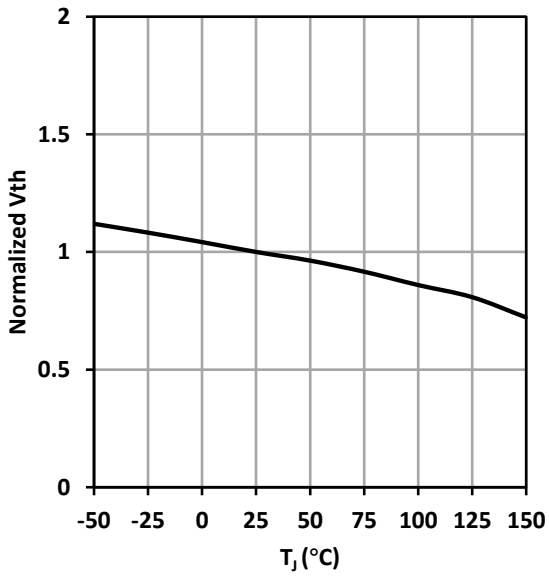


Figure 14 Output Charge

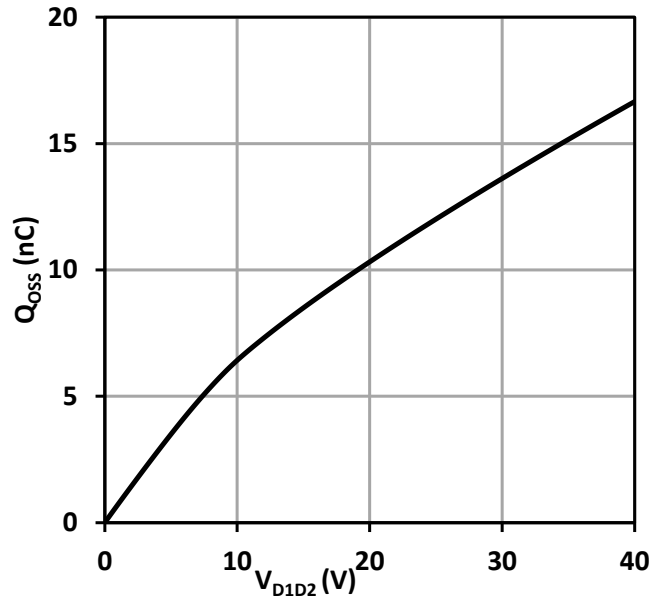


Figure 15 Output Capacitance Stored Energy

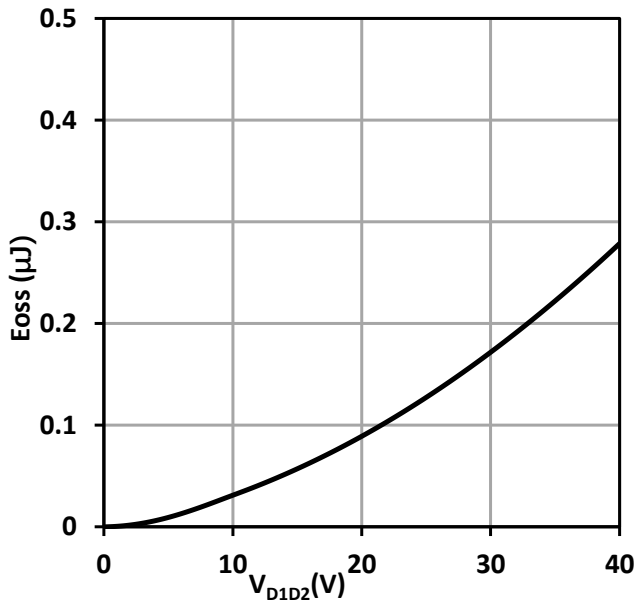
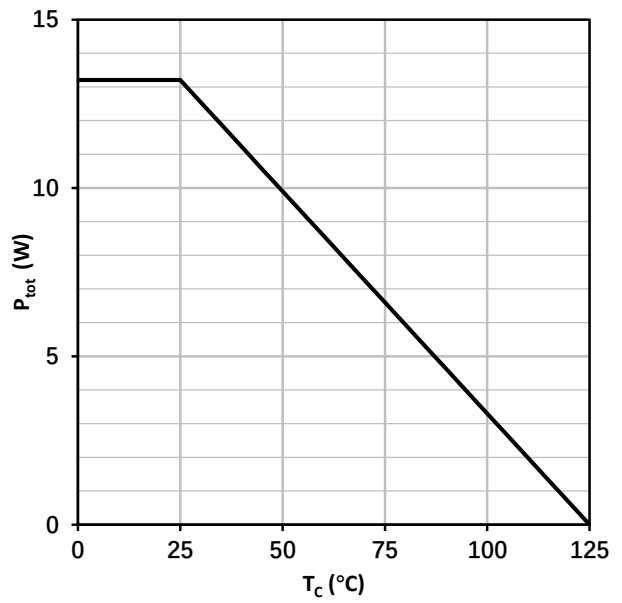


Figure 16 Power Dissipation



INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

Figure 17 Safe Operating Area

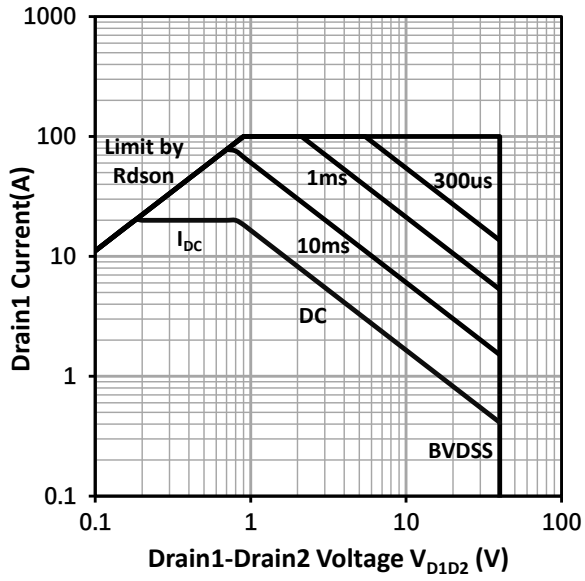
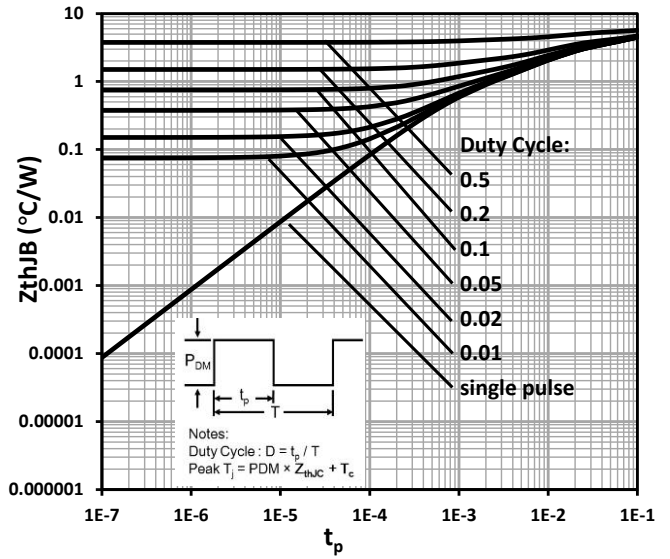


Figure 18 Max. Transient Thermal Impedance

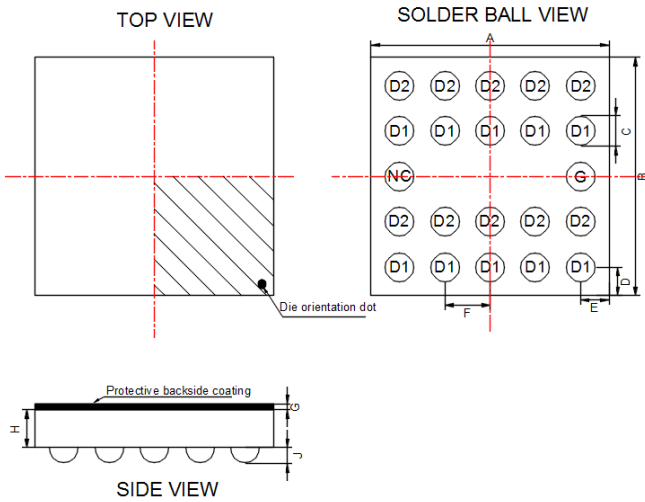


INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

10. Package Outlines

Package Reference

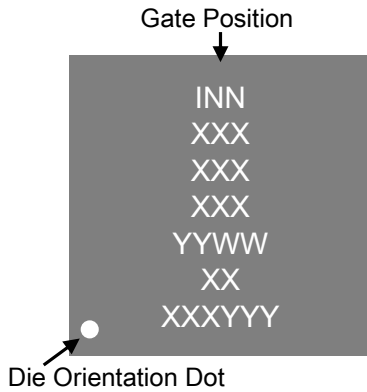


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.075	2.1	2.125
B	2.075	2.1	2.125
C	0.241	0.268	0.295
D	0.25 REF		
E	0.25 REF		
F	0.4 BASIC		
G	0.022	0.025	0.028
H	0.330	0.344	0.358
J	0.165	0.195	0.225

NOTE:

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) BALL COPLANARITY SHALL BE 0.01 MILLIMETERS MAX.
- 3) COMPLIES WITH JEDEC MO-211.
- 4) DRAWING IS NOT TO SCALE.

Marking Reference:

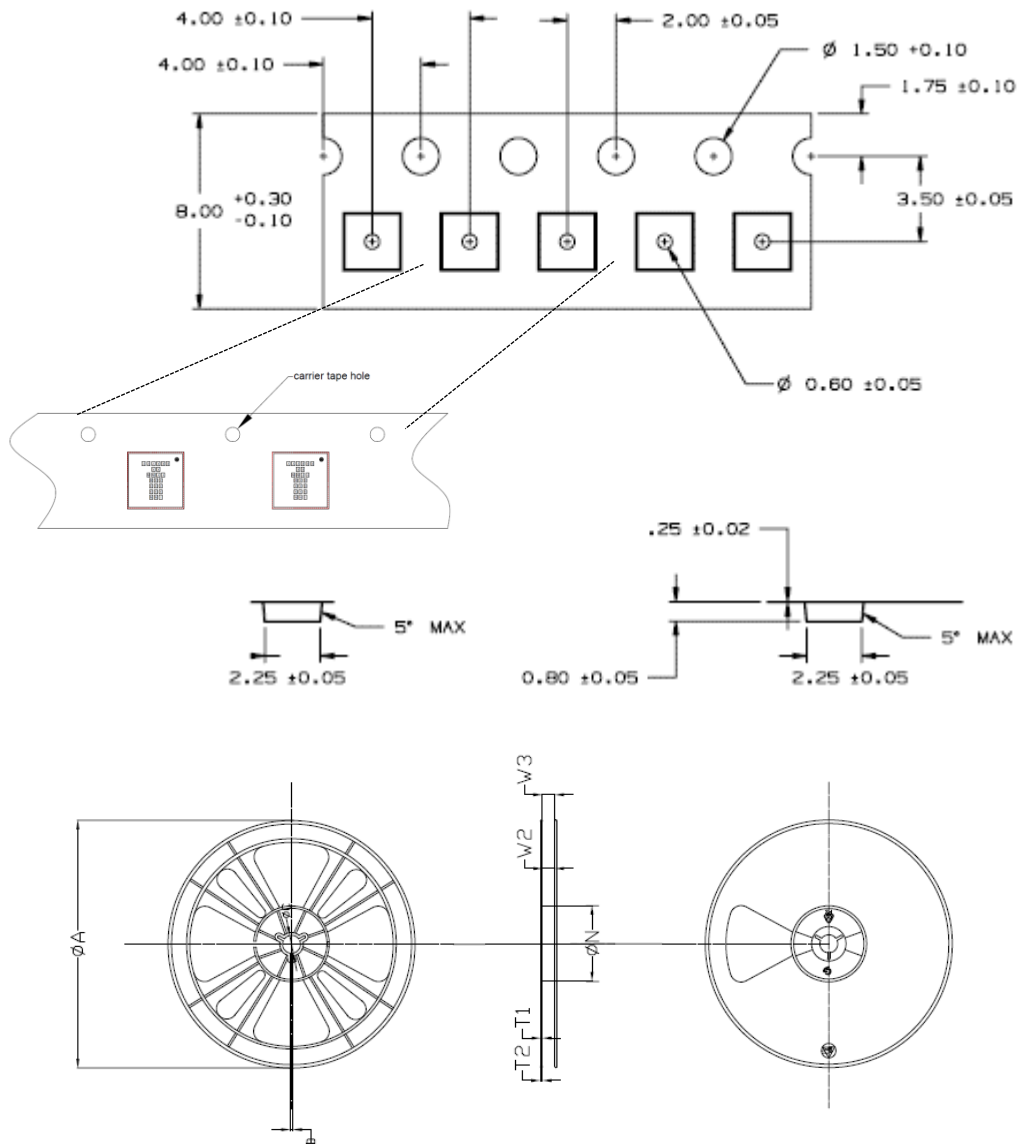


Row	Description	Example
Row 1	Company name	INN
Row 2	Product code	XXX
Row 3	Lot code	XXX
Row 4		XXX
Row 5	Date code	YYWW
Row 6	Wafer ID	XX
Row 7	Location ID	XXXYYY

INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

11. Reel Information

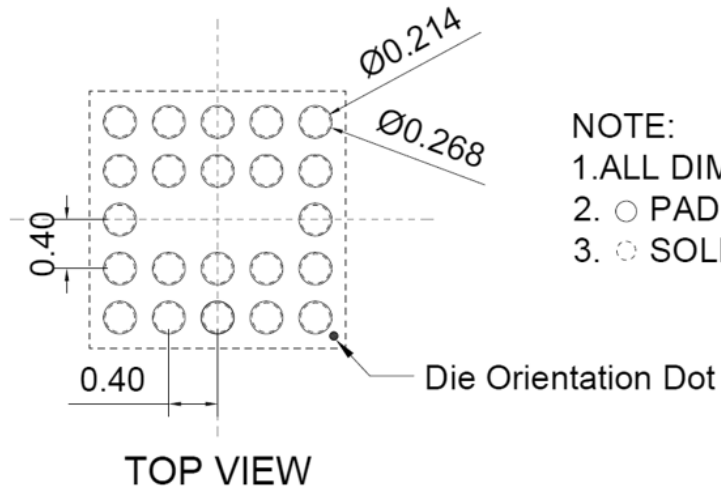


Item	Value&Tolerance
A	179 ± 1.0
B	2.0 ± 0.2
C	13.5 ± 0.2
N	54.8 ± 0.2
W2	9.0 ± 0.2
W3	9.2 ± 1.0
T1	1.2 ± 0.2
T2	1.5 ± 0.2

INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

12. Land Pattern



NOTE:

1. ALL DIMENSION ARE IN MILLIMETERS
2. ○ PAD DIMENSION
3. ○ SOLDER BALL DIMENSION

INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

13. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2022-04-28	1.0 version release
1.1	2022-06-30	Updated land pattern information
1.2	2023-08-14	<ol style="list-style-type: none">1. Updated format and corrected typos2. Added P_{tot} in Maximum Ratings3. Corrected description 'D' to 'D1', 'S' to 'D2' in Electric Characteristics Diagrams4. Updated Note in Electric Characteristics Diagrams

INN040W048A

40V Bi-directional GaN Enhancement-mode Power Transistor

