TPS7A16A-Q1
60-V, 5-µA I_Q, 100-mA, low-dropout voltage regulator with enable and power-good

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to 125°C ambient operating temperature range
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C3B
- Wide input voltage range: 3 V to 60 V
- Ultralow quiescent current: 5 µA
- Quiescent current at shutdown: 1 µA
- Output current: 100 mA
- Low dropout voltage: 60 mV at 20 mA
- Accuracy: 2%
- Available in:
  - Fixed output voltage: 3.3 V, 5 V
  - Adjustable version from approximately 1.2 to 18.5 V
- Power-good with programable delay
- Current-limit and thermal shutdown protections
- Stable with ceramic output capacitors: ≥ 2.2 µF
- Package: High-thermal-performance HVSSOP-8 PowerPAD™

2 Applications

- Emergency call (eCall)
- Battery management systems (BMS)
- On-board (OBC) and wireless chargers
- DC/DC converters

3 Description

The TPS7A16A-Q1 ultralow-power, low-dropout (LDO) voltage regulator offers the benefits of ultralow quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A16A-Q1 is designed for continuous or sporadic (power backup) battery-powered applications where ultralow quiescent current is critical to extending system battery life.

The TPS7A16A-Q1 offers an enable pin (EN) compatible with standard complementary metal oxide semiconductor (CMOS) logic and an integrated open-drain, active-high, power-good output (PG) with a user-programmable delay. These pins are intended for use in microcontroller-based, battery-powered applications where power-rail sequencing is required.

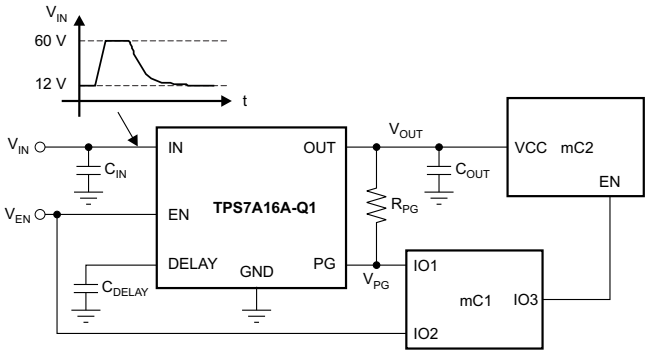
In addition, the TPS7A16A-Q1 is ideal for generating a low-voltage supply from multicell solutions ranging from high-cell-count power-tool packs to automotive applications; not only can this device supply a well-regulated voltage rail, but the TPS7A16A-Q1 can also withstand and maintain regulation during voltage transients. These features translate to simpler and more cost-effective, electrical surge-protection circuitry.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A16A-Q1	HVSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



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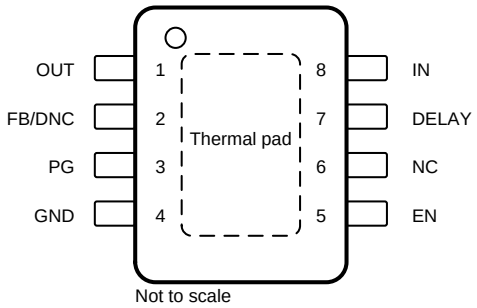
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2019) to Revision A	Page
• Changed status from Advance Information to Production Data	1

5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP With Exposed Thermal Pad
Top View



Not to scale

NC – No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DELAY	7	O	Delay pin. Connect a capacitor to GND to adjust the PG delay time; leave open if the reset function is not needed.
EN	5	I	Enable pin. This pin turns the regulator on or off. If $V_{EN} \geq V_{EN\_HI}$, the regulator is enabled. If $V_{EN} \leq V_{EN\_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
FB/DNC	2	I	For the adjustable version, the feedback pin is the input to the control-loop error amplifier. This pin is used to set the output voltage of the device when the regulator output voltage is set by external resistors. For the fixed-voltage versions, **do not connect** to this pin. Do not route this pin to any electrical net, not even to GND or IN.
GND	4	—	Ground pin
IN	8	I	Regulator input supply pin. A capacitor > 0.1 µF must be tied from this pin to ground to assure stability. TI recommends connecting a 10-µF ceramic capacitor from IN to GND (as close to the device as possible) to reduce circuit sensitivity to printed-circuit-board (PCB) layout, especially when long input tracer or high source impedances are encountered.
NC	6	---	This pin can be left open or tied to any voltage between GND and IN.
OUT	1	O	Regulator output pin. A capacitor > 2.2 µF must be tied from this pin to ground to assure stability. TI recommends connecting a 10-µF ceramic capacitor from OUT to GND (as close to the device as possible) to maximize ac performance.
PG	3	O	Power-good pin. Open-collector output; leave open or connect to GND if the power-good function is not needed.
Thermal pad	Pad	---	Solder to the printed circuit board (PCB) to enhance thermal performance. Although the thermal pad can be left floating, TI highly recommends connecting the thermal pad to the GND plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–0.3	62	V
	OUT pin to GND pin	–0.3	20	
	OUT pin to IN pin	–62	0.3	
	FB pin to GND pin	–0.3	3	
	FB pin to IN pin	–62	0.3	
	EN pin to IN pin	–62	0.3	
	EN pin to GND pin	–0.3	62	
	PG pin to GND pin	–0.3	5.5	
	DELAY pin to GND pin	–0.3	5.5	
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J, absolute maximum(2)	–40	150	°C
	Storage, T_{STG}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Permanent damage does not occur to the part operating within this range, though electrical performance is not guaranteed outside the operating ambient temperature range.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)		±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	Corner pins (OUT, GND, IN, and EN)	±750	
			Other pins	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	3		60	V
V_{OUT}	Output voltage	1.2		18.5	V
EN	EN pin voltage	0		V_{IN}	V
	EN pin slew-rate, voltage ramp-up			1.5	V/µs
DELAY	Delay pin voltage	0		5	V
PG	Power-good pin voltage	0		5	V

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A16A-Q1 DGN (HVSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	72.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	10.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

at T_A= –40°C to +125°C, V_{IN} = $V_{OUT(NOM)}$ + 500 mV or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 10 µA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and FB tied to OUT (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		3		60	V
V_{REF}	Internal reference	T_A = 25°C, V_{FB} = V_{REF}, V_{IN} = 3 V, I_{OUT} = 10 µA	1.169	1.193	1.217	V
V_{UVLO}	Undervoltage lockout threshold			2		V
V_{OUT}	Output voltage range	V_{IN} ≥ $V_{OUT(NOM)}$ + 0.5 V	V_{REF}		18.5	V
	Overall V_{OUT} accuracy	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 60 V(1), 10 µA ≤ I_{OUT} ≤ 100 mA	–2%		2%	
$\Delta V_{O(\Delta VI)}$	Line regulation	3 V ≤ V_{IN} ≤ 60 V		±1		$\%V_{OUT}$
$\Delta V_{O(\Delta IO)}$	Load regulation	10 µA ≤ I_{OUT} ≤ 100 mA		±1		$\%V_{OUT}$
V_{DO}	Dropout voltage	V_{IN} = 0.95x$V_{OUT(NOM)}$, I_{OUT} = 20 mA		60		mV
		V_{IN} = 0.95x$V_{OUT(NOM)}$, I_{OUT} = 100 mA		265	500	
I_{LIM}	Current limit	V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = $V_{OUT(NOM)}$ + 1 V(2)	101	225	400	mA
		V_{OUT} = 90% $V_{OUT(NOM)}$, V_{IN} = 3 V(3)	101	225	400	
I_{GND}	Ground current	3 V ≤ V_{IN} ≤ 60 V, I_{OUT} = 10 µA		5	15	µA
		I_{OUT} = 100 mA, V_{OUT} = 1.2 V		60		
I_{SHDN}	Shutdown supply current	V_{EN} = 0.4 V, V_{IN} = 12 V		0.59	5.0	µA
I_{FB}	Feedback current(4)		–1	0.0	1	µA
I_{EN}	Enable current	3 V ≤ V_{IN} ≤ 12 V, V_{IN} = V_{EN}	–1	0.01	1	µA
V_{EN_HI}	Enable high-level voltage		1.2			V
V_{EN_LO}	Enable low-level voltage				0.3	V
V_{IT}	PG trip threshold	OUT pin floating, V_{FB} increasing, V_{IN} ≥ V_{IN_MIN}	85		95	$\%V_{OUT}$
		OUT pin floating, V_{FB} decreasing, V_{IN} ≥ V_{IN_MIN}	83		93	
V_{HYS}	PG trip hysteresis			2.3		$\%V_{OUT}$
$V_{PG,\ LO}$	PG output low voltage	OUT pin floating, V_{FB} = 80% V_{REF}, I_{PG} = 100 µA			0.4	V
$I_{PG,\ LKG}$	PG leakage current	V_{PG} = $V_{OUT(NOM)}$	–1		1	µA
I_{DELAY}	DELAY pin current			1	2	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3 V, $V_{OUT(NOM)}$ = V_{REF}, C_{OUT} = 10 µF, f = 100 Hz		50		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		175		°C
		Reset, temperature decreasing		155		

(1) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load (P ≈ (V_{IN} – V_{OUT}) × I_{OUT} = (24 V – V_{REF}) × 50 mA ≈ 1.14 W). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.
(2) For fixed output voltages only.
(3) For adjustable output only, where V_{OUT} = 1.2 V
(4) I_{FB} > 0 µA flows out of the device.

6.6 Typical Characteristics

at T_A = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 10 µA, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, and FB tied to OUT (unless otherwise noted)

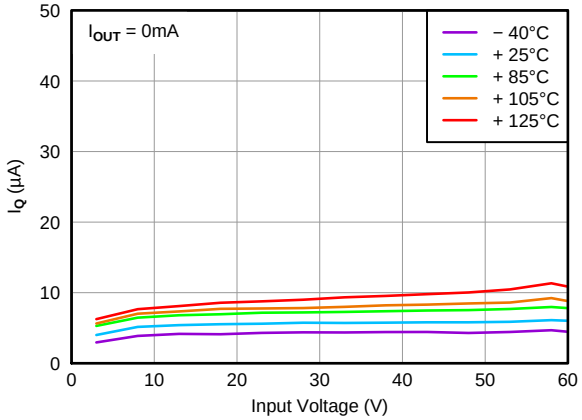


Figure 1. Quiescent Current vs Input Voltage

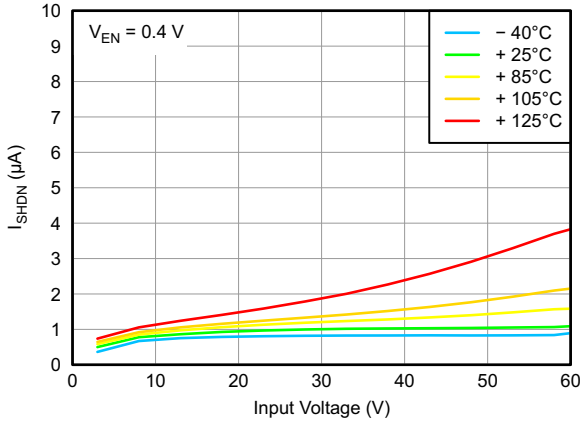


Figure 2. Shutdown Current vs Input Voltage

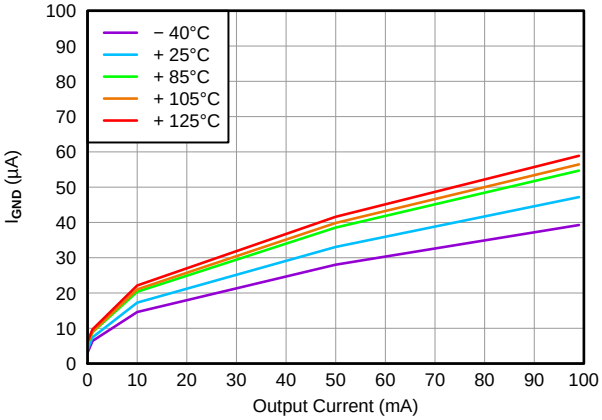


Figure 3. Quiescent Current vs Output Current

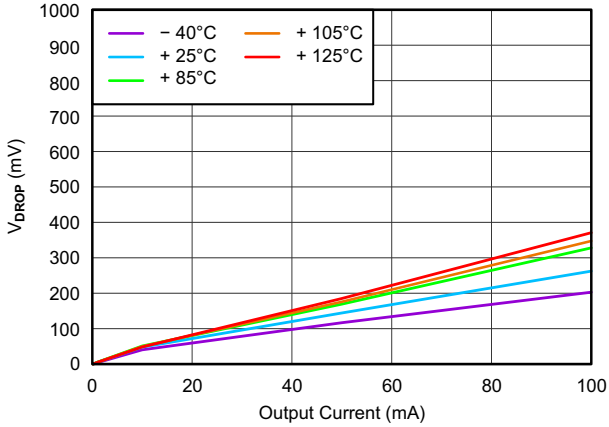


Figure 4. Dropout Voltage vs Output Current

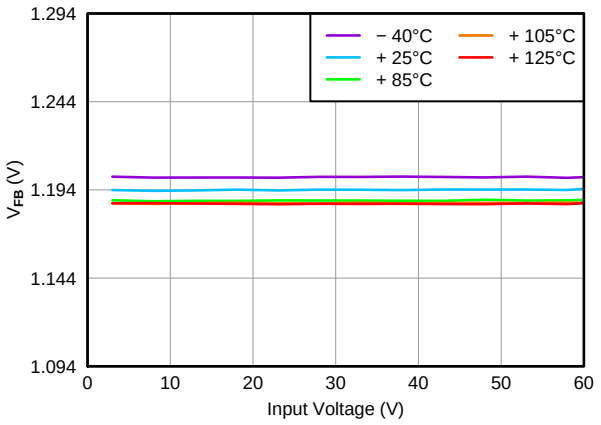


Figure 5. Feedback Voltage vs Input Voltage

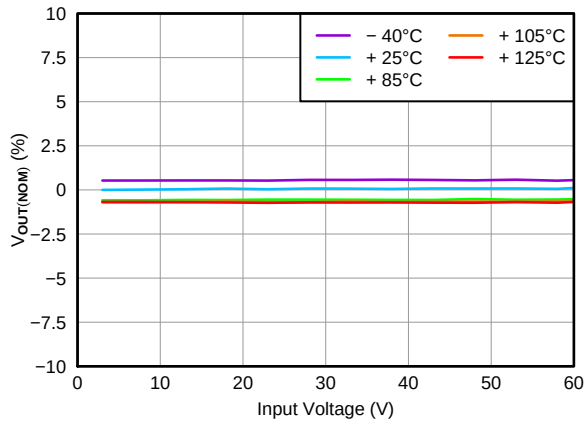


Figure 6. Line Regulation

Typical Characteristics (continued)

at T_A = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 10 µA, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, and FB tied to OUT (unless otherwise noted)

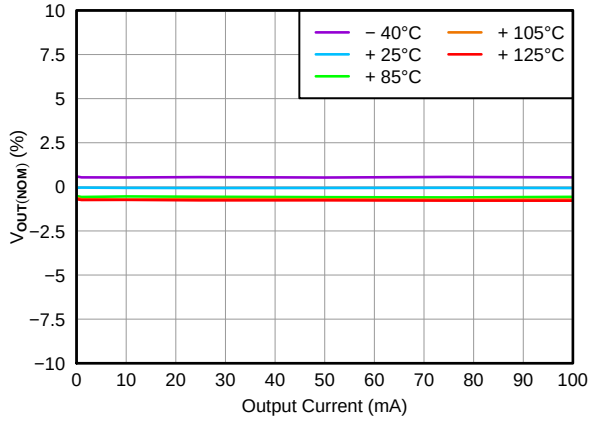


Figure 7. Load Regulation

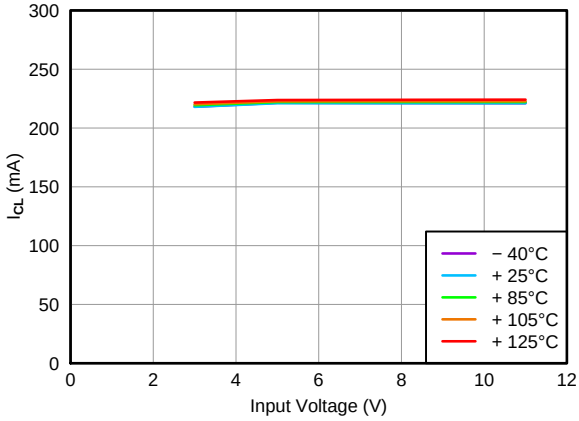


Figure 8. Current Limit vs Input Voltage

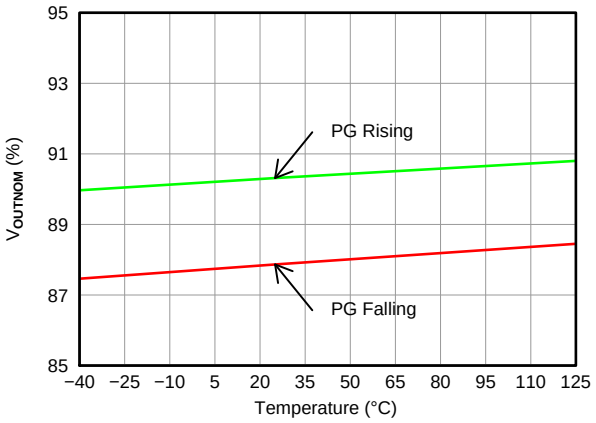


Figure 9. Power-Good Threshold Voltage vs Temperature

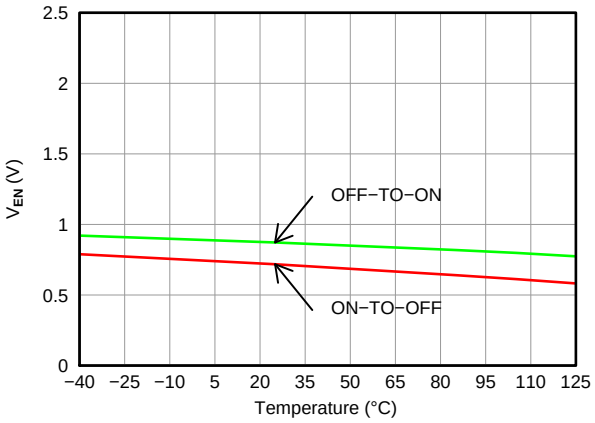


Figure 10. Enable Threshold Voltage vs Temperature

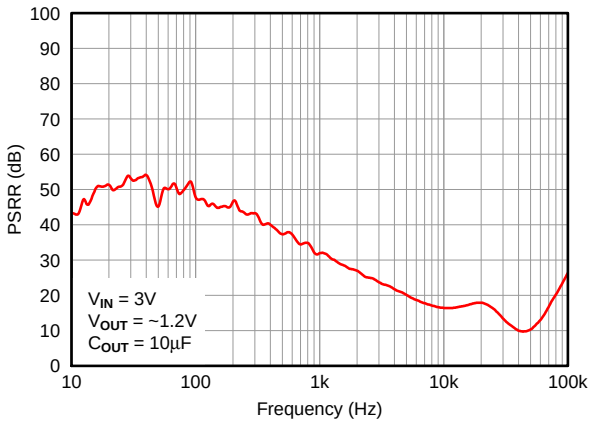


Figure 11. Power-Supply Rejection Ratio vs Frequency

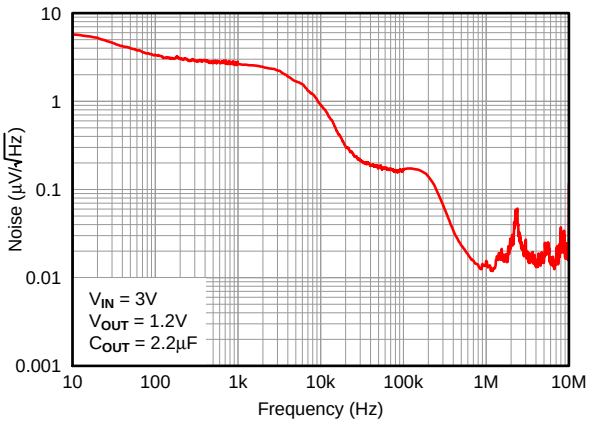


Figure 12. Output Spectral Noise Density

Typical Characteristics (continued)

at T_A = –40°C to 125°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or V_{IN} = 3 V (whichever is greater), V_{EN} = V_{IN}, I_{OUT} = 10 µA, C_{IN} = 1 µF, C_{OUT} = 2.2 µF, and FB tied to OUT (unless otherwise noted)

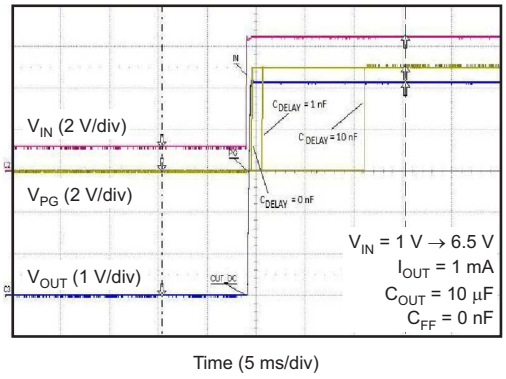


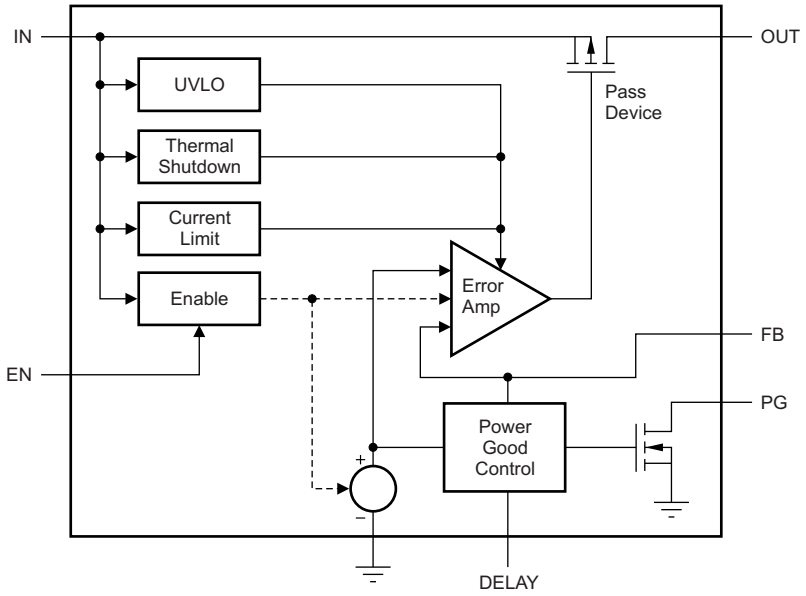
Figure 13. Power-Good Delay

7 Detailed Description

7.1 Overview

The TPS7A16A-Q1 is an ultra-low-power, low-dropout (LDO) voltage regulator that offers the benefits of ultra-low quiescent current, high input voltage, and miniaturized, high thermal-performance packaging. The TPS7A16A-Q1 also offers an enable pin (EN) and an integrated open-drain, active-high, power-good output (PG) with a user-programmable delay.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable (EN)

The enable pin is a high-voltage-tolerant pin. A high input on EN actives the device and turns on the regulator. For self-bias applications, connect this input to the IN pin. Ensure that $V_{EN} \leq V_{IN}$ at all times.

When the enable signal is comprised of pulse-width modulation (PWM) pulses, the slew rate of the rising and falling edges must be less than 1.5 V/µs. Adding a 0.1-µF capacitor from the EN pin to GND is recommended.

7.3.2 Regulated Output (V_{OUT})

The OUT pin is the regulated output based on the required voltage. The output has current limitation. During initial power up, the regulator has a soft-start incorporated to control the initial current through the pass element. In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the undervoltage lockout (UVLO) threshold, the regulator shuts down until the input voltage recovers above the minimum start-up level.

7.3.3 PG Delay Timer (DELAY)

The power-good delay time (t_{DELAY}) is defined as the time period from when V_{OUT} exceeds the PG trip threshold voltage (V_{IT}) to when the PG output is high. This power-good delay time is set by an external capacitor (C_{DELAY}) connected from the DELAY pin to GND; this capacitor is charged from 0 V to approximately 1.8 V by the DELAY pin current (I_{DELAY}) when V_{OUT} exceeds the PG trip threshold (V_{IT}).

7.4 Device Functional Modes

7.4.1 Power-Good

The power-good (PG) pin is an open-drain output and can be connected to any 5.5-V or lower rail through an external pullup resistor. When no C_{DELAY} is used, the PG output is high-impedance when V_{OUT} is greater than the PG trip threshold (V_{IT}). If V_{OUT} drops below V_{IT}, the open-drain output turns on and pulls the PG output low. If output voltage monitoring is not needed, the PG pin can be left floating or connected to GND.

To ensure proper operation of the power-good feature, maintain $V_{IN} \geq 3$ V (V_{IN_MIN}).

7.4.1.1 Power-Good Delay and Delay Capacitor

The power-good delay time (t_{DELAY}) is defined as the time period from when V_{OUT} exceeds the PG trip threshold voltage (V_{IT}) to when the PG output is high. This power-good delay time is set by an external capacitor (C_{DELAY}) connected from the DELAY pin to GND; this capacitor is charged from 0 V to ap 1.8 V by the DELAY pin current (I_{DELAY}) once V_{OUT} exceeds the PG trip threshold (V_{IT}).

When C_{DELAY} is used, the PG output is high-impedance when V_{OUT} exceeds V_{IT}, and V_{DELAY} exceeds V_{REF}.

The power-good delay time can be calculated using: $t_{DELAY} = (C_{DELAY} \times V_{REF})/I_{DELAY}$. For example, when C_{DELAY} = 10 nF, the PG delay time is approximately 12 ms; that is, (10 nF × 1.193 V) / 1 µA = 11.93 ms.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A16A-Q1 offers the benefit of ultra-low quiescent current, high input voltage, and miniaturized, high-thermal-performance packaging.

The TPS7A16A-Q1 is designed for continuous or sporadic (power backup) battery-operated applications where ultra-low quiescent current is critical to extending system battery life.

8.2 Typical Applications

8.2.1 TPS7A16A-Q1 Circuit as an Adjustable Regulator

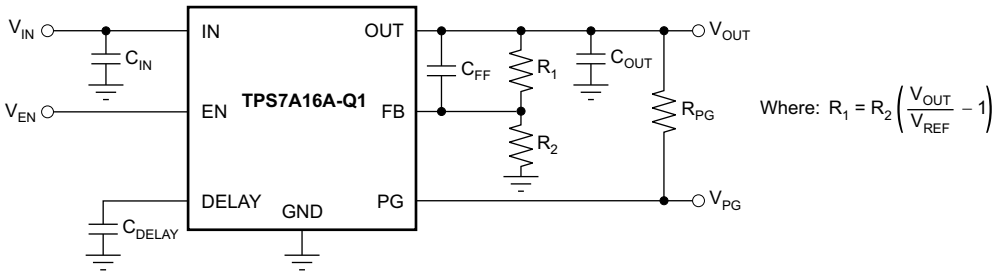


Figure 14. The TPS7A16A-Q1 Circuit as an Adjustable Regulator Schematic

8.2.1.1 Design Requirements

Table 1 lists the design parameters for this application.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 40 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 µF to 100 µF
Delay capacitor range	100 pF to 100 nF

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Adjustable Voltage Operation

The TPS7A16A-Q1 has an output voltage range from 1.194 V to 20 V. As shown in Figure 15, the nominal output of the device is set by two external resistors.

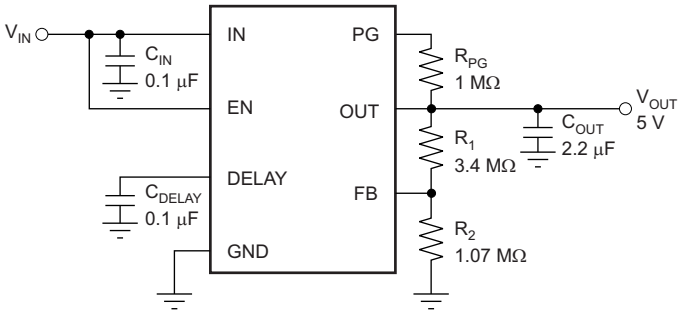


Figure 15. Adjustable Operation

Equation 1 can calculate R_1 and R_2 for any output voltage range:

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (1)$$

8.2.1.2.1.1 Resistor Selection

Use resistors in the order of MΩ to keep the overall quiescent current of the system as low as possible (by making the current used by the resistor divider negligible compared to the quiescent current of the device).

If greater voltage accuracy is required, take into account the voltage offset contributions as a result of feedback current and use 0.1% tolerance resistors.

Table 2 shows the resistor combination to achieve an output for a few of the most common rails using commercially available 0.1% tolerance resistors to maximize nominal voltage accuracy, while adhering to the formula shown in Equation 1.

Table 2. Selected Resistor Combinations

V_{OUT}	R_1	R_2	$V_{OUT}/(R_1 + R_2) \ll I_Q$	NOMINAL ACCURACY
1.194 V	0 Ω	∞	0 µA	±2%
1.8 V	1.18 MΩ	2.32 MΩ	514 nA	±(2% + 0.14%)
2..5 V	1.5 MΩ	1.37 MΩ	871 nA	±(2% + 0.16%)
3.3 V	2 MΩ	1.13 MΩ	1056 nA	±(2% + 0.35%)
5 V	3.4 MΩ	1.07 MΩ	1115 nA	±(2% + 0.39%)
10 V	7.87 MΩ	1.07 MΩ	1115 nA	±(2% + 0.42%)
12 V	14.3 MΩ	1.58 MΩ	755 nA	±(2% + 0.18%)
15 V	42.2 MΩ	3.65 MΩ	327 nA	±(2% + 0.19%)
18 V	16.2 MΩ	1.15 MΩ	1038 nA	±(2% + 0.26%)

Close attention must be paid to board contamination when using high-value resistors; board contaminants can significantly impact voltage accuracy. If board cleaning measures cannot be ensured, consider using a fixed-voltage version of the TPS7A16A-Q1 or using resistors in the order of hundreds or tens of kΩ.

8.2.1.2.2 Capacitor Recommendations

Use low equivalent-series-resistance (ESR) capacitors for the input, output, and feed-forward capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, but ceramic X5R capacitors are the most cost-effective and are available in higher values.

However, high-ESR capacitors can degrade PSRR.

8.2.1.2.3 Input and Output Capacitor Requirements

The TPS7A16A-Q1 ultra-low-power, high-voltage linear regulator achieves stability with a minimum input capacitance of 0.1 µF and output capacitance of 2.2 µF; however, TI recommends using a 10-µF ceramic capacitor to maximize ac performance.

8.2.1.2.4 Feed-Forward Capacitor (Only for Adjustable Version)

Although a feed-forward capacitor (C_{FF}) from OUT to FB is not needed to achieve stability, TI recommends using a 0.01-µF feed-forward capacitor to maximize ac performance.

8.2.1.2.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

8.2.1.3 Application Curves

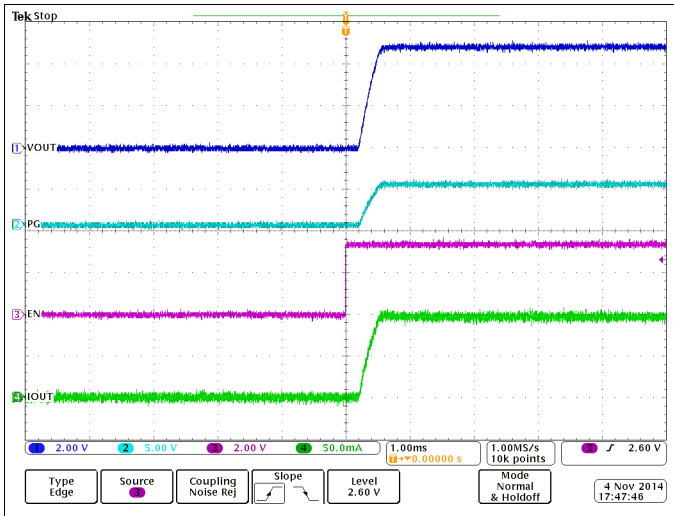


Figure 16. Channel 1 is V_{OUT}, Channel 2 is PG, Channel 4 is I_{OUT}, V_{IN} is 12 V and Ready Before EN

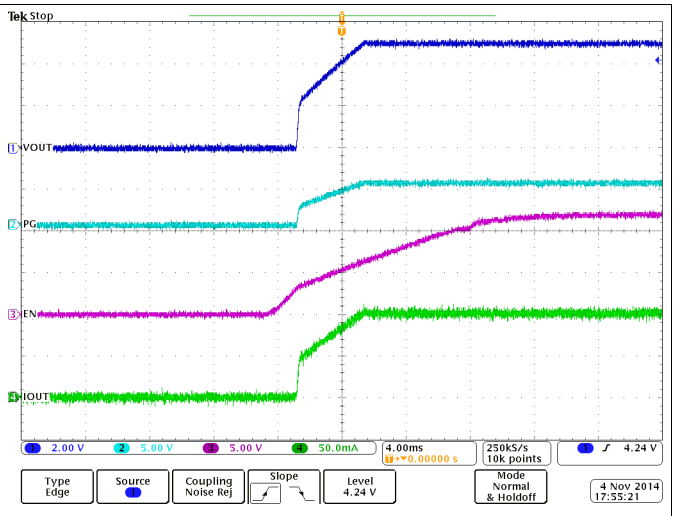


Figure 17. Channel1 is V_{OUT}, Channel 2 is PG, Channel 3 is EN, Channel4 is I_{OUT}, V_{IN} is 12 V Connected to EN

8.2.2 Automotive Applications

The TPS7A16A-Q1 maximum input voltage of 60 V makes the device ideal for use in automotive applications where high-voltage transients are present.

Events such as load-dump overvoltage (where the battery is disconnected while the alternator is providing current to a load) can cause voltage spikes from 25 V to 60 V. In order to prevent any damage to sensitive circuitry, local transient voltage suppressors can be used to cap voltage spikes to lower, more manageable voltages.

The TPS7A16A-Q1 can be used to simplify and lower costs in such cases. The very high voltage range allows this regulator not only to withstand the voltages coming out of these local transient voltage suppressors, but even replace them, thus lowering system cost and complexity. Figure 18 shows a circuit diagram of an example automotive application.

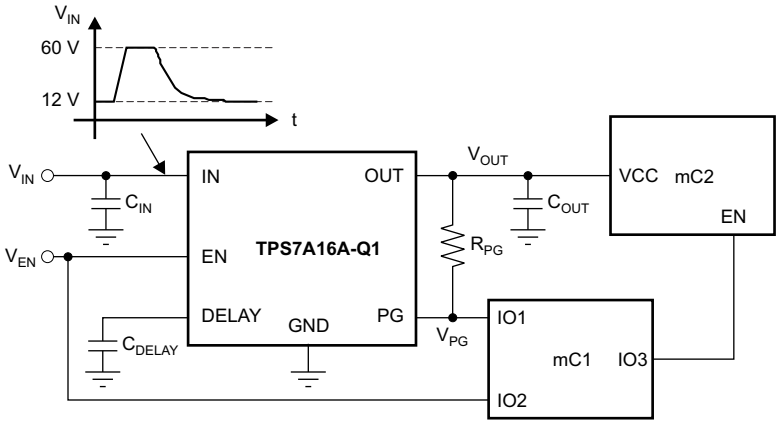


Figure 18. Low-Power Microcontroller Rail Sequencing in Automotive Applications Subjected to Load-Dump Transients

8.2.2.1 Design Requirements

Table 3 lists the design parameters for this application.

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	5.5 V to 60 V
Output voltage	5 V
Output current rating	100 mA
Output capacitor range	2.2 µF to 100 µF
Delay capacitor range	100 pF to 100 nF

8.2.2.2 Detailed Design Procedure

See the *Capacitor Recommendations* and *Input and Output Capacitor Requirements* sections.

8.2.2.2.1 Device Recommendations

The output is fixed, so choose the TPS7A16A-Q1.

8.2.2.3 Application Curves

See Figure 16 and Figure 17.

9 Power Supply Recommendations

Design of the device is for operation from an input voltage supply with a range between 3 V and 60 V. This input supply must be well regulated. The TPS7A16A-Q1 ultra-low-power, high-voltage linear regulator achieves stability with a minimum input capacitance of 0.1 µF and output capacitance of 2.2 µF; however, TI recommends using a 10-µF ceramic capacitor to maximize AC performance.

10 Layout

10.1 Layout Guidelines

To improve ac performance such as PSRR, output noise, and transient response, the board is recommended to be designed with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. This grounding scheme is commonly referred to as *star grounding*. In addition, directly connect the ground connection for the output capacitor to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized in order to maximize performance and ensure stability. Every capacitor must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they can impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this document, use the same layout pattern used for the TPS7A16A-Q1 evaluation board, available at www.ti.com.

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, bypass the IN pin to ground with a low-ESR ceramic bypass capacitor with X5R or X7R dielectric.

Acceptable performance can be obtained with alternative PCB layouts; however, the layout and the schematic have been shown to produce good results and are meant as a guideline.

Figure 19 illustrates the schematic for the suggested layout. Figure 20 and Figure 21 depict the top and bottom printed circuit board (PCB) layers for the suggested layout, respectively.

10.1.1 Additional Layout Considerations

The high impedance of the FB pin makes the regulator sensitive to parasitic capacitances that can couple undesirable signals from nearby components (especially from logic and digital devices, such as microcontrollers and microprocessors); these capacitively-coupled signals can produce undesirable output voltage transients. In these cases, use a fixed-voltage version of the TPS7A16A-Q1, or isolate the FB node by flooding the local PCB area with ground-plane copper to minimize any undesirable signal coupling.

10.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper increases the effectiveness of removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. As Equation 2 shows, power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element:

$$P_D = (V_{IN} - V_{OUT})\, I_{OUT} \quad (2)$$

Layout Guidelines (continued)

10.1.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting the regulator from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat-spreading area. For reliable operation, limit junction temperature to a maximum of 125°C at the worst-case ambient temperature for a given application. To estimate the margin of safety in a complete design (including the copper heat-spreading area), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 45°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A16A-Q1 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS7A16A-Q1 into thermal shutdown degrades device reliability.

10.2 Layout Examples

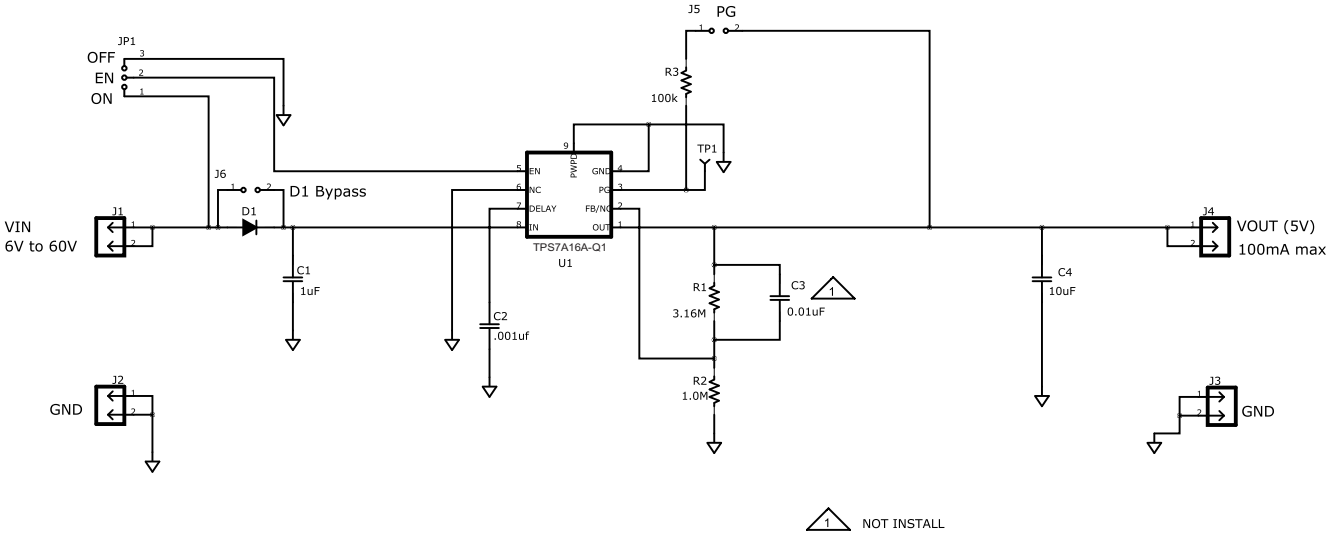


Figure 19. Schematic for Suggested Layout

Layout Examples (continued)

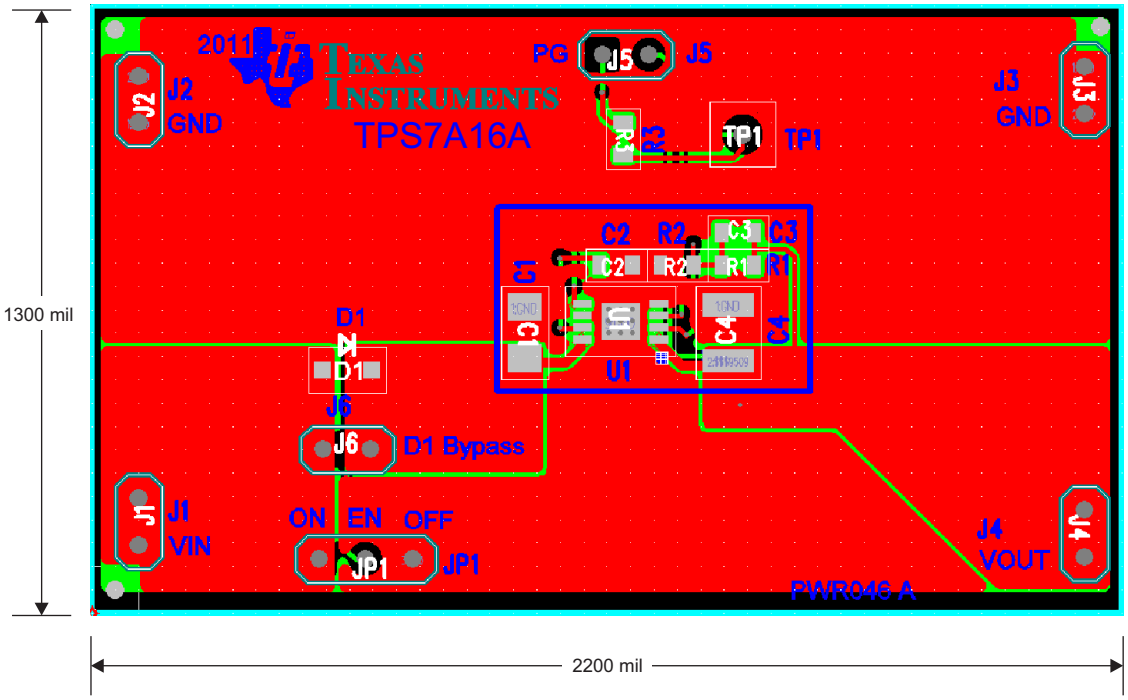


Figure 20. Suggested Layout: Top Layer

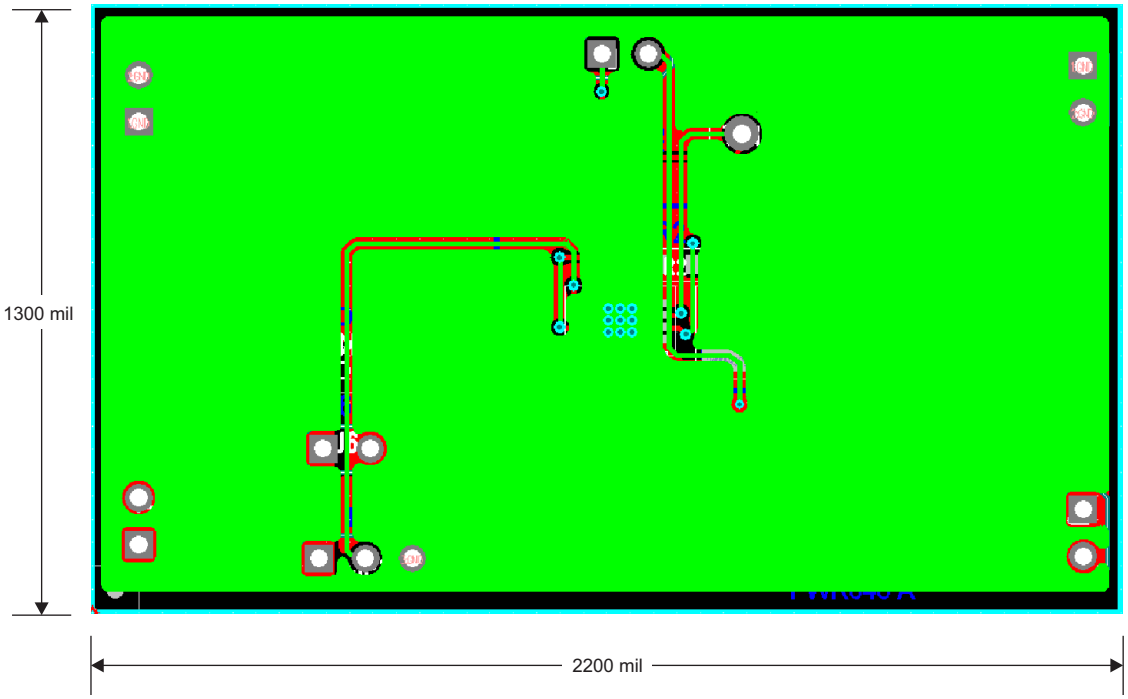


Figure 21. Suggested Layout: Bottom Layer

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7A1601AQDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1NT1
TPS7A1601AQDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1NT1
TPS7A1633AQDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1NU1
TPS7A1633AQDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1NU1
TPS7A1650AQDGNRQ1	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1NV1
TPS7A1650AQDGNRQ1.A	Active	Production	HVSSOP (DGN) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1NV1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF TPS7A16A-Q1 :

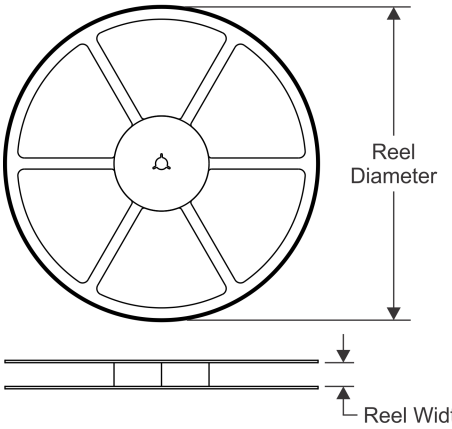
- Catalog : TPS7A16A

NOTE: Qualified Version Definitions:

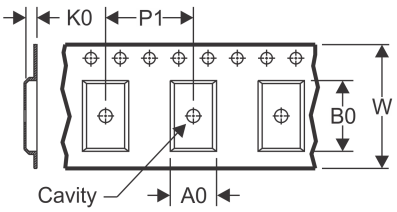
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

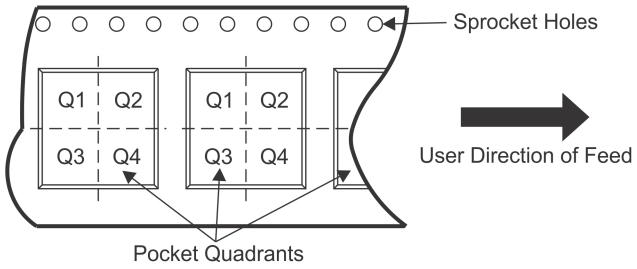


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

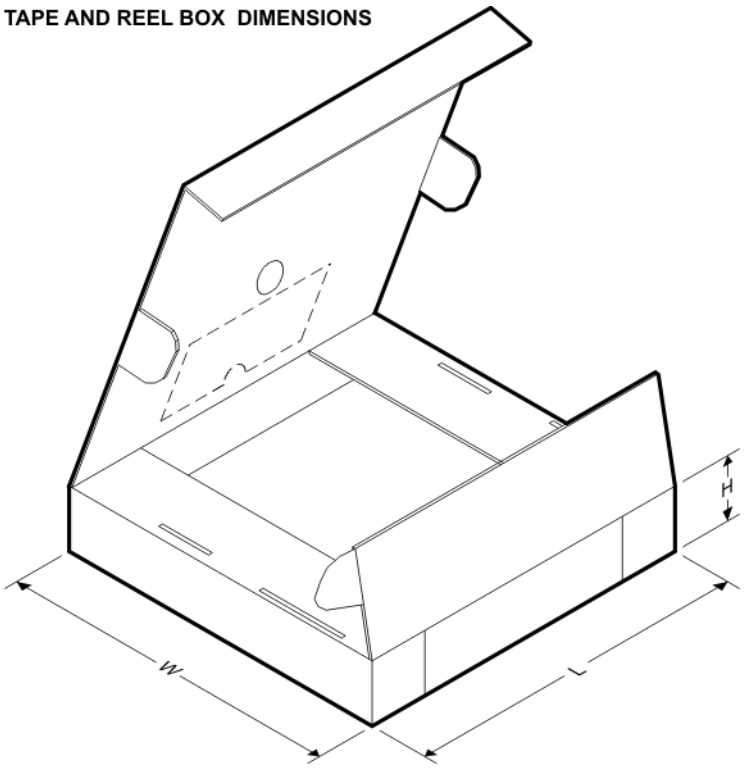
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A1601AQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1633AQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A1650AQDGNRQ1	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A1601AQDGNRQ1	HVSSOP	DGN	8	2500	367.0	367.0	38.0
TPS7A1633AQDGNRQ1	HVSSOP	DGN	8	2500	367.0	367.0	38.0
TPS7A1650AQDGNRQ1	HVSSOP	DGN	8	2500	367.0	367.0	38.0

GENERIC PACKAGE VIEW

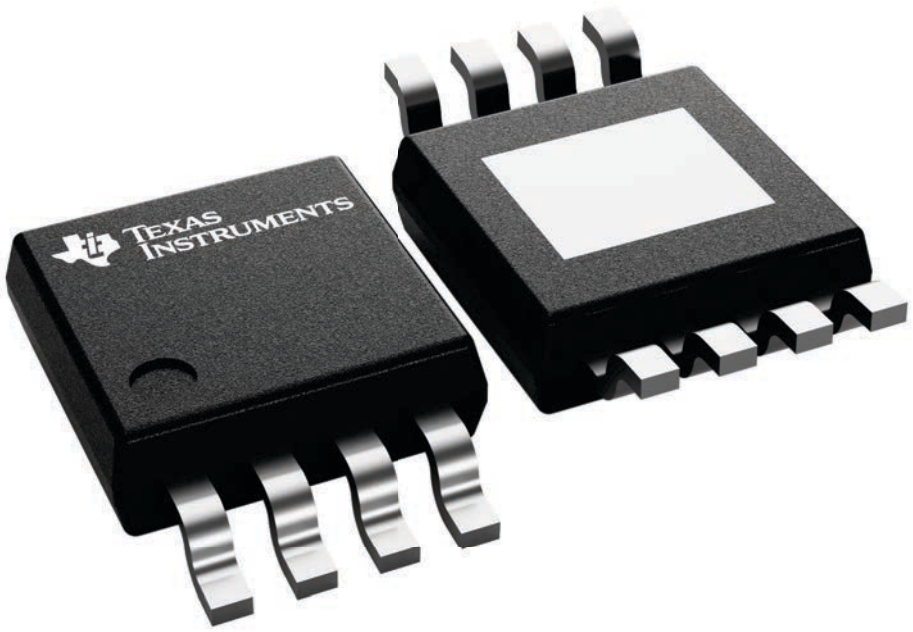
DGN 8

PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

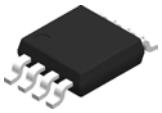
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



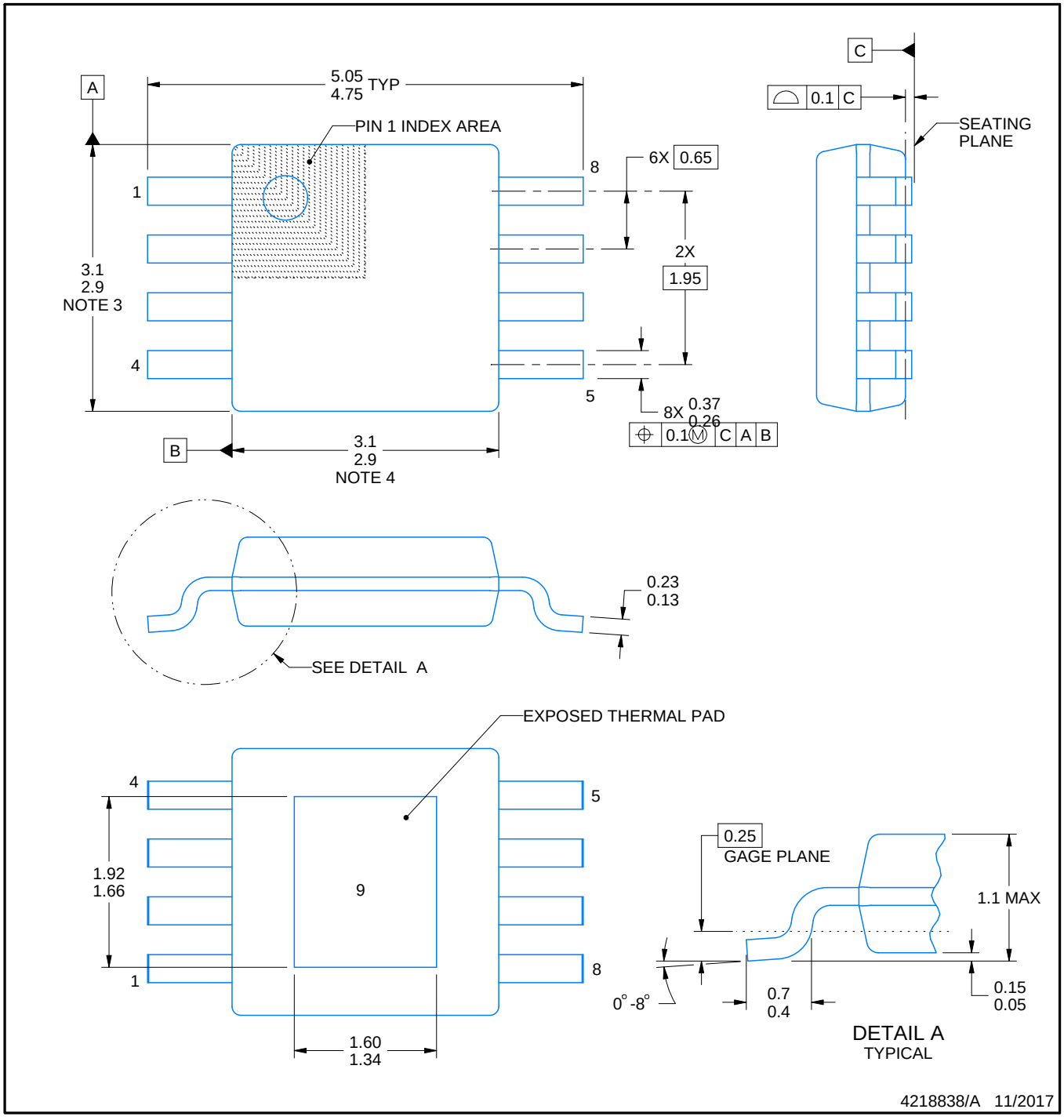
PACKAGE OUTLINE

DGN0008C



HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

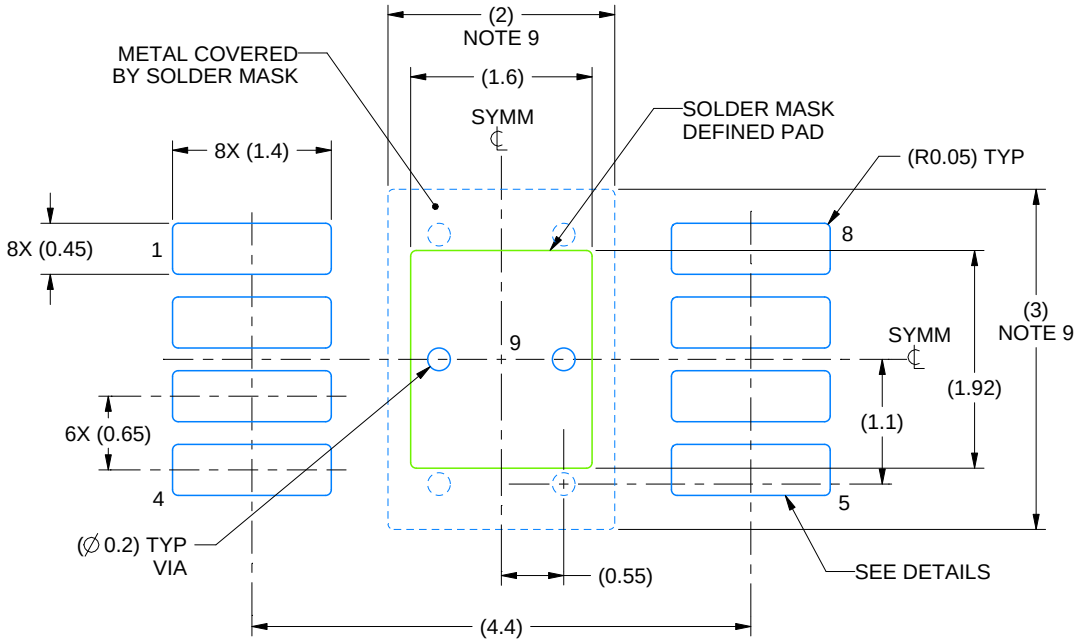
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

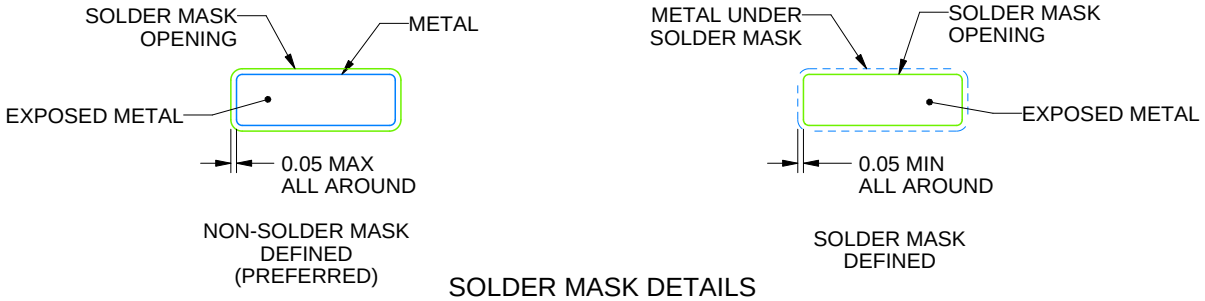
DGN0008C

HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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NOTES: (continued)

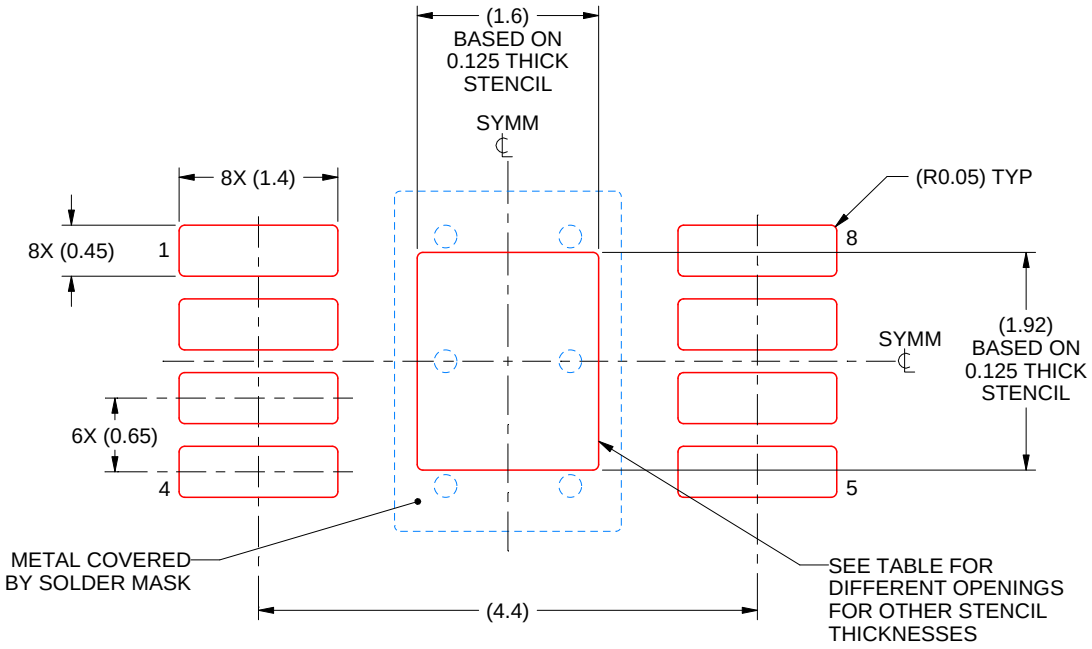
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008C

HVSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.79 X 2.15
0.125	1.60 X 1.92 (SHOWN)
0.15	1.46 X 1.75
0.175	1.35 X 1.62

4218838/A 11/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.