

# PUMD9

# 50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 k $\Omega$ , R2 = 47 k $\Omega$

1 July 2022

Product data sheet

### 1. General description

NPN/PNP Resistor-Equipped double Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PUMH9 PNP/PNP complement: PUMB9

#### 2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- · Reduces component count
- · Reduces pick and place costs

# 3. Applications

- Digital application in automotive and industrial segments
- · Cost-saving alternative for BC847/BC857 series in digital applications
- Controlling IC inputs
- Switching loads

#### 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
Per transistor,	Per transistor, for the PNP transistor with negative polarity							
V <sub>CEO</sub>	collector-emitter voltage	open base		-	-	50	V	
Io	output current			-	-	100	mA	
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ	
R2/R1	bias resistor ratio		[1]	3.7	4.7	5.7		

<sup>[1]</sup> See "Section 11: Test information" for resistor calculation and test conditions.

# 5. Pinning information

#### **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1		O1 I2 GND2
2	I1	input (base) TR1		
3	O2	output (collector) TR2	6 5 4	R1 R2
4	GND2	GND (emitter) TR2		TR2
5	12	input (base) TR2	0	TR1 R2 R1
6	01	output (collector) TR1	□1 □2 □3	
			TSSOP6 (SOT363)	
				GND1 I1 O2 006aaa143

# 6. Ordering information

**Table 3. Ordering information** 

Type number	Package				
	Name	Description	Version		
PUMD9		plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363		

### 7. Marking

#### Table 4. Marking codes

Type number	Marking code[1]
PUMD9	D%9

[1] % = placeholder for manufacturing site code

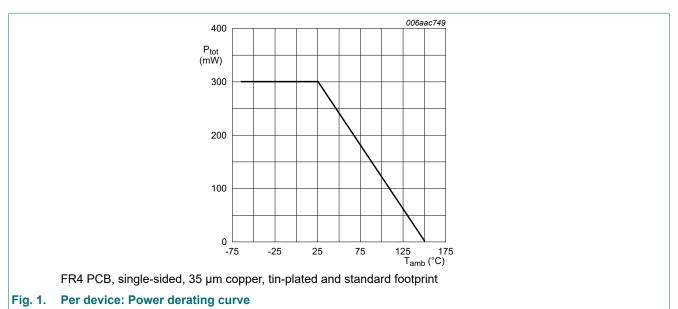
# 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transiste	or, for the PNP transistor wit	n negative polarity	,	<u> </u>		
V <sub>CBO</sub>	collector-base voltage	open emitter		-	50	V
V <sub>CEO</sub>	collector-emitter voltage	open base		-	50	V
V <sub>EBO</sub>	emitter-base voltage	open collector		-	6	V
V <sub>I</sub>	input voltage	input voltage TR1		-	40	V
				-	-6	V
		input voltage TR2		-	6	V
				-	-40	V
lo	output current			-	100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	200	mW
Per device	<u> </u>		,	'		
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C	[1]	-	300	mW
Tj	junction temperature			-	150	°C
T <sub>amb</sub>	ambient temperature			-65	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 µm copper, tin-plated and standard footprint.



#### 9. Thermal characteristics

**Table 6. Thermal characteristics** 

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transistor	1						
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint.

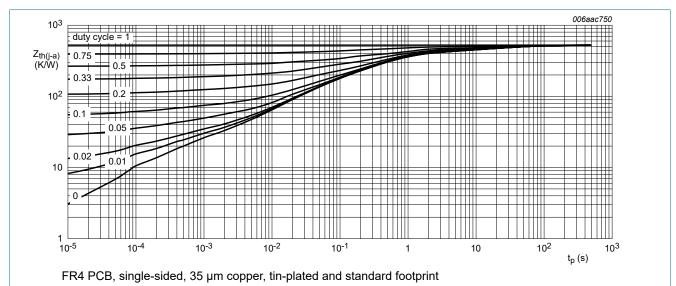


Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

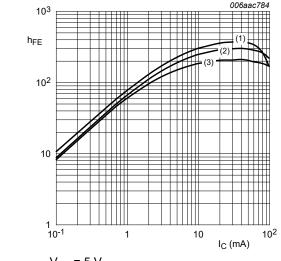
# 10. Characteristics

#### **Table 7. Characteristics**

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transist	tor, for the PNP transistor v	vith negative polarity					
V <sub>(BR)CBO</sub>	collector-base breakdown voltage	$I_C = 100 \ \mu A; I_E = 0 \ A; T_{amb} = 25 \ ^{\circ}C$		50	-	-	V
V <sub>(BR)CEO</sub>	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}; I_B = 0 \text{ A}; T_{amb} = 25 \text{ °C}$		50	-	-	V
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = 50 V; I <sub>E</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	100	nA
		V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A; T <sub>amb</sub> = 25 °C		-	-	100	nA
	current	V <sub>CE</sub> = 30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C		-	-	5	μA
I <sub>EBO</sub>	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_{C} = 0 \text{ mA}; T_{amb} = 25 \text{ °C}$		-	-	150	μA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 5 mA; T <sub>amb</sub> = 25 °C		100	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	$I_C = 5 \text{ mA}; I_B = 0.25 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$		-	-	100	mV
$V_{I(off)}$	off-state input voltage	V <sub>CE</sub> = 5 V; I <sub>C</sub> = 100 μA; T <sub>amb</sub> = 25 °C		-	0.7	0.5	V
V <sub>I(on)</sub>	on-state input voltage	V <sub>CE</sub> = 0.3 V; I <sub>C</sub> = 1 mA; T <sub>amb</sub> = 25 °C		1.4	0.8	-	V
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	3.7	4.7	5.7	
TR1 (NPN)					'		
C <sub>c</sub>	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A}; f = 1 \text{ MHz}; $ $T_{amb} = 25 \text{ °C}$		-	-	2.5	pF
f <sub>T</sub>	transition frequency	$V_{CE}$ = 5 V; $I_{C}$ = 10 mA; f = 100 MHz; $T_{amb}$ = 25 °C	[2]	-	230	-	MHz
TR2 (PNP)					,		
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = -10 V; I <sub>E</sub> = 0 A; i <sub>e</sub> = 0 A; f = 1 MHz; T <sub>amb</sub> = 25 °C		-	-	3	pF
f <sub>T</sub>	transition frequency	$V_{CE}$ = -5 V; $I_{C}$ = -10 mA; f = 100 MHz; $T_{amb}$ = 25 °C	[2]	-	180	-	MHz

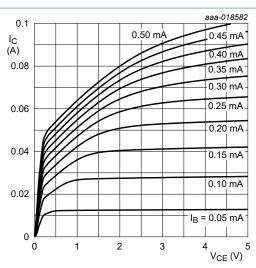
<sup>[1]</sup> See "Section 11: Test information" for resistor calculation and test conditions.

<sup>[2]</sup> Characteristics of built-in transistor



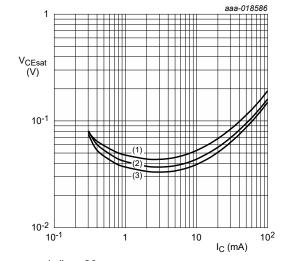
V<sub>CE</sub> = 5 V (1) T<sub>amb</sub> = 100 °C (2) T<sub>amb</sub> = 25 °C (3) T<sub>amb</sub> = -40 °C

TR1 (NPN): DC current gain as a function of Fig. 3. collector current; typical values



T<sub>amb</sub> = 25 °C

TR1 (NPN): Collector current as a function of Fig. 4. collector-emitter voltage; typical values



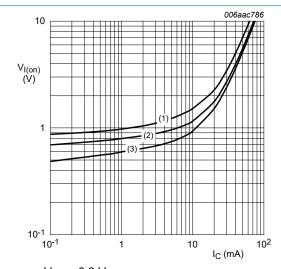
 $I_{\rm C}/I_{\rm B} = 20$ 

(1) T<sub>amb</sub> = 100 °C

(2) T<sub>amb</sub> = 25 °C

(3)  $T_{amb} = -40 \, ^{\circ}C$ 

Fig. 5. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values



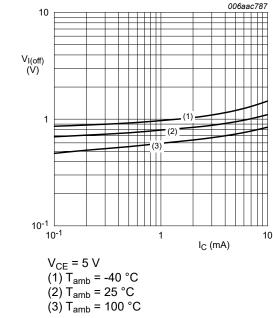
 $V_{CE} = 0.3 V$ 

 $(1) T_{amb} = -40 °C$ 

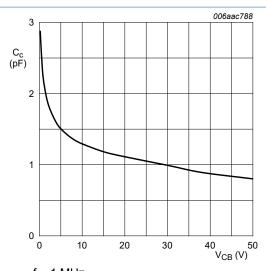
 $(2) T_{amb} = 25 °C$ 

(3)  $T_{amb} = 100 \, ^{\circ}C$ 

Fig. 6. TR1 (NPN): On-state input voltage as a function of collector current; typical values

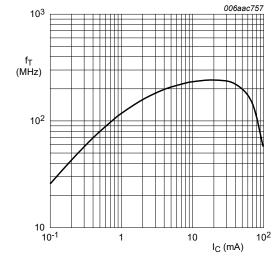


TR1 (NPN): Off-state input voltage as a function Fig. 7. of collector current; typical values



f = 1 MHz $T_{amb} = 25 \, ^{\circ}C$ 

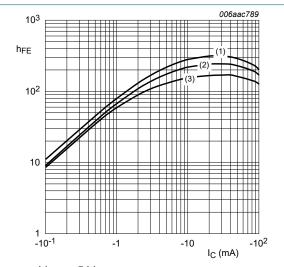
TR1 (NPN): Collector capacitance as a function Fig. 8. of collector-base voltage; typical values



f = 100 MHz

 $T_{amb}$  = 25 °C  $V_{CE} = 5 V$ 

Fig. 9. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor



 $V_{CE} = -5 V$ 

 $(1) T_{amb} = 100 °C$ 

 $(2) T_{amb} = 25 °C$ 

(3)  $T_{amb} = -40 \, ^{\circ}C$ 

Fig. 10. TR2 (PNP): DC current gain as a function of collector current; typical values

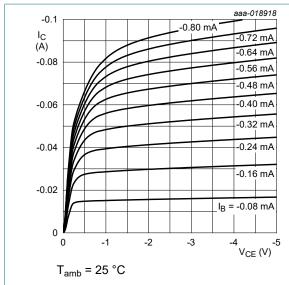
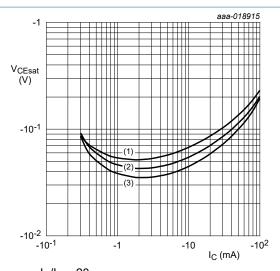
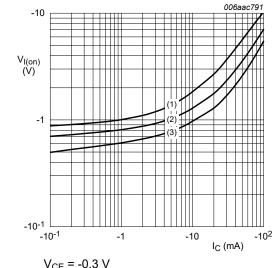


Fig. 11. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values



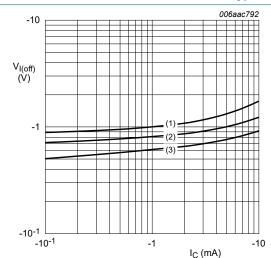
 $I_{C}/I_{B} = 20$ (1)  $T_{amb} = 100 \, ^{\circ}C$ (2)  $T_{amb} = 25 \, ^{\circ}C$ (3)  $T_{amb} = -40 \, ^{\circ}C$ 

Fig. 12. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values



 $V_{CE} = -0.3 \text{ V}$ (1)  $T_{amb}$  = -40 °C (2) T<sub>amb</sub> = 25 °C (3)  $T_{amb} = 100 \, ^{\circ}C$ 

of collector current; typical values



 $V_{CE} = -5 V$  $(1) T_{amb} = -40 °C$  $(2) T_{amb} = 25 °C$ (3)  $T_{amb} = 100 \, ^{\circ}C$ 

Fig. 13. TR2 (PNP): On-state input voltage as a function | Fig. 14. TR2 (PNP): Off-state input voltage as a function of collector current; typical values

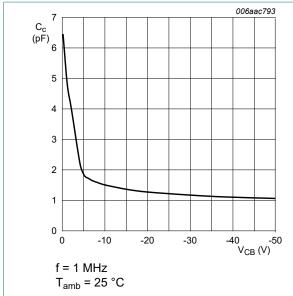


Fig. 15. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values

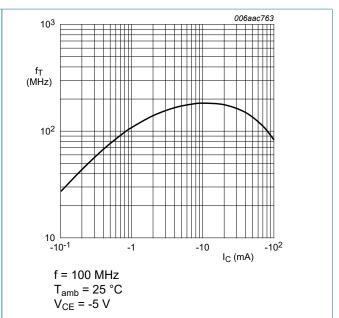


Fig. 16. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

### 11. Test information

#### **Resistor calculation**

· Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I12) - V(I11)}{I12 - I11}$$

· Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I14) - V(I13)}{R1 \cdot (I14 - I13)} - 1$$

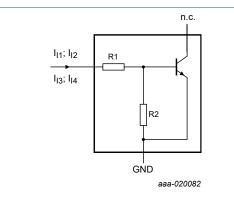


Fig. 17. TR1 (NPN): Resistor test circuit

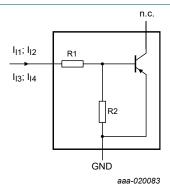


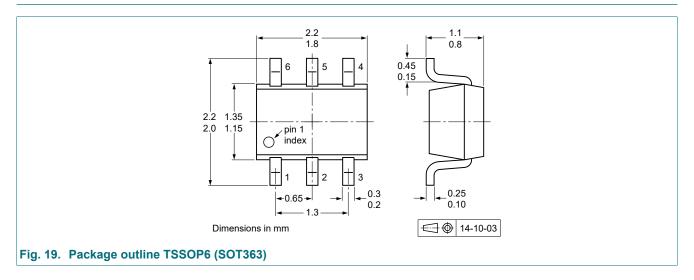
Fig. 18. TR2 (PNP): Resistor test circuit

#### **Resistor test conditions**

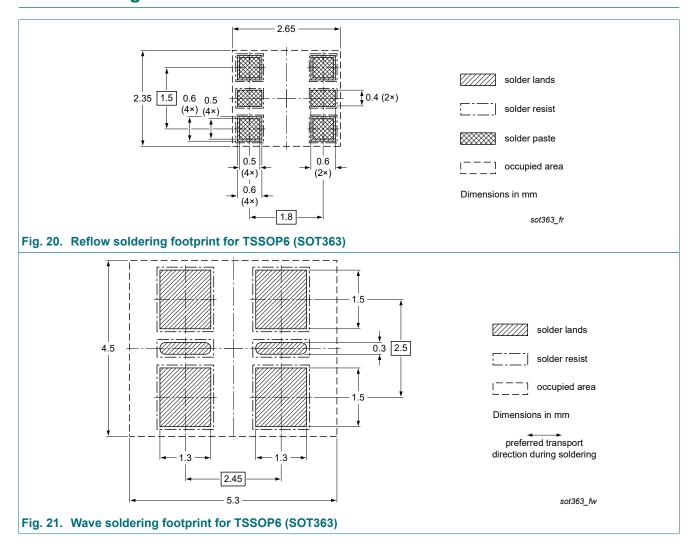
**Table 8. Resistor test conditions** 

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I <sub>I1</sub>	I <sub>12</sub>	I <sub>13</sub>	I <sub>14</sub>
Per transistor, for the PNP with negative polarity						
PUMD9	10	47	90 μΑ	140 μΑ	-55 μΑ	-105 μA

# 12. Package outline



# 13. Soldering



# 14. Revision history

#### Table 9. Revision history

			1	
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMD9 v.7	20220701	Product data sheet	-	PEMD9_PUMD9 v.6
Modification:	of Nexperia. Legal texts h Family data Product char automotive (	of this data sheet has been red have been adapted to the new sheet reduced to single type d nged to non-automotive qualifity-Q) product alternative(s). rmation removed.	company name ata sheet.	where appropriate.
PEMD9_PUMD9 v.6	20111122	Product data sheet	-	PEMD9_PUMD9 v.5
PEMD9_PUMD9 v.5	20040415	Product data sheet	-	PEMD9_PUMD9 v.4
PEMD9_PUMD9 v.4	20031104	Product specification	-	PEMD9 v.2 PUMD9 v.3
PEMD9 v.2	20020905	Product specification	-	PEMD9 v.1
PEMD9 v.1	20011022	Preliminary specification	-	-
PUMD9 v.3	20010216	Product specification	-	PUMD9 v.2
PUMD9 v.2	19990520	Product specification	-	PUMD9 v.1
PUMD9 v.1	19990107	Product specification	-	-

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#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <a href="https://www.nexperia.com">https://www.nexperia.com</a>.

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