REF4132-Q1 Low-Drift, Low-Power, Small-Footprint Series Voltage Reference

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40ºC to +125ºC ambient operating temperature range
  - Device HBM ESD classification level 2
- Voltage options: 2.5V, 3V, 3.3V, 4.096V, 5V
- Initial accuracy: ±0.05% (maximum)
- Temperature coefficient : A grade: 12 ppm/°C (maximum) B grade: 30 ppm/°C (maximum)
- Operating temperature range: −40°C to +125°C
- Output current: ±10 mA
- Low quiescent current: 100 μA (maximum)
- Output 1/f noise (0.1 Hz to 10 Hz): 15 μV_{PP}/V
- Excellent long-term stability 30 ppm/1000 hrs
- Small footprint 5-pin SOT-23 package

2 Applications

- ADAS front camera
- ADAS surround view system ECU
- Traction inverter
- Automotive DC/DC converter
- HEV/EV On-board (OBC) & wireless charger

3 Description

The REF4132-Q1 device is a low temperature drift (12 ppm/°C), low-power, high-precision CMOS voltage reference, featuring ±0.05% initial accuracy, low operating current with power consumption less than 100μA. This device also offers very low output noise of 15 μV_{p-p} /V, which enables its ability to maintain high signal integrity with high-resolution data converters in noise critical systems. Packaged in the same SOT-23-5 package, REF4132-Q1 offers enhanced specifications and pin-to-pin replacement for LM4128-Q1 and LM4132-Q1.

Stability and system reliability are further improved by the low output-voltage hysteresis of the device and low long-term output voltage drift. Furthermore, the small size and low operating current of the devices (100 μA) can benefit portable and battery-powered applications.

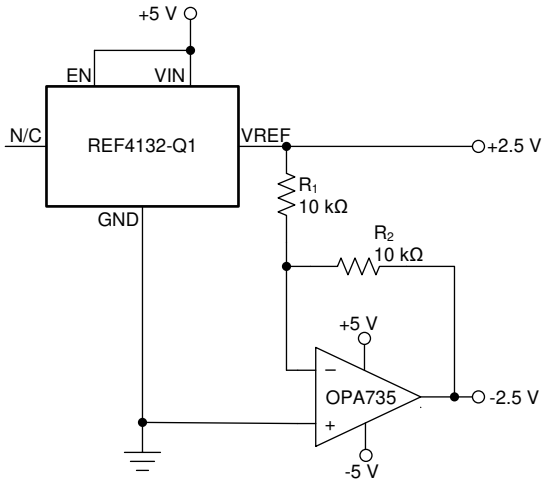
REF4132-Q1 is specified for the wide temperature range of −40°C to +125°C.

Device Information(1)

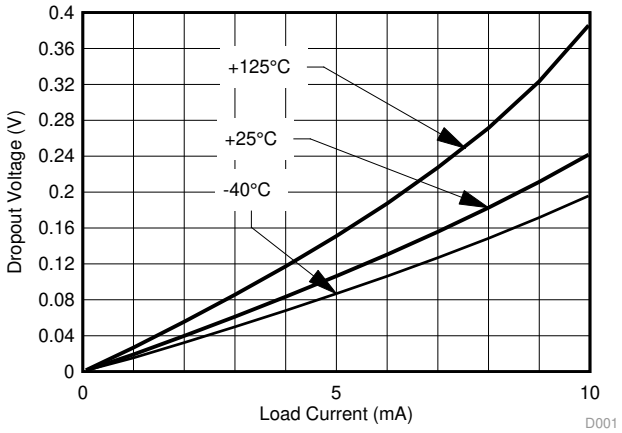
PART NAME	PACKAGE	BODY SIZE (NOM)
REF4132-Q1	SOT-23 (5)	2.90 mm × 1.60 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Dropout vs. Current Load Over Temperature



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

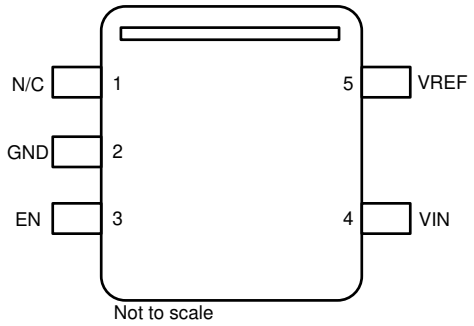
Changes from Original (February 2020) to Revision A	Page
• APL to RTM release.	1

5 Device Comparison Table

PRODUCT	V_{OUT}
REF4132 - 2.5	2.5 V
REF4132 - 3.0	3 V
REF4132 - 3.3	3.3 V
REF4132 - 4.0	4.096 V
REF4132 - 5.0	5 V

6 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	N/C	–	No connect pin, leave floating
2	GND	Ground	Ground
3	EN	I/O	Enable pin. Enables or disables the device.
4	VIN	Power	Input supply
5	VREF	Output	Reference output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	6	V
Enable voltage	V_{EN}	–0.3	V_{IN} + 0.3	V
Output voltage	V_{REF}	–0.3	5.5	V
Output short circuit current	I_{SC}		20	mA
Operating temperature range	T_A	–55	150	°C
Storage temperature range	Tstg	–65	170	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. These are stress ratings only and functional operation of the device at these or any other conditions beyond those specified in the Electrical Characteristics Table is not implied.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged-device model (CDM), per AEC Q100-011	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input Voltage	V_{REF} + V_{DO}(1)		5.5	V
V_{EN}	Enable Voltage	0		V_{IN}	V
I_L	Output Current	–10		10	mA
T_A	Operating Temperature	–40	25	125	℃

(1) Dropout voltage

7.4 Thermal Information

THERMAL METRIC(1)		DEVICE DBV 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	185	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	156	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	33.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	29.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At V_{IN} = 5.5 V, V_{EN} = V_{IN}, C_{REF} = 10 µF, C_{IN} = 0.1 µF, I_L = 0 mA, minimum and maximum specifications at T_A = –40℃ to 125℃; typical specifications at T_A = 25℃ unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	T_A = 25°C		–0.05		0.05	%
	Output voltage temperature coefficient	–40°C ≤ T_A ≤ 125°C	REF4132 A grade			12	ppm/℃
		–40°C ≤ T_A ≤ 125°C	REF4132 B grade			30	ppm/℃
LINE & LOAD REGULATION							
$\Delta V_{REF}/\Delta V_{IN}$	Line Regulation	V_{REF} + V_{DO} ≤ V_{IN} ≤ 5.5 V			2		ppm/V
		V_{REF} + V_{DO} ≤ V_{IN} ≤ 5.5 V				15	ppm/V
		V_{REF} = 5 V, V_{REF} + V_{DO} ≤ V_{IN} ≤ 5.5 V				55	ppm/V
$\Delta V_{REF}/\Delta I_L$	Load Regulation	I_L = 0 mA to 10mA, V_{IN} = V_{REF} + V_{DO}			20		ppm/mA
		I_L = 0 mA to 10mA, V_{IN} = V_{REF} + V_{DO}				120	ppm/mA
POWER SUPPLY							
V_{IN}	Input voltage			V_{REF} + V_{DO}		5.5	V
I_Q	Quiescent current	Active mode			80	100	µA
		Shutdown mode, V_{EN} = 0 V			2.5	5	µA
V_{EN}	Enable pin Voltage	Voltage reference in active mode (EN=1)		1.6			V
		Voltage reference in shutdown mode (EN=0)				0.5	V
I_{EN}	Enable pin current	V_{EN} = 5.5 V			1	2	µA
V_{DO}	Dropout voltage	I_L = 0 mA			50		mV
		I_L = 0 mA				100	mV
		I_L = 10 mA				500	mV
I_{SC}	Short circuit current (1)	V_{REF} = 0 V			18	11.5	mA
TURNON							
t_{ON}	Turn-on time	0.1% settling, C_L = 1 µF, 10% to 90%			2.5		ms
NOISE							
$e_{n(p-p)}$	Low frequency noise	f = 0.1 Hz to 10 Hz			15		ppm_{p-p}
e_n	Wide band noise	f = 10 Hz to 10 kHz			24		μV_{rms}
HYSTERESIS AND LONG-TERM STABILITY							
	Long-term stability	0 to 1000h at 35℃			30		ppm
V_{HYST}	Output voltage hysteresis	T_A= 25℃ to −40℃ to 125℃ to 25℃			35		ppm
CAPACITIVE LOAD							
C_L	Stable output capacitor range			0.1		10	µF

(1) At higher ambient temperature the short circuit current capacity is limited due to junction temeprature max limit

7.6 Typical Characteristics

at T_A = 25°C, V_{IN} = V_{EN} = 5 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

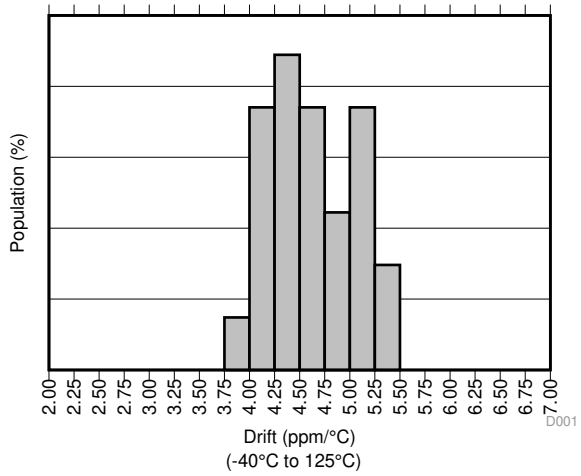


Figure 1. Temperature Drift

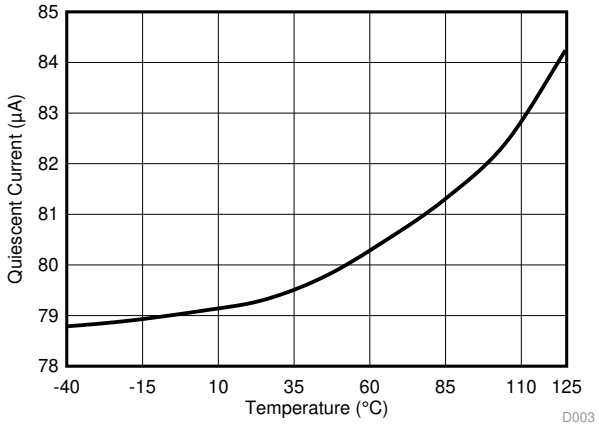


Figure 2. V_{IN} vs I_Q over Temperature

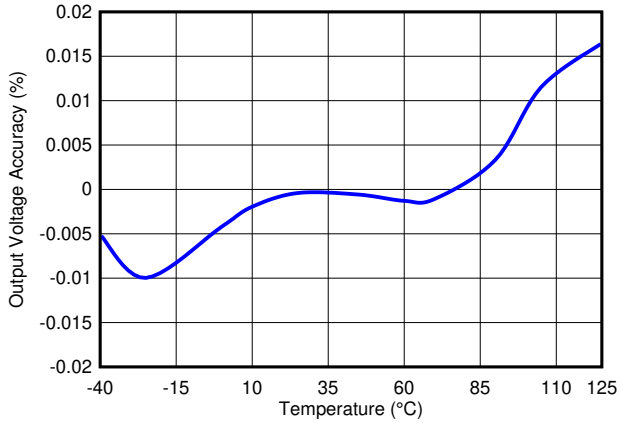


Figure 3. Output Voltage Accuracy vs Temperature

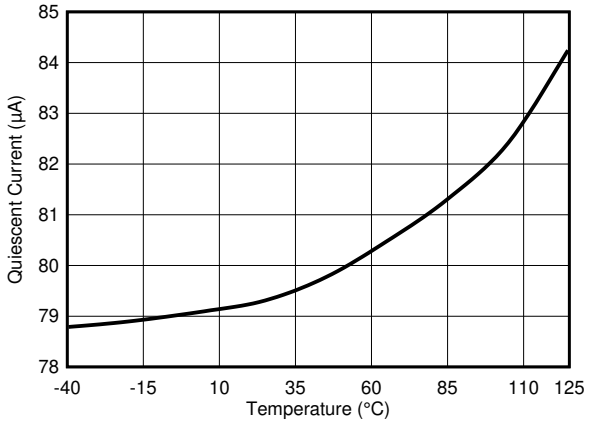


Figure 4. Quiescent Current vs Temperature

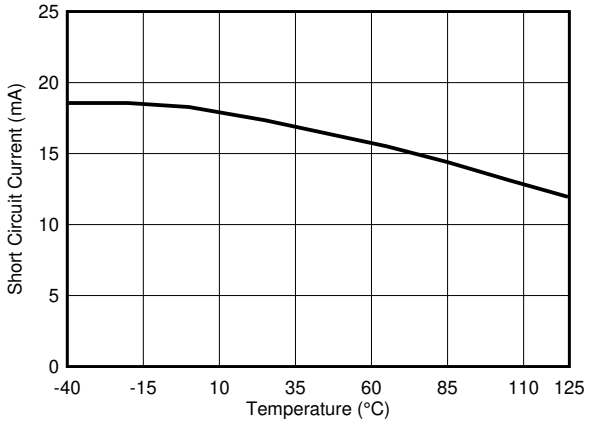


Figure 5. Short Circuit Current

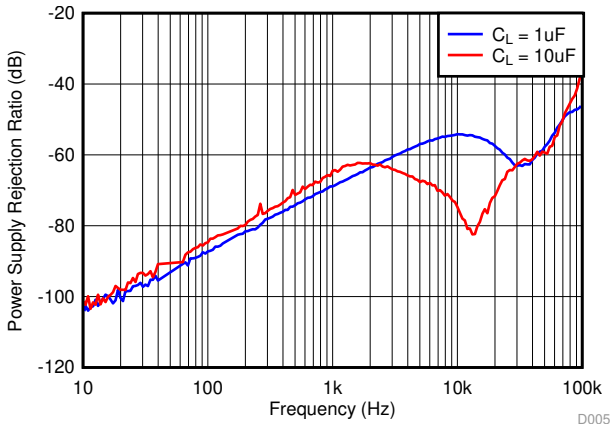


Figure 6. Power-Supply Rejection Ratio vs Frequency

Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 5 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

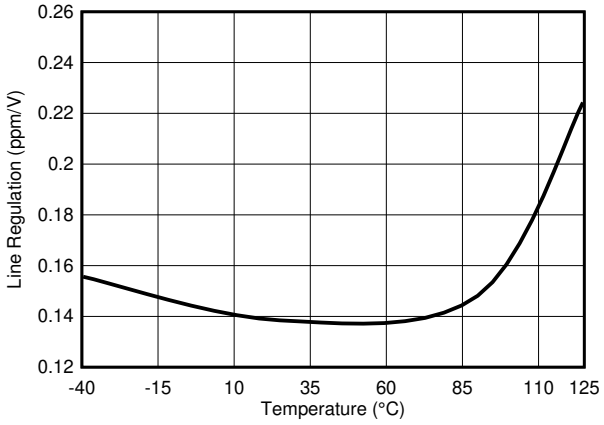


Figure 7. Line Regulation

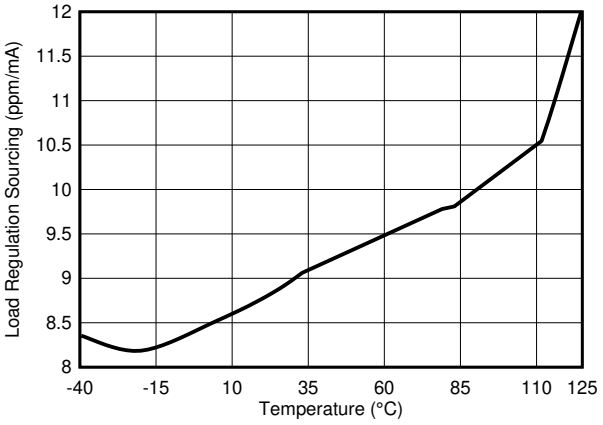


Figure 8. Load Regulation Sourcing

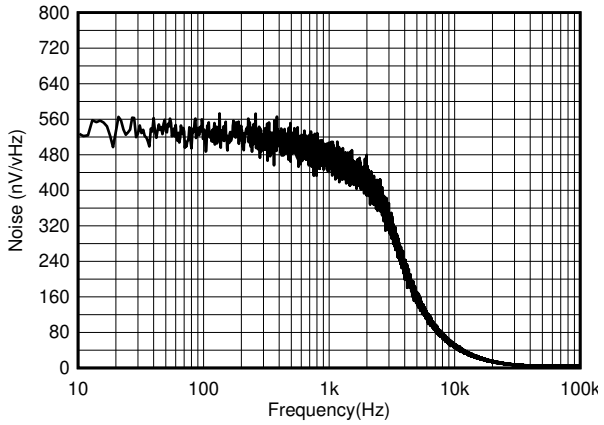


Figure 9. Noise Performance 10 Hz to 10 kHz

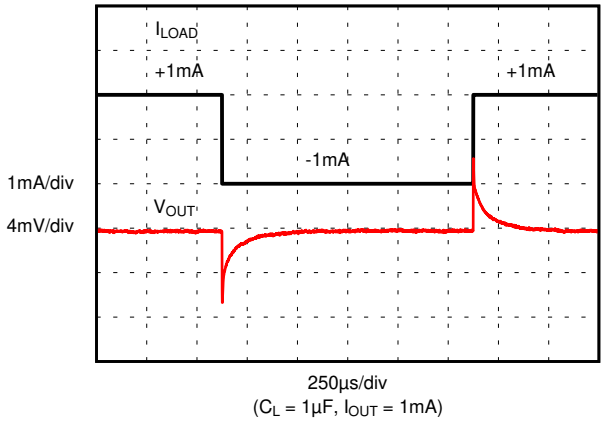


Figure 10. Load Transient

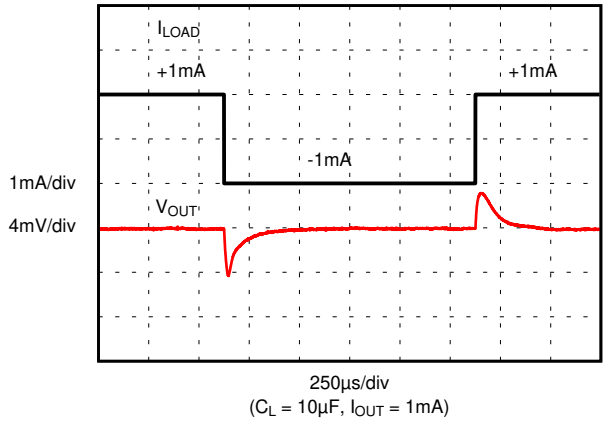


Figure 11. Load Transient

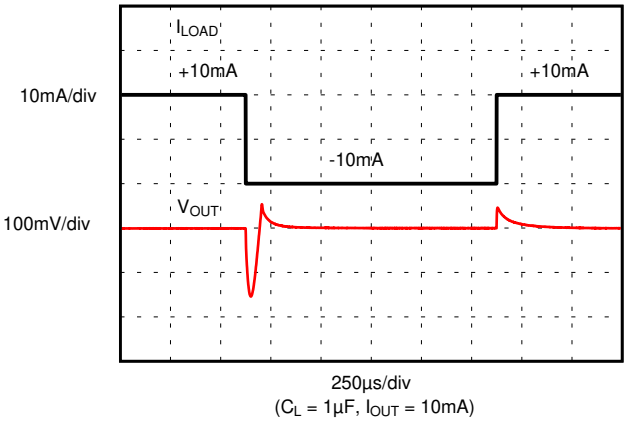


Figure 12. Load Transient

Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 5 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

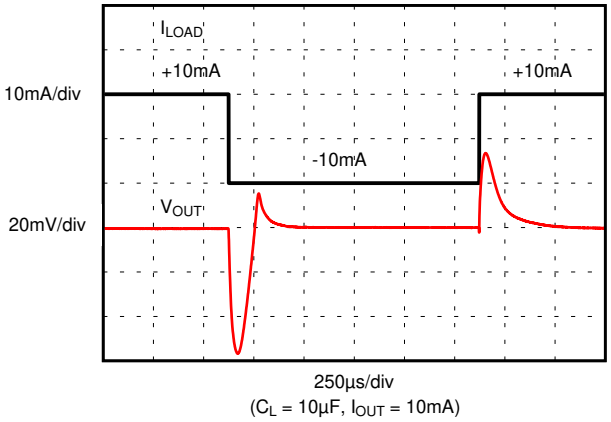


Figure 13. Load Transient

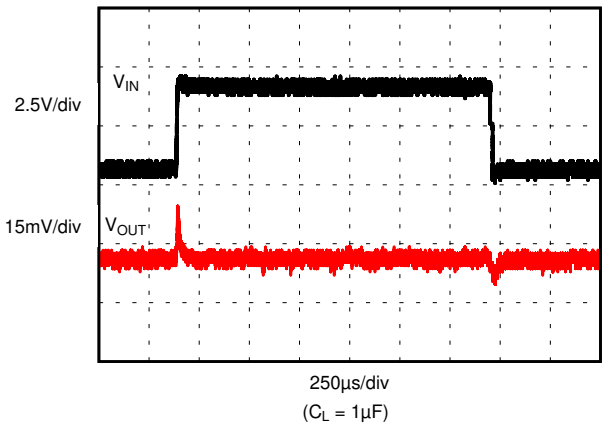


Figure 14. Line Transient

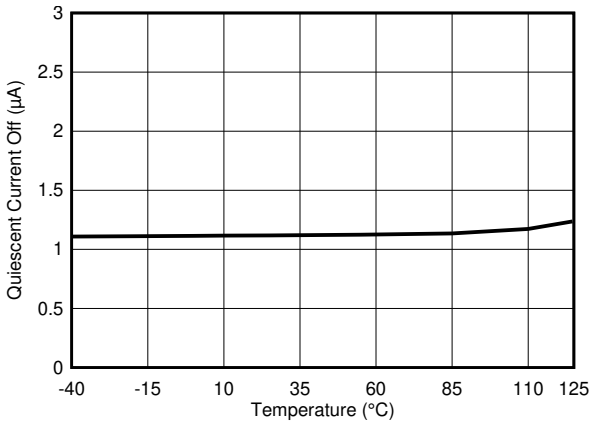


Figure 15. Quiescent Current Shutdown Mode

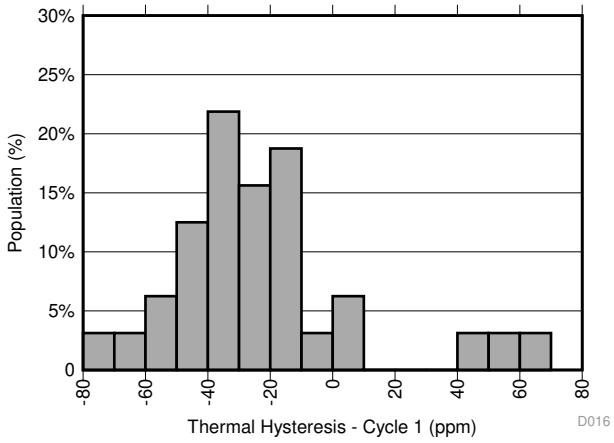


Figure 16. Thermal Hysteresis Distribution (Cycle 1)

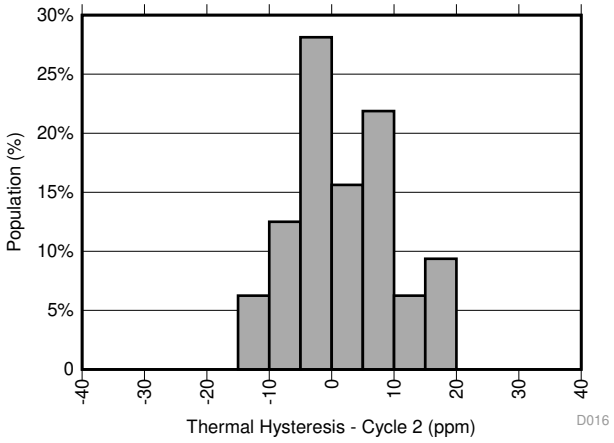


Figure 17. Thermal Hysteresis Distribution (Cycle 2)



Refer to *Solder Heat Shift* for more information

Figure 18. Solder Heat Shift Distribution

Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = 5 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

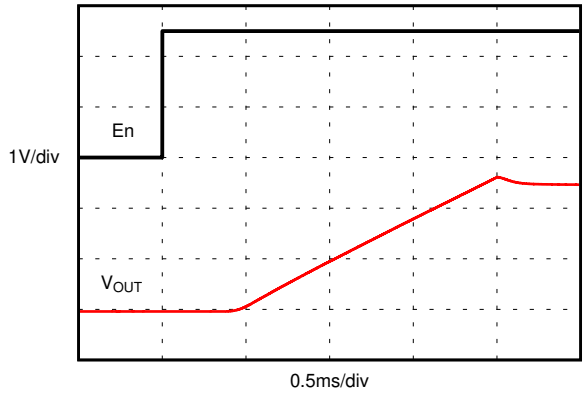


Figure 19. Turnon Time (Enable)

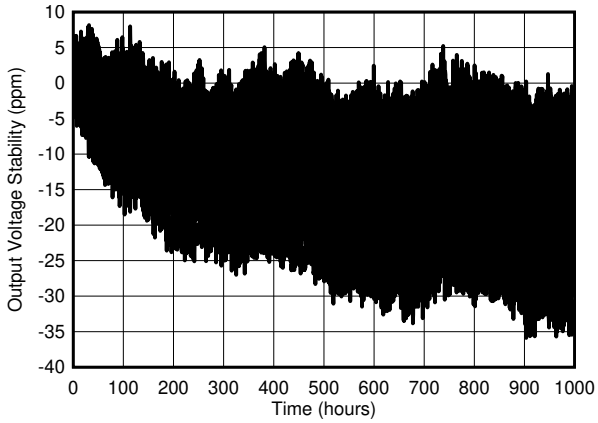


Figure 20. Long Term Stability - 1000 hours (V_{REF})

8 Parameter Measurement Information

8.1 Solder Heat Shift

The materials used in the manufacture of the REF4132-Q1 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 32 devices were soldered on four printed circuit boards [16 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in Figure 21. The printed circuit board is comprised of FR4 material. The board thickness is 1.65 mm and the area is 114 mm × 152 mm.

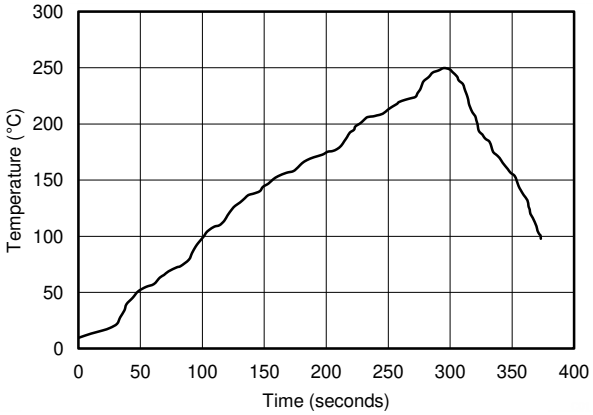


Figure 21. Reflow Profile

The reference output voltage is measured before and after the reflow process; the typical shift is displayed in Figure 22 Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the second pass to minimize its exposure to thermal stress.

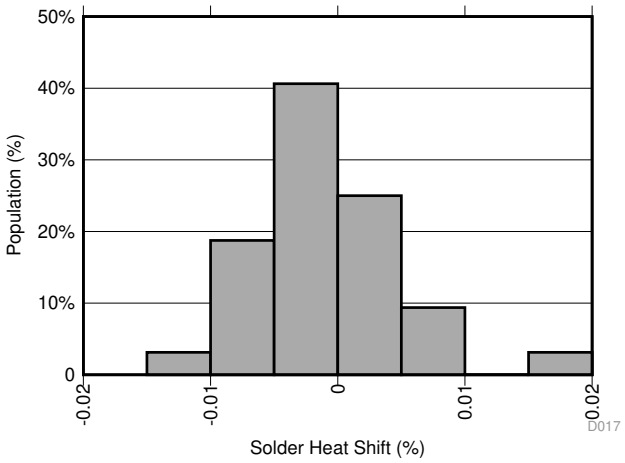


Figure 22. Solder Heat Shift Distribution, V_{REF} (%)

8.2 Long-Term Stability

One of the key parameters of the REF4132-Q1 references is long-term stability. Typical characteristic expressed as: curves shows the typical drift value for the REF4132-Q1 is 25 ppm from 0 to 1000 hours. This parameter is characterized by measuring 32 units at regular intervals for a period of 1000 hours. It is important to understand that long-term stability is not ensured by design and that the output from the device may shift beyond the typical 25 ppm specification at any time. For systems that require highly stable output voltages over long periods of time, the designer should consider burning in the devices prior to use to minimize the amount of output drift exhibited by the reference over time.

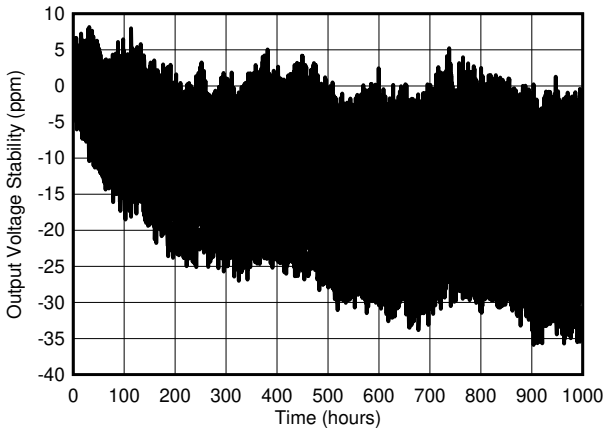


Figure 23. Long Term Stability - 1000 hours (V_{REF})

8.3 Thermal Hysteresis

Thermal hysteresis is measured with the REF4132-Q1 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. The PCB was baked at 150°C for 30 minutes before thermal hysteresis was measured. Hysteresis can be expressed by Equation 1:

$$V_{HYST} \left(\frac{| V_{PRE} - V_{POST} |}{V_{NOM}} \right) \times 10^6 \text{ (ppm)} \quad (1)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to +125°C and returns to 25°C.

Figure 24. Thermal Hysteresis Distribution (V_{REF})

8.4 Power Dissipation

The REF4132-Q1 voltage references are capable of source and sink up to 10 mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to ensure that the device does not exceeded its maximum power dissipation rating. The maximum power dissipation of the device can be calculated with Equation 2:

$$T_J \quad T_A + P_D \times R_{\theta JA}$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance (2)

Because of this relationship, acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the device be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

8.5 Noise Performance

Typical 0.1-Hz to 10-Hz voltage noise can be seen in Figure 25 . Device noise increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care must be taken to ensure the output impedance does not degrade ac performance. Peak-to-peak noise measurement setup is shown in Figure 25.

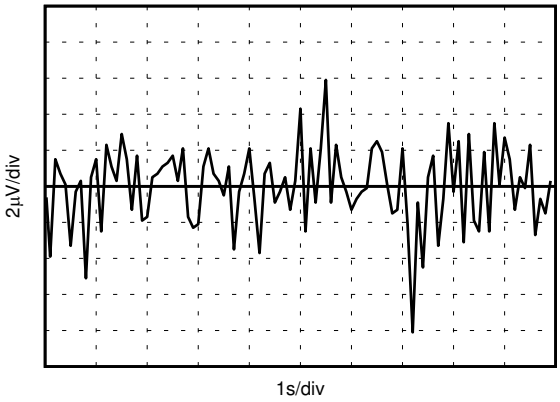


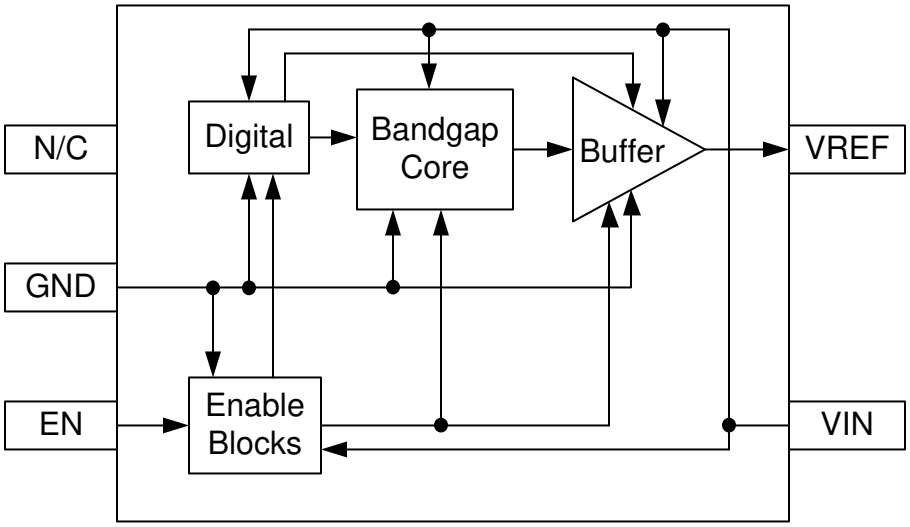
Figure 25. 0.1-Hz to 10-Hz Noise (V_{REF})

9 Detailed Description

9.1 Overview

The REF4132-Q1 is a low-drift, low-power precision bandgap voltage reference that is specifically designed for excellent initial voltage accuracy and drift. The *Functional Block Diagram* is a simplified block diagram of the REF4132-Q1 showing basic band-gap topology.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Supply Voltage

The REF4132-Q1 voltage reference features an extremely low dropout voltage. For loaded conditions, a typical dropout voltage versus load is shown on the front page. The REF4132-Q1 features a low quiescent current that is extremely stable over changes in both temperature and supply. The typical room temperature quiescent current is 75 μA, and the maximum quiescent current over temperature is just 100 μA. Supply voltages below the specified levels can cause the REF4132-Q1 to momentarily draw currents greater than the typical quiescent current. Use a power supply with a fast rising edge and low output impedance to easily prevent this issue.

The supply current vs supply voltage figure is shown in Figure 26.

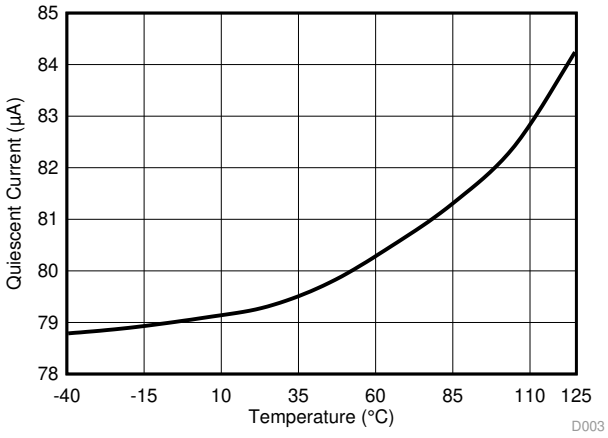


Figure 26. Supply Current vs Supply Voltage

Feature Description (continued)

9.3.2 Low Temperature Drift

The REF4132-Q1 is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by Equation 3:

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF} \times \text{Temperature Range}} \right) \times 10^6 \quad (3)$$

9.3.3 Load Current

The REF4132-Q1 family is specified to deliver a current load of ±10 mA per output. The V_{REF} output of the device are protected from short circuits by limiting the output short-circuit current to 18 mA. The device temperature increases according to Equation 4:

$$T_J \quad T_A + P_D \times R_{\theta JA} \quad (4)$$

where

- T_J = junction temperature (°C),
- T_A = ambient temperature (°C),
- P_D = power dissipated (W), and
- $R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)

The REF4132-Q1 maximum junction temperature must not exceed the absolute maximum rating of 150°C.

9.4 Device Functional Modes

9.4.1 EN Pin

When the EN pin of the REF4132-Q1 is pulled high, the device is in active mode. The device must be in active mode for normal operation. The REF4132-Q1 can be placed in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 2.5 µA (typical) in shutdown mode. The EN pin must not be pulled higher than VIN supply voltage. See the Thermal Information for logic high and logic low voltage levels.

9.4.2 Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF4132-Q1 and OPA735 can be used to provide a dual-supply reference from a 5-V supply. Figure 27 shows the REF4132-Q1 used to provide a 2.5-V supply reference voltage. The low drift performance of the REF4132-Q1 complements the low offset voltage and zero drift of the OPA735 to provide an accurate solution for split-supply applications. Take care to match the temperature coefficients of R1 and R2.

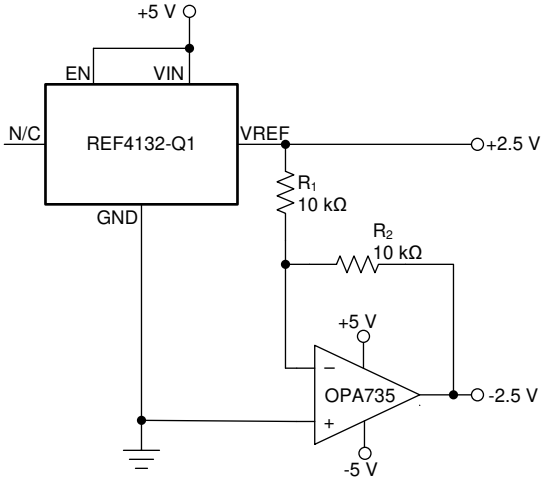


Figure 27. REF4132-Q1 and OPA735 Create Positive and Negative Reference Voltages

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

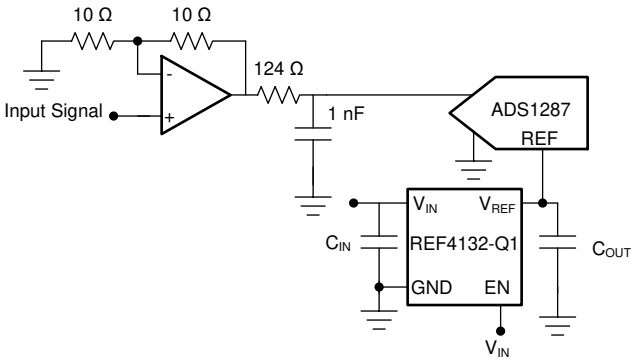
As this device has many applications and setups, there are many situations that this datasheet can not characterize in detail. Basic applications includes positive/negative voltage reference and data acquisition systems. The table below shows the typical application of REF4132-Q1 and its companion ADC.

Table 1. Typical Applications and Companion ADC

Applications	ADC/DAC
HEV/EV	ADS1259-Q1, ADS1015-Q1, ADS7049-Q1
High Temperature Sensor	ADS1118-Q1
Traction Inverter	ADS7049-Q1
Automotive Head Unit	ADS7142-Q1

10.2 Typical Application: Basic Voltage Reference Connection

The circuit shown in Figure 28 shows the basic configuration for the REF4132-Q1 references. Connect bypass capacitors according to the guidelines in *Layout Guidelines*.



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Figure 28. Basic Reference Connection

10.2.1 Design Requirements

A detailed design procedure is described based on a design example. For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage V_{IN}	5 V
Output voltage V_{OUT}	2.5 V
REF4132-Q1 input capacitor	1 µF
REF4132-Q1 output capacitor	10 µF

10.2.2 Detailed Design Procedure

10.2.2.1 Input and Output Capacitors

A 1-μF to 10-μF electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate. Connect an additional 0.1-μF ceramic capacitor in parallel to reduce high frequency supply noise.

A ceramic capacitor of at least a 0.1 μF must be connected to the output to improve stability and help filter out high frequency noise. An additional 1-μF to 10-μF electrolytic or ceramic capacitor can be added in parallel to improve transient performance in response to sudden changes in load current; however, keep in mind that doing so increases the turnon time of the device.

Best performance and stability is attained with low-ESR, low-inductance ceramic chip-type output capacitors (X5R, X7R, or similar). If using an electrolytic capacitor on the output, place a 0.1-μF ceramic capacitor in parallel to reduce overall ESR on the output.

10.2.2.2 V_{IN} Slew Rate Considerations

In applications with slow-rising input voltage signals, the reference exhibits overshoot or other transient anomalies that appear on the output. These phenomena also appear during shutdown as the internal circuitry loses power.

To avoid such conditions, ensure that the input voltage wave-form has both a rising and falling slew rate close to 6 V/ms.

10.2.2.3 Shutdown/Enable Feature

The REF4132-Q1 references can be switched to a low power shut-down mode when a voltage of 0.5 V or lower is input to the ENABLE pin. Likewise, the reference becomes operational for ENABLE voltages of 1.6 V or higher. During shutdown, the supply current drops to less than 5 μA, useful in applications that are sensitive to power consumption.

If using the shutdown feature, ensure that the ENABLE pin voltage does not fall between 0.5 V and 1.6 V because this causes a large increase in the supply current of the device and may keep the reference from starting up correctly. If not using the shutdown feature, however, the ENABLE pin can simply be tied to the IN pin, and the reference remains operational continuously.

10.2.3 Application Curves

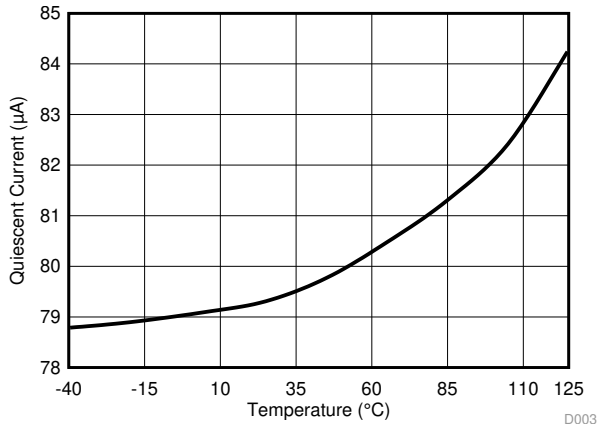


Figure 29. Quiescent Current vs Temperature

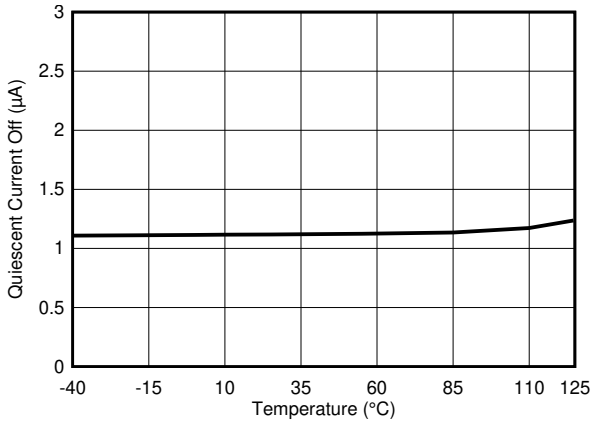


Figure 30. Quiescent Current Shutdown Mode

11 Power Supply Recommendations

The REF4132-Q1 family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 50 mV above the output voltage. TI recommends a supply bypass capacitor ranging between 0.1 µF to 10 µF.

12 Layout

12.1 Layout Guidelines

Figure 31 illustrates an example of a PCB layout for a data acquisition system using the REF4132-Q1. Some key considerations are:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors at V_{IN}, V_{REF} of the REF4132-Q1.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

12.2 Layout Example

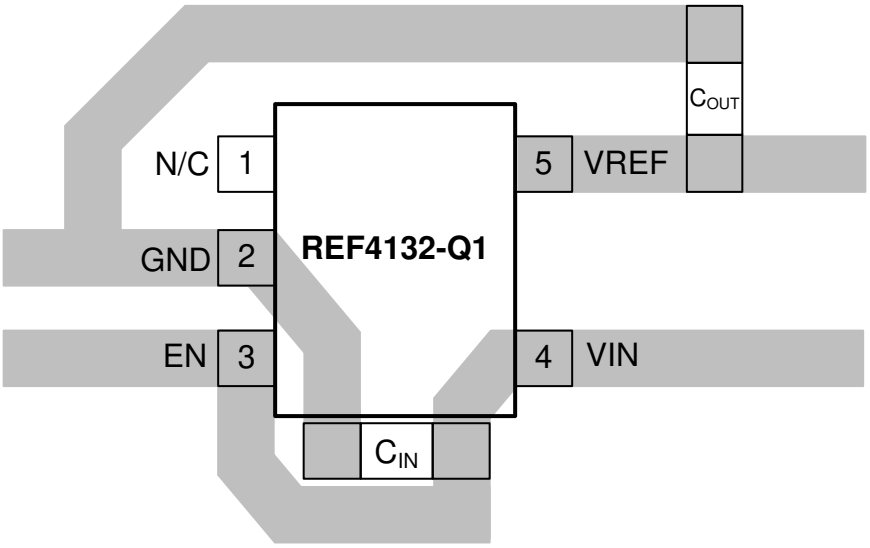


Figure 31. Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors*
- *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design*

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF4132A25DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25MC	Samples
REF4132A30DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25NC	Samples
REF4132A33DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25OC	Samples
REF4132A40DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25PC	Samples
REF4132A50DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25QC	Samples
REF4132B25DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25XC	Samples
REF4132B30DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25RC	Samples
REF4132B33DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25SC	Samples
REF4132B40DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25TC	Samples
REF4132B50DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	25VC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF REF4132-Q1 :

- Catalog : REF4132

NOTE: Qualified Version Definitions:

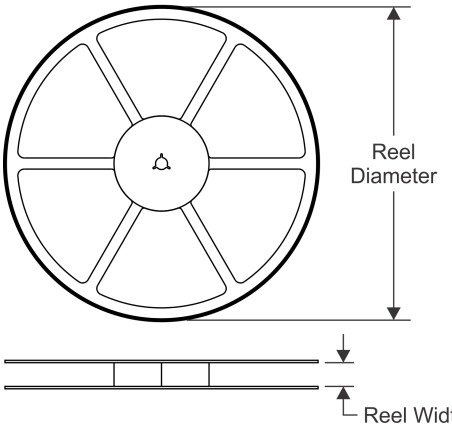
- Catalog - TI's standard catalog product

PACKAGE MATERIALS INFORMATION

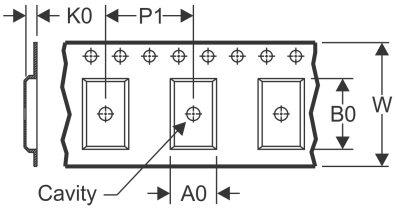
29-Aug-2020

TAPE AND REEL INFORMATION

REEL DIMENSIONS

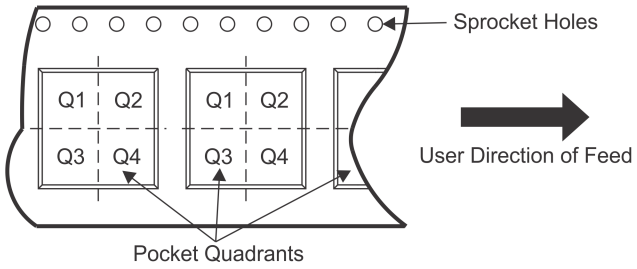


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



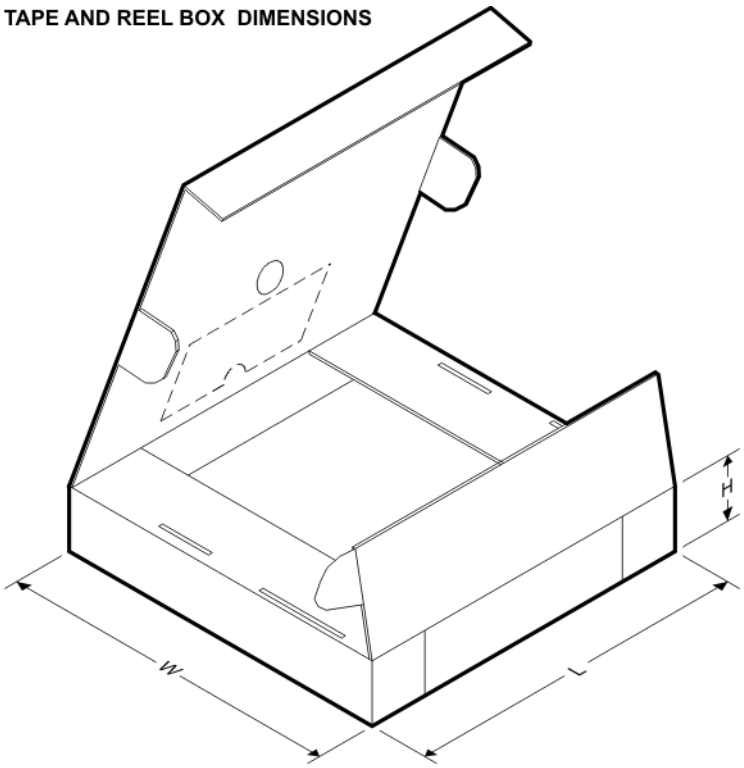
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF4132A25DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF4132A30DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF4132A33DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF4132A40DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF4132A50DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF4132B25DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF4132B30DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF4132B33DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF4132B40DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
REF4132B50DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

29-Aug-2020

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

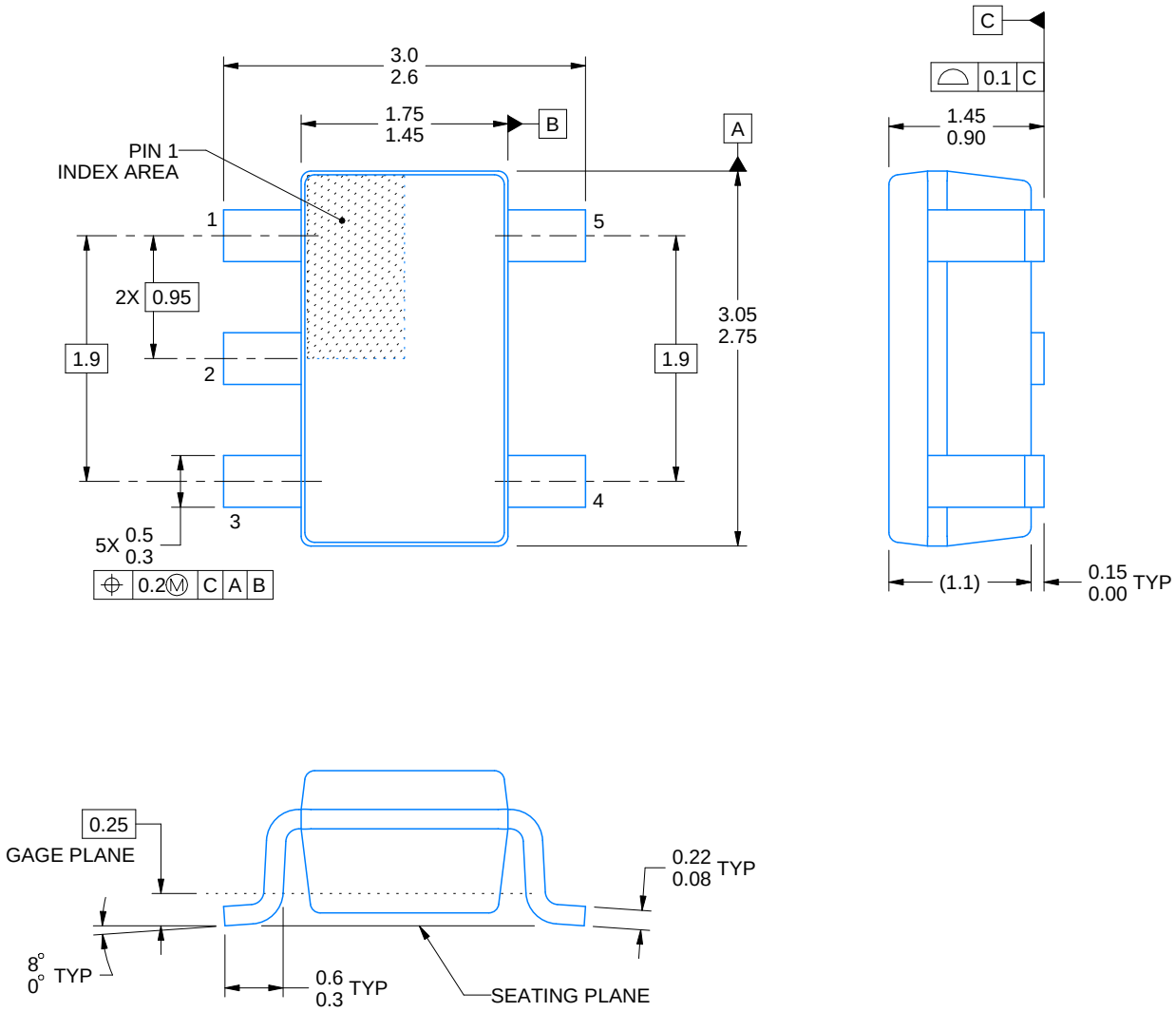
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF4132A25DBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF4132A30DBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF4132A33DBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF4132A40DBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF4132A50DBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF4132B25DBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF4132B30DBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF4132B33DBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF4132B40DBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0
REF4132B50DBVRQ1	SOT-23	DBV	5	3000	213.0	191.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/F 06/2021

NOTES:

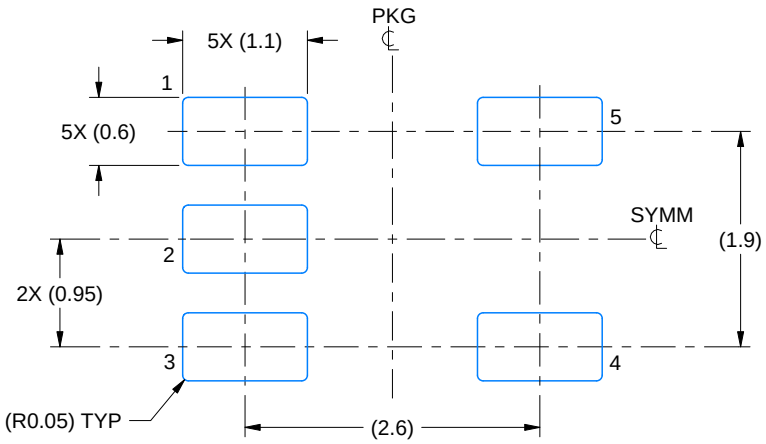
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

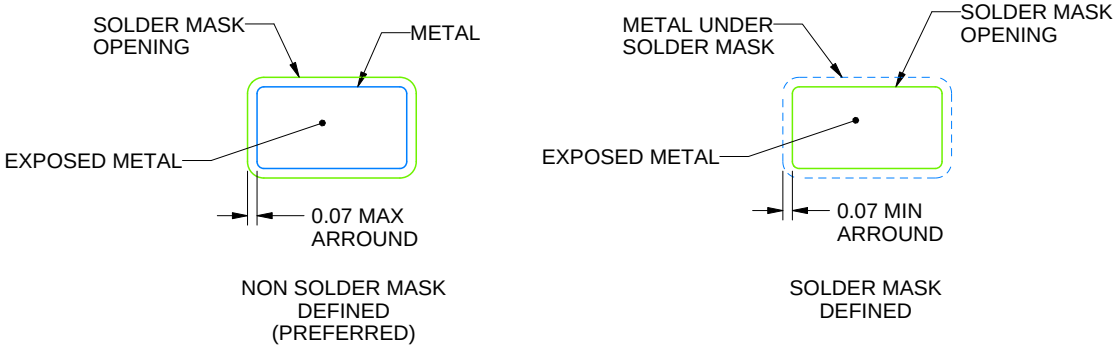
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/F 06/2021

NOTES: (continued)

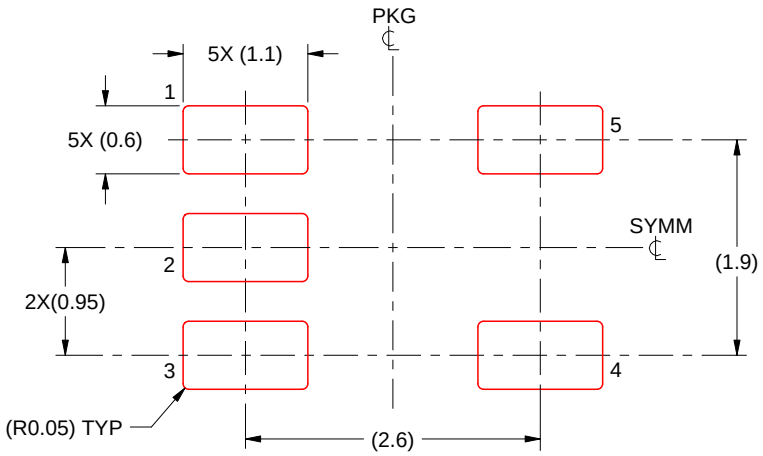
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/F 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.