SGM25730Q
TVS-less Automotive Reverse Battery Protection Ideal Diode Controller

GENERAL DESCRIPTION

The SGM25730Q, an ideal diode controller used as an ideal diode rectifier with external NMOS, offers low-loss reverse polarity protection, which has a mere 20mV forward voltage drop. Designed for automotive 12V power systems, this solution effectively addresses cold crank challenges through its extended operational capability down to 3.2V input voltage. The controller's minimal voltage loss and robust protection features make it particularly advantageous for vehicle power management applications requiring high reliability under extreme conditions.

Controlling the GATE of MOSFET, the device regulates the 20mV forward voltage drop. During a reverse current event, the SGM25730Q ensures smooth turn-off of the MOSFET, effectively preventing any steady-state reverse current. With a rapid reverse current blocking response time of less than 1.1μs, the device is well-suited for applications requiring output voltage hold-up during ISO7637 pulse tests, as well as during input micro-short and power fail scenarios.

The SGM25730Q integrates the function of V_{DS} clamp, which enables TVS-less input polarity protection, typically saving 60% PCB space in constrained automotive systems.

This controller incorporates a charge pump gate driver for an external NMOS. Its high voltage rating simplifies system designs for automotive EMC transient interference standard ISO7637. When the enable pin is low, the controller is deactivated and consumes approximately 1μA of current.

The device is AEC-Q100 qualified (Automotive Electronics Council (AEC) standard Q100 Grade 1) and it is suitable for automotive applications.

The SGM25730Q is available in a Green TSOT-23-8 package.

FEATURES

- **AEC-Q100 Qualified for Automotive Applications**
  Device Temperature Grade 1
  T_A = -40℃ to +125℃
- **3.2V to 65V Input Range (3.9V Start-Up)**
- **-33V Reverse Voltage Rating**
- **Charge Pump for External NMOS**
- **Regulation of 20mV Forward Voltage Drop from ANODE to CATHODE**
- **1μA Shutdown Current (EN = Low)**
- **80μA Operating Quiescent Current (EN = High)**
- **1.5A Peak Gate Turn-Off Current**
- **Quick Response Time to Reverse Current Blocking: < 1.1μs**
- **Integrated SW Terminal for Battery Voltage Sensing**
- **Compliance with Automotive ISO7637 Transient Requirements in TVS-less Implementation**
- **Available in a Green TSOT-23-8 Package**

APPLICATIONS

Automotive Infotainment Systems: Telematics Control and Head Unit
Automotive ADAS Systems: Camera Integration
Automotive USB Hubs
Active ORing for Redundant Power Systems

SIMPLIFIED SCHEMATIC

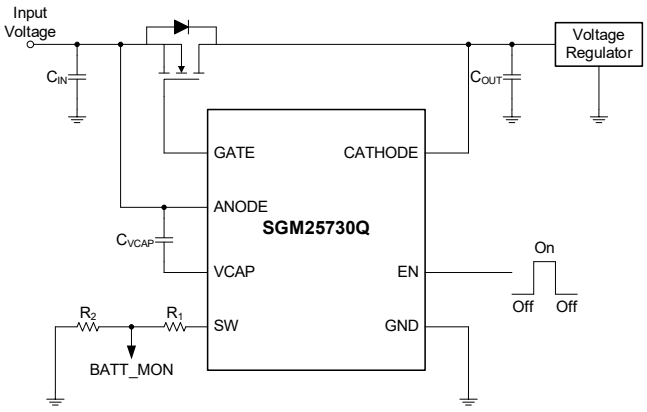


Figure 1. Simplified Schematics

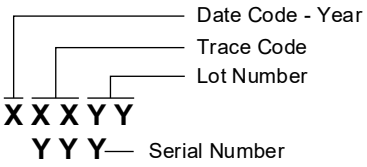
代理商 威尔逊 www.viswie.com 联系电话 138 2526 5270

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM25730Q	TSOT-23-8	-40℃ to +125℃	SGM25730QTN8G/TR	XXXYY 1TJ	Tape and Reel, 3000

MARKING INFORMATION

NOTE: XXXYY = Date Code, Trace Code and Lot Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Input Pins
- ANODE to GND ..... -(V_{CLAMP} - 1)V to 65V
- SW, EN to GND, (V_{ANODE} > 0V)..... -0.3V to 65V
- EN to GND, (V_{ANODE} ≤ 0V) ..... V_{ANODE} to 65V + V_{ANODE}
- SW to GND, (V_{ANODE} ≤ 0V)..... V_{ANODE} to 0.3V + V_{ANODE}
- I_{SW} ..... -1mA to 10mA

Output Pins
- GATE to ANODE ..... -0.3V to 15V
- VCAP to ANODE ..... -0.3V to 15V

Output to Input Pins
- CATHODE to ANODE..... -0.5V to V_{CLAMP}

Package Thermal Resistance
- TSOT-23-8, θ_{JA} ..... 125.5℃/W
- TSOT-23-8, θ_{JB} ..... 47.1℃/W
- TSOT-23-8, θ_{JC} ..... 82.5℃/W

Junction Temperature.....+150℃

Storage Temperature Range .....-65℃ to +150℃

Lead Temperature (Soldering, 10s).....+260℃

ESD Susceptibility (1) (2)

HBM.....±2000V

CDM .....±1000V

NOTES:

1. For human body model (HBM), all pins comply with AEC-Q100-002 specification.

2. For charged device model (CDM), all pins comply with AEC-Q100-011 specification.

RECOMMENDED OPERATING CONDITIONS

Input Pins
- ANODE to GND.....-33V to 60V
- CATHODE to GND 60V
- EN to GND.....-33V to 60V

Input to Output Pins
- ANODE to CATHODE .....-V_{CLAMP} to 5V

External Capacitance
- ANODE..... 0.1μF to 1μF
- VCAP to ANODE .....≥ 0.1μF

External MOSFET Max V_{GS} Rating
- GATE to ANODE ..... ≥ 15V

Operating Junction Temperature Range ..... -40℃ to +150℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

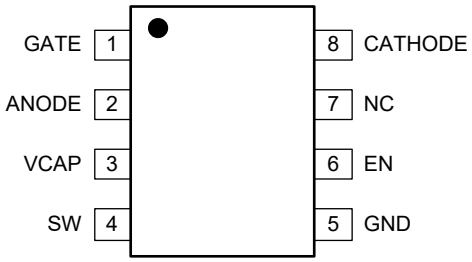
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

SGM25730Q (TOP VIEW)



TSOT-23-8

PIN DESCRIPTION

PIN	NAME	TYPE (1)	FUNCTION
1	GATE	O	Gate Drive Output. This pin is connected to the gate of the external MOSFET.
2	ANODE	I	Anode of the Diode and Input Power. This pin is connected to the source of the external MOSFET.
3	VCAP	O	Charge Pump Output. This pin is connected to external charge pump capacitor.
4	SW	O	Voltage Sensing Disconnect Switch Terminal. EN high connects ANODE to SW internally, enabling battery voltage monitoring via a resistor ladder to GND; EN low turns the switch off, disconnecting the ladder to cut off leakage current.
5	GND	G	Ground.
6	EN	I	Enable. This pin is connected to ANODE during always on operation.
7	NC	—	No Connection.
8	CATHODE	I	Cathode of the Diode. This pin is connected to the drain of the external MOSFET.

NOTE:

1. I = input, O = output, G = ground.

ELECTRICAL CHARACTERISTICS

(T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, V_{ANODE} = 12V, C_{VCAP} = 0.1μF, V_{EN} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{ANODE} Supply Voltage						
$V_{CATHODE_to_ANODE}$ Clamp Voltage	V_{CLAMP}		34		43	V
Operating Input Voltage	V_{ANODE}		4		60	V
V_{ANODE} POR Rising Threshold	V_{ANODE_POR}				3.9	V
V_{ANODE} POR Falling Threshold			2.6	2.8	3.0	V
V_{ANODE} POR Hysteresis	$V_{ANODE_POR_HYS}$		0.76	0.9	1.03	V
Shutdown Supply Current	I_{SD}	V_{EN} = 0V		1	3	μA
Operating Quiescent Current	I_Q			80	130	μA
Enable Input						
Enable Input Low Threshold	V_{EN_IL}		0.66	0.98	1.29	V
Enable Input High Threshold	V_{EN_IH}		1.77	2.09	2.40	V
Enable Hysteresis	V_{EN_HYS}		0.78	1.11	1.43	V
Enable Sink Current	I_{EN}	V_{EN} = 12V		2	3	μA
V_{ANODE} to $V_{CATHODE}$						
Regulated Forward V_{AK} Threshold	V_{AK_REG}		10	20	29	mV
V_{AK} Threshold for Full Conduction Mode	V_{AK}		30	45	62	mV
V_{AK} Threshold for Reverse Current Blocking	V_{AK_REV}		-22	-11	-1	mV
Regulation Error AMP Transconductance (1)	Gm		1200	1800	3100	μA/V
Switch						
Battery Sensing Disconnect Switch Resistance	R_{SW}	V_{ANODE} = 4V to 60V	5	22	43	Ω
Gate Drive						
Peak Source Current	I_{GATE}	V_{ANODE} - $V_{CATHODE}$ = 100mV, V_{GATE} - V_{ANODE} = 5V	6.5	8		mA
Peak Sink Current		V_{ANODE} - $V_{CATHODE}$ = -100mV, V_{GATE} - V_{ANODE} = 5V		1500		mA
Regulation Max Sink Current		V_{ANODE} - $V_{CATHODE}$ = 0V, V_{GATE} - V_{ANODE} = 5V	5	24		μA
Discharge Switch R_{DSON}	R_{DSON}	V_{ANODE} - $V_{CATHODE}$ = -100mV, V_{GATE} - V_{ANODE} = 100mV	0.2		2.3	Ω

ELECTRICAL CHARACTERISTICS (continued)

(T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, V_{ANODE} = 12V, C_{VCAP} = 0.1μF, V_{EN} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charge Pump						
Charge Pump Source Current (Charge Pump On)	I_{VCAP}	V_{VCAP} - V_{ANODE} = 7V	170	300	430	μA
Charge Pump Sink Current (Charge Pump Off)		V_{VCAP} - V_{ANODE} = 13V		4.4	10	μA
Charge Pump Voltage at V_{ANODE} = 3.2V	V_{VCAP} - V_{ANODE}	I_{VCAP} ≤ 10μA	7.5			V
Charge Pump Turn On Voltage			8.6	9.8	11.2	V
Charge Pump Turn Off Voltage			9.5	10.7	12.1	V
Charge Pump Enable Comparator Hysteresis			0.7	1.0	1.2	V
V_{VCAP} - V_{ANODE} UV Release	V_{VCAP_UVLO}	V_{ANODE} - $V_{CATHODE}$ = 100mV, rising edge	4.95	5.86	6.89	V
V_{VCAP} - V_{ANODE} UV Threshold		V_{ANODE} - $V_{CATHODE}$ = 100mV, falling edge	4.16	5.01	5.95	V
CATHODE						
CATHODE Sink Current	$I_{CATHODE}$	V_{ANODE} = 12V, V_{ANODE} - $V_{CATHODE}$ = -100mV		1.0	1.7	μA
		V_{ANODE} - $V_{CATHODE}$ = -100mV		1.0	1.7	
		V_{ANODE} = -14V, V_{DRAIN} = 0V		5	8	
		V_{ANODE} = -16V, $V_{CATHODE}$ = 16V		10	14	

NOTE:

1. Guaranteed by design, not tested in production.

SWITCHING CHARACTERISTICS

(T_J = -40℃ to +125℃, typical values are measured at T_J = +25℃, V_{ANODE} = 12V, C_{VCAP} = 0.1μF, V_{EN} = 3.3V, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Enable (Low to High) to Gate Turn On Delay	EN_{TDLY}	V_{VCAP} > V_{VCAP_UVLOR}		123	180	μs
Reverse Voltage Detection to Gate Turn Off Delay	$t_{Reverse_Delay}$	V_{ANODE} - $V_{CATHODE}$ = 100mV to -100mV		0.4	1.1	μs
Forward Voltage Detection to Gate Turn On Delay	$t_{Forward_Recovery}$	V_{ANODE} - $V_{CATHODE}$ = -100mV to 700mV (10%)		0.8	2.0	μs
		V_{ANODE} - $V_{CATHODE}$ = -100mV to 700mV (90%)		16		

PARAMETER MEASUREMENT INFORMATION

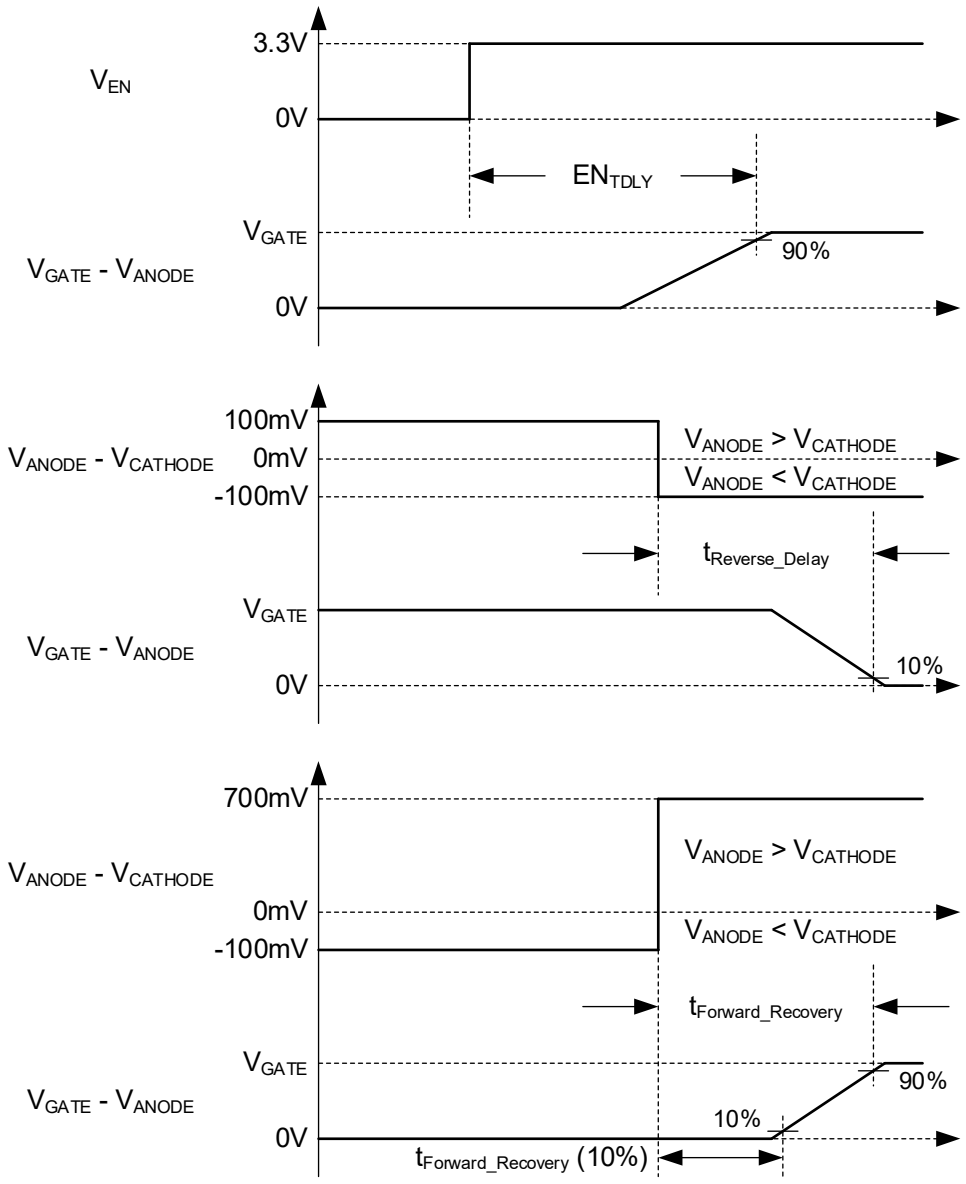
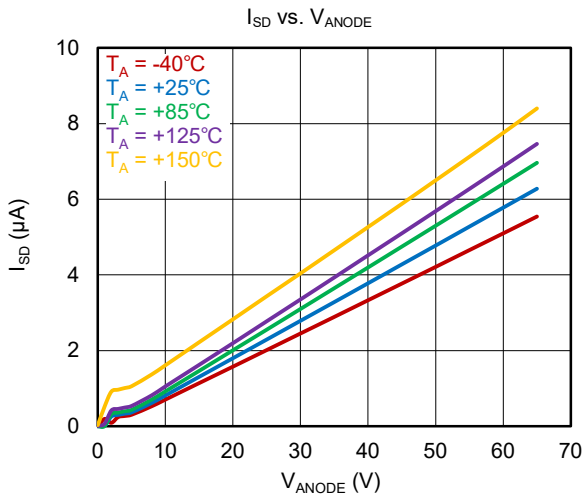
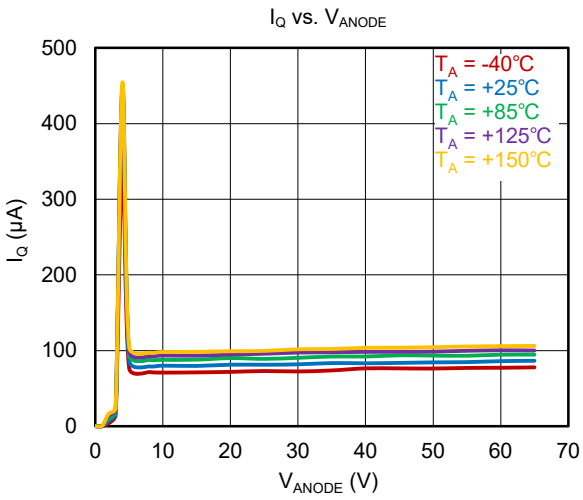
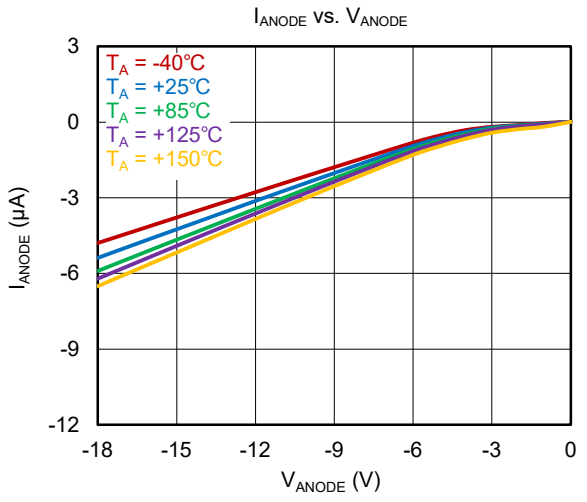


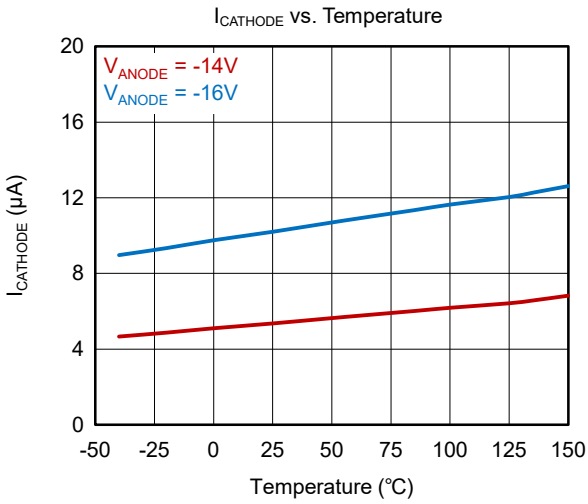
Figure 2. Timing Waveforms

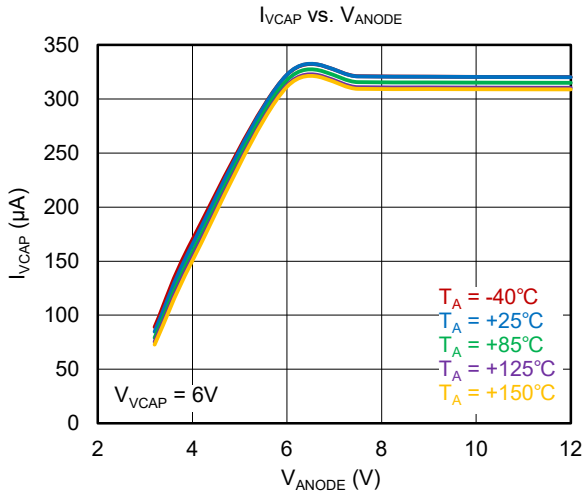
TYPICAL PERFORMANCE CHARACTERISTICS

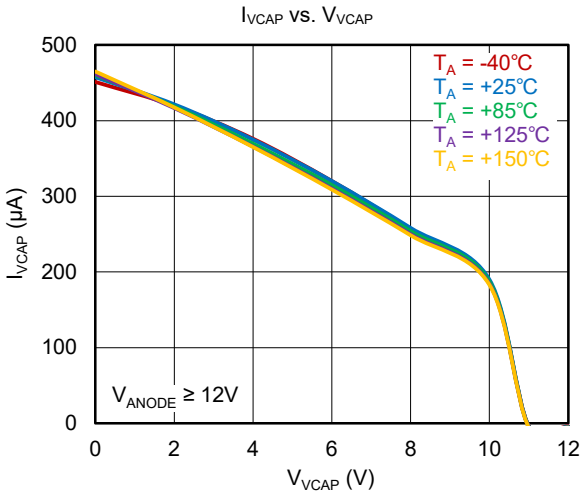






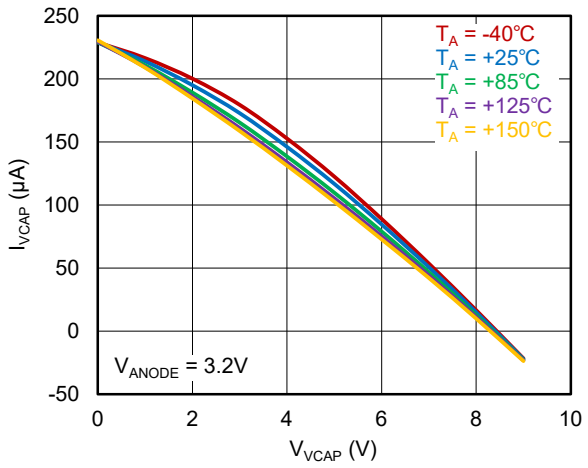




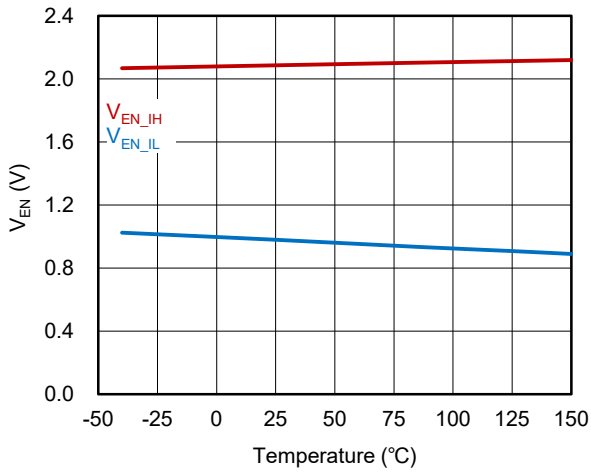


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

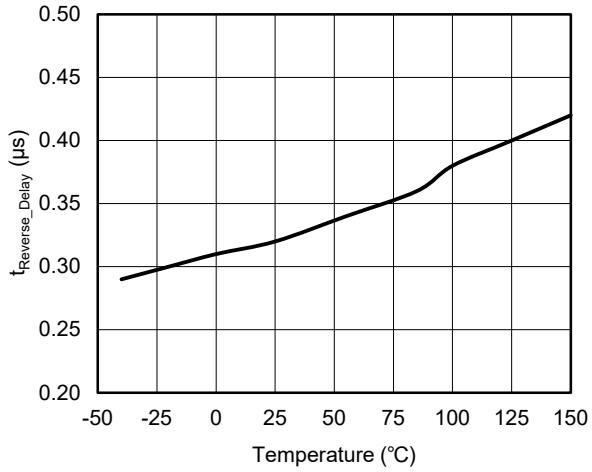
I_{VCAP} vs. V_{VCAP}



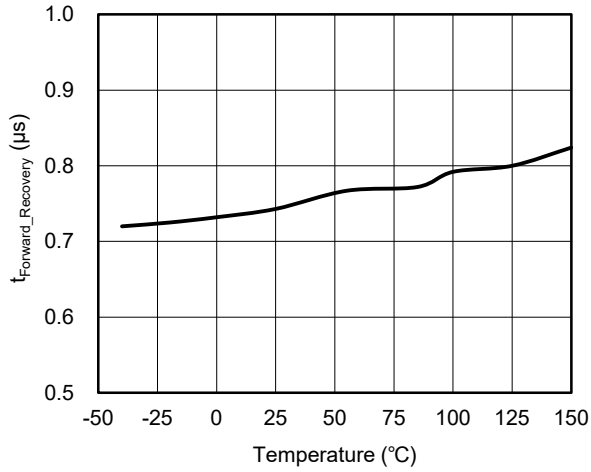
V_{EN} vs. Temperature



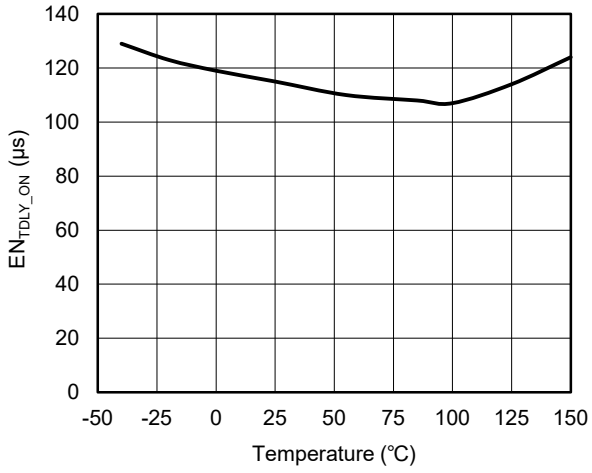
$t_{Reverse_Delay}$ vs. Temperature



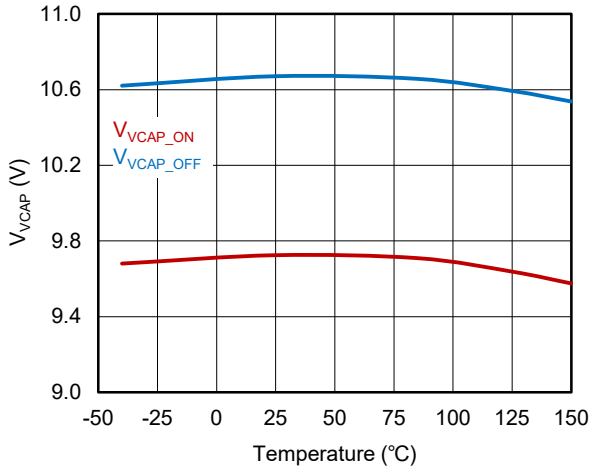
$t_{Forward_Recovery}$ vs. Temperature



EN_{TDLY_ON} vs. Temperature

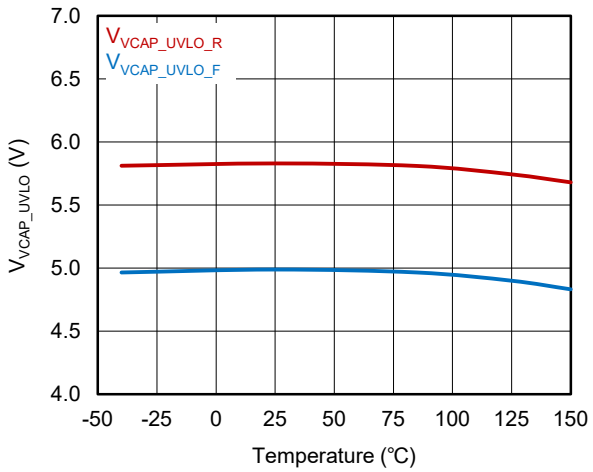


V_{VCAP} vs. Temperature

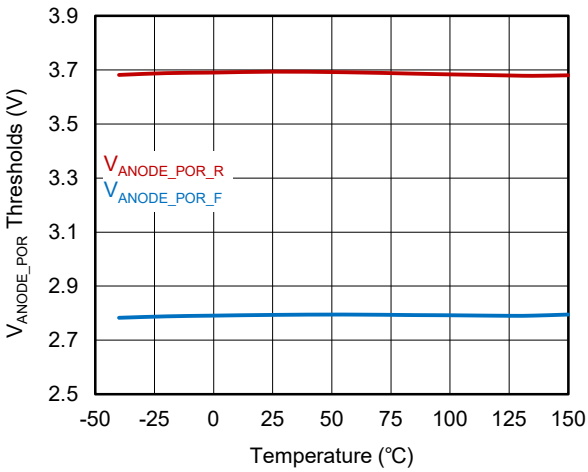


TYPICAL PERFORMANCE CHARACTERISTICS (continued)

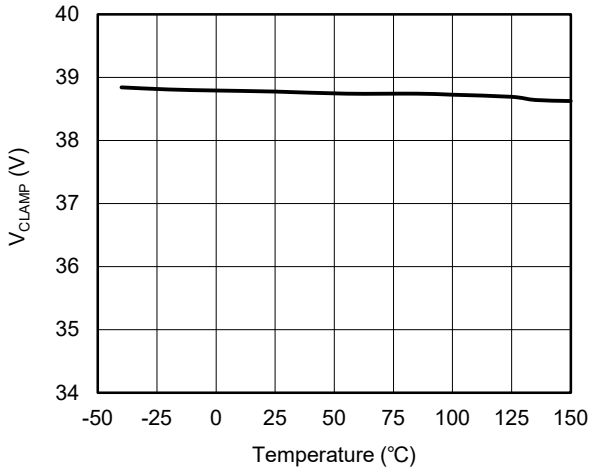
V_{VCAP_UVLO} vs. Temperature



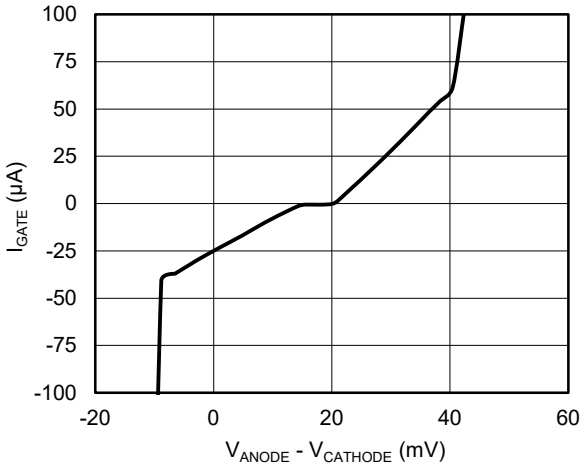
V_{ANODE_POR} Thresholds vs. Temperature



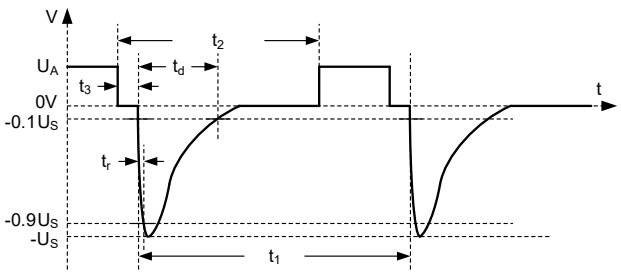
V_{CLAMP} vs. Temperature



I_{GATE} vs. Forward Voltage Drop



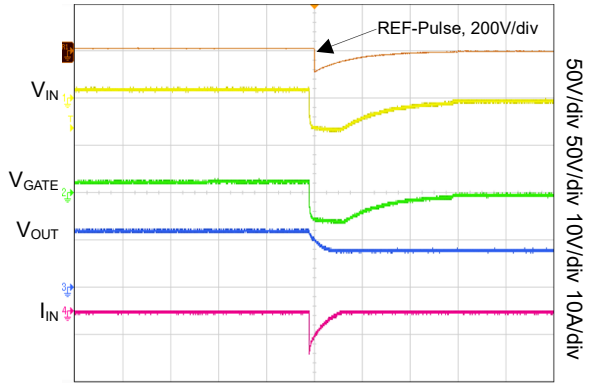
ISO7637-2 Pulse 1



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

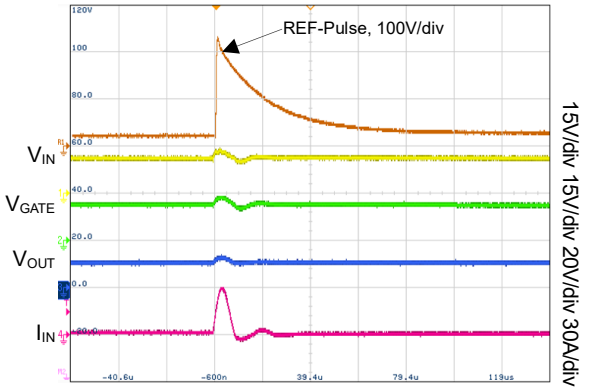
T_A = +25℃, C_{VCAP} = 0.1μF, C_{OUT} = 470μF, unless otherwise noted.

Response to ISO7637-2 Pulse 1



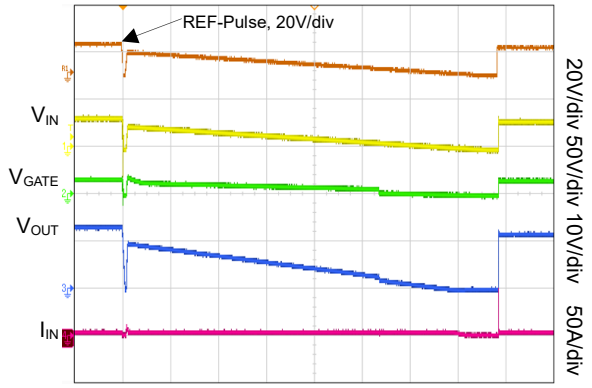
Time (1ms/div)

Response to ISO7637-2 Pulse 2a



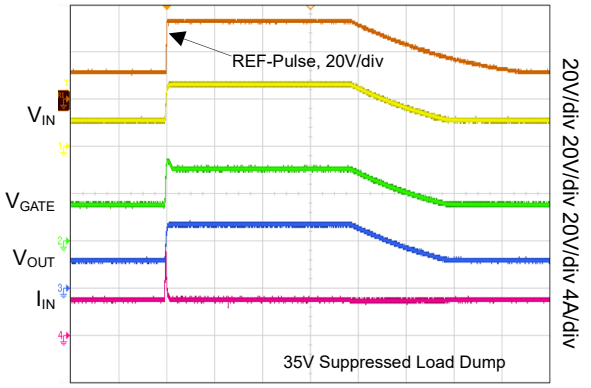
Time (20μs/div)

Response to ISO7637-2 Pulse 2b



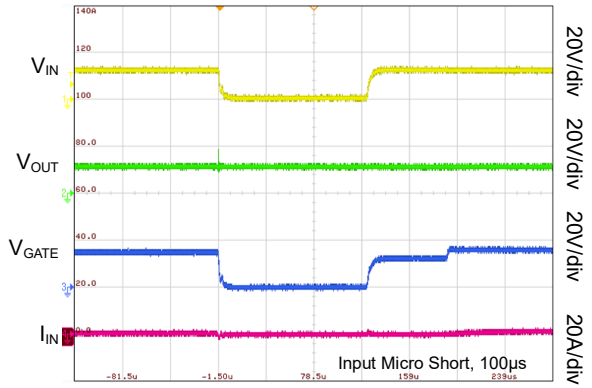
Time (30ms/div)

Response to ISO16750 Pulse 5b



Time (50ms/div)

Response to LV124 E-10

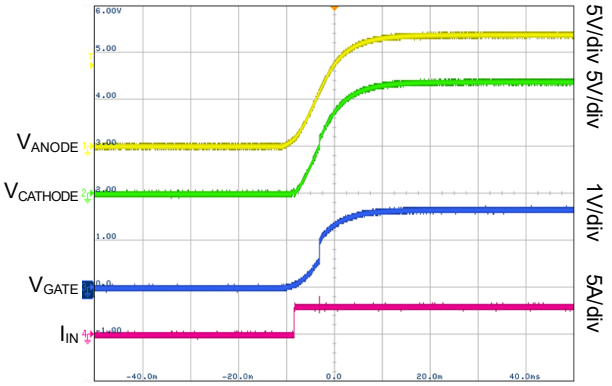


Time (40μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

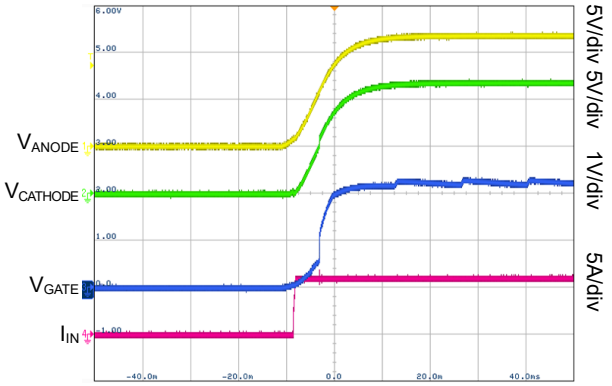
T_A = +25℃, C_{VCAP} = 0.1μF, C_{OUT} = 470μF, unless otherwise noted.

Start-Up with 3A Load



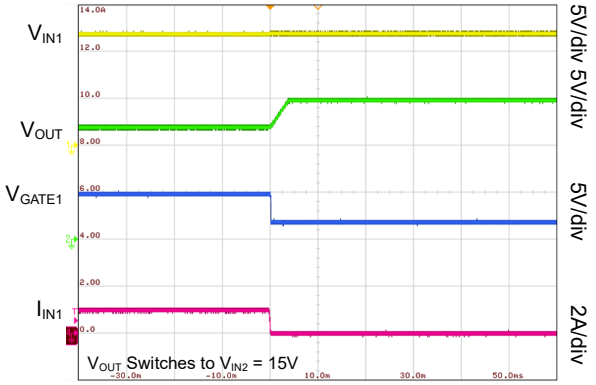
Time (10ms/div)

Start-Up with 6A Load



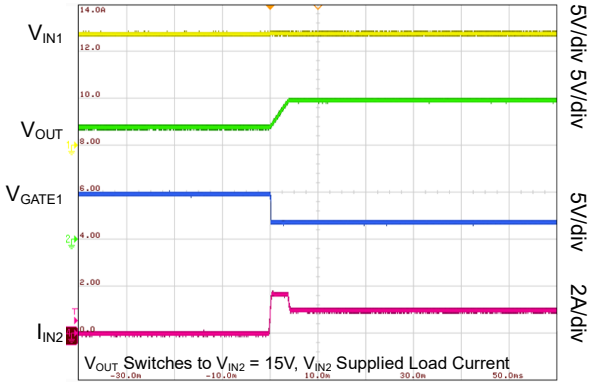
Time (10ms/div)

ORing - V_{IN1} to V_{IN2} Switch Over



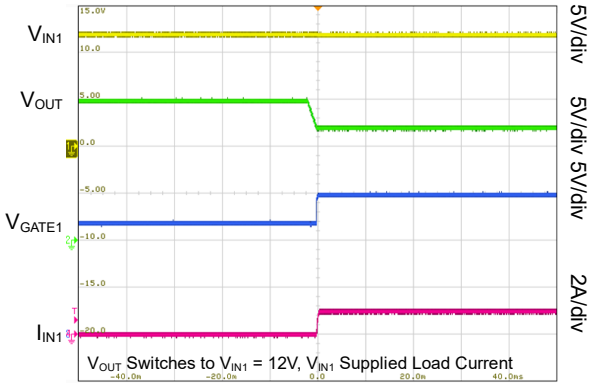
Time (10ms/div)

ORing - V_{IN1} to V_{IN2} Switch Over



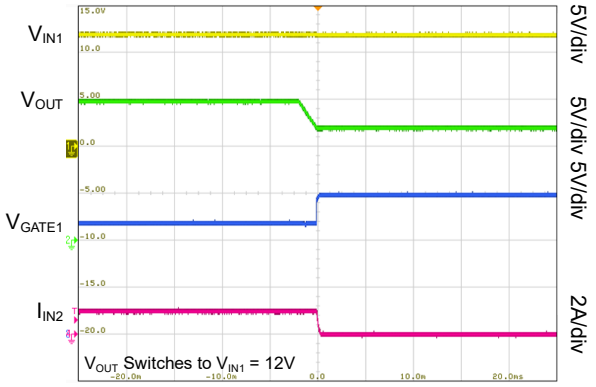
Time (10ms/div)

ORing - V_{IN2} to V_{IN1} Switch Over



Time (10ms/div)

ORing - V_{IN2} to V_{IN1} Switch Over

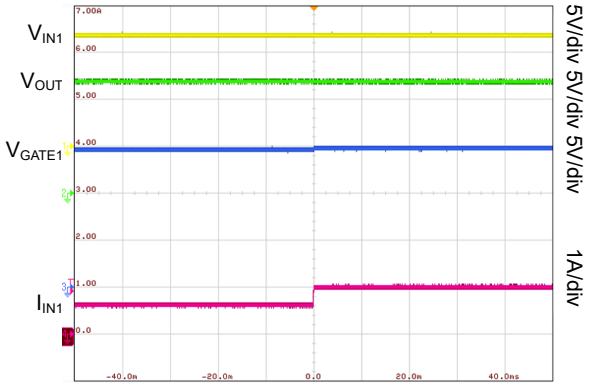


Time (5ms/div)

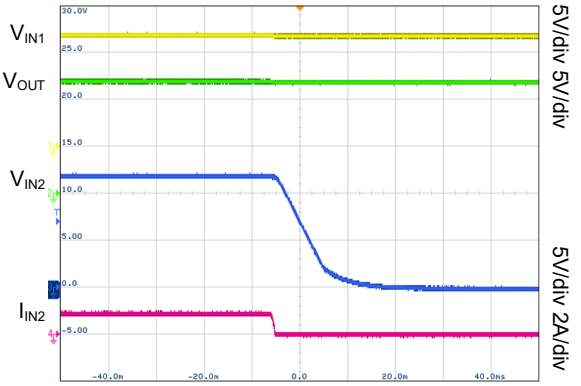
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, C_{VCAP} = 0.1μF, C_{OUT} = 470μF, unless otherwise noted.

ORing - V_{IN2} Fail and Switch Over to V_{IN1}



ORing - V_{IN2} Fail and Switch Over to V_{IN1}



FUNCTIONAL BLOCK DIAGRAM

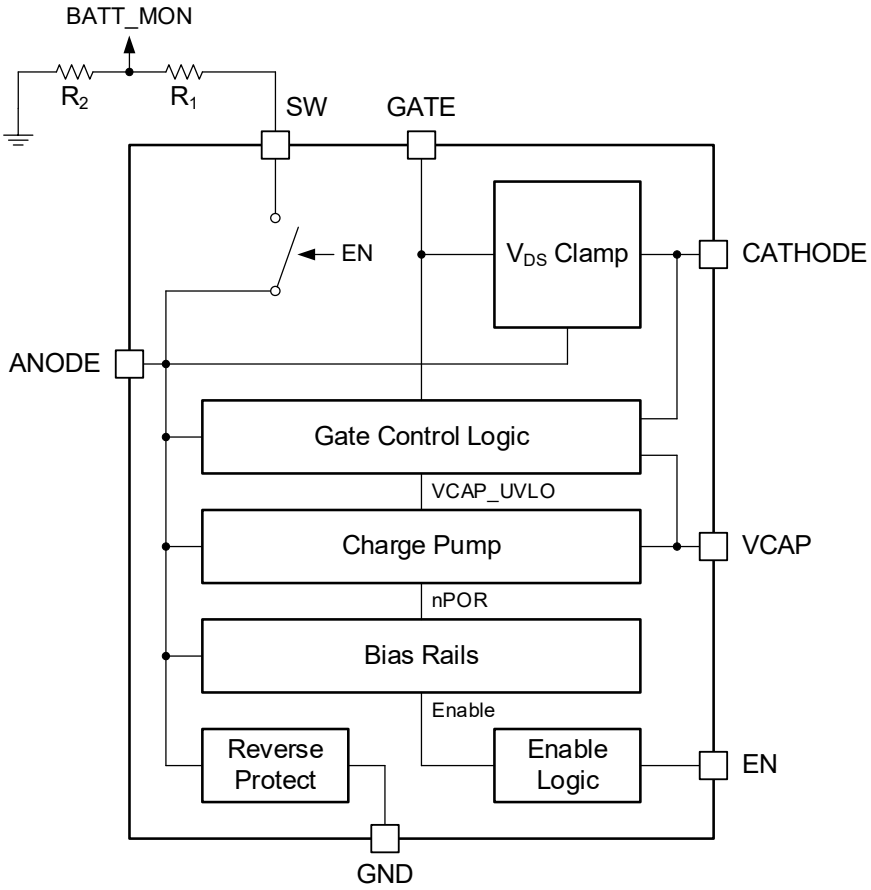


Figure 3. Block Diagram

DETAILED DESCRIPTION

The SGM25730Q ideal diode controller integrates all the essential functions for building a fast, efficient reverse polarity protection circuit while requiring minimal external components. At the same time, it minimizes the amount of external components. This user-friendly ideal diode controller is combined with an NMOS situated externally. The user-friendly ideal diode controller, combined with an external NMOS, replaces PMOSFETs or Schottky diodes for reverse polarity protection. Its internal charge pump drives the MOSFET with a max 12V gate voltage. The device constantly measures the voltage across the MOSFET via the ANODE and CATHODE pins, dynamically adjusting the GATE-to-ANODE voltage to maintain a forward voltage drop of 20mV. This closed-loop control mechanism allows for smooth MOSFET turn-off during reverse current conditions and guarantees zero steady-state reverse current. When the voltage difference between the ANODE and CATHODE pins lower than -11mV, it triggers the detection of a rapid reverse current event. Subsequently, an internal connection is made between the GATE pin and the ANODE pin, effectively deactivating the external NMOS. And the body diode takes over to block all reverse current flows. There is also an enable pin called EN. By using this pin, the SGM25730Q can enter shutdown mode, which disables the NMOS and reduces the quiescent current to the minimum. When SGM25730Q is enabled, an internal SW-to-ANODE switch allows input voltage monitoring through an external resistor divider on SW pin. The integrated V_{DS} clamp provides reverse polarity protection without an external TVS diode. For implementation details, please refer to the Functional Modes and Application Information section.

Input Voltage

The ANODE pin supplies power to the internal circuitry of the SGM25730Q. Generally, it consumes 80μA when it is enabled and 1μA when disabled. When the voltage of the ANODE pin exceeds the POR rising threshold, the SGM25730Q will operate either in shutdown mode or conduction mode, depending on the voltage of the EN pin. The designed voltage range from the ANODE to GND is from 65V to -33V. This enables the SGM25730Q to endure negative voltage input.

Charge Pump

The external NMOS is driven by the voltage produced by the charge pump. An external charge-pump capacitor is positioned between the VCAP and ANODE pins. This capacitor supplies the energy required to activate the external MOSFET. For the charge pump to deliver current to the external capacitor, the EN pin voltage must exceed the defined input high threshold, V_{EN_IH}. Once enabled, the charge pump typically provides a charging current of 300μA. When the EN pin is set to a low level, the charge pump remains inoperative. In order to guarantee the external MOSFET can be driven to a voltage higher than its specified threshold, the voltage between VCAP pin and ANODE pin must exceed the under-voltage lockout threshold, which is typically 5.86V. This condition must be met before enabling the internal gate driver. Calculate the initial gate driver enable delay using Equation 1. Here, C_{VCAP} represents the charge-pump capacitance connected between the ANODE pin and VCAP pin, and $V_{VCAP_UVLO_R}$ = 5.86V (TYP).

$$t_{DRV_EN} = 123\mu s + C_{VCAP} \times \frac{V_{VCAP_UVLO_R}}{300\mu A} \quad (1)$$

To eliminate gate drive chatter, approximately 800mV of hysteresis is applied to the VCAP under-voltage lockout threshold. The charge pump continues operating until the VCAP-to-ANODE voltage rises to 10.7V (TYP). Once this voltage level is reached, the charge pump is switched off. This action results in a reduction of the current consumption on the ANODE pin. The charge pump remains in the disabled state until the voltage from VCAP to ANODE drops below 9.8V typically. Once this voltage condition is met, the charge pump is activated. As illustrated in Figure 4, the voltage between VCAP and ANODE cycles through charging and discharging processes within the range of 9.8V to 10.7V. This on-off operation of the charge pump serves to reduce the quiescent operating current of the SGM25730Q. When disabled, the charge pump typically sinks a current of 4.4μA.

DETAILED DESCRIPTION (continued)

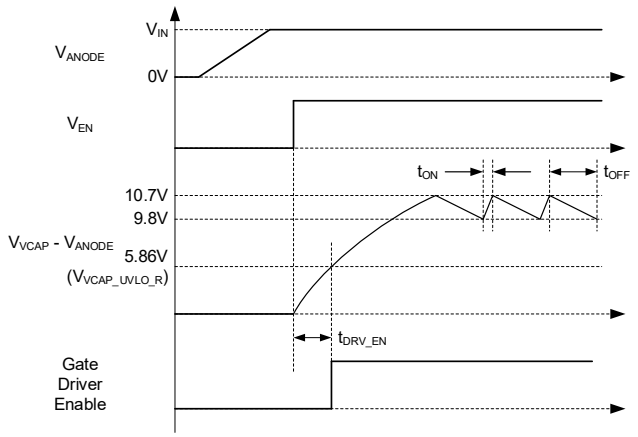


Figure 4. Charge Pump Operation

Gate Driver

The gate driver controls the external NMOS by adjusting the GATE to ANODE voltage to match the appropriate operating mode. Depending on the voltage difference between the ANODE pin and CATHODE pin, there are three distinct operational modes for the gate driver. These are forward regulation mode, full conduction mode, and reverse current protection. These three modes are described in more detail in the Conduction Mode section. Figure 5 illustrates the operating modes of the SGM25730Q as a function of the ANODE-to-CATHODE voltage. Transition from regulated conduction mode to full conduction mode occurs at 45mV, while the switch to reverse current protection mode happens when the ANODE-to-CATHODE voltage drops below -11mV. The device transitions from reverse current mode to V_{DS} clamp mode when the ANODE-to-CATHODE voltage reaches -39V.

In order to enable the gate driver, three specific requirements must all be satisfied:

- The voltage at the EN pin must exceed the enable input high threshold.
- The VCAP-to-ANODE voltage must exceed the under-voltage lockout threshold.
- The ANODE voltage must exceed the V_{ANODE} POR rising threshold.

If these conditions are not met, the GATE pin is internally pulled to the ANODE pin. This ensures the external MOSFET is turned off. Once the conditions are satisfied, the gate driver functions according to the appropriate mode based on the ANODE-to-CATHODE voltage.

Enable

The SGM25730Q features an enable pin, EN. An external signal uses this pin to enable or disable the gate driver. When $V_{EN} > V_{EN_IH}$, the gate driver and charge pump function as outlined in the sections above. When $V_{EN} < V_{EN_IL}$, the charge pump and gate driver are disabled, causing the SGM25730Q to enter a shutdown state. The EN pin has a specified voltage tolerance ranging from -33V to 65V. When enable function is unnecessary, it can be directly connected to the ANODE pin. When EN pin floats, a 1μA internal sink current pulls it to a low level, thus disabling the device.

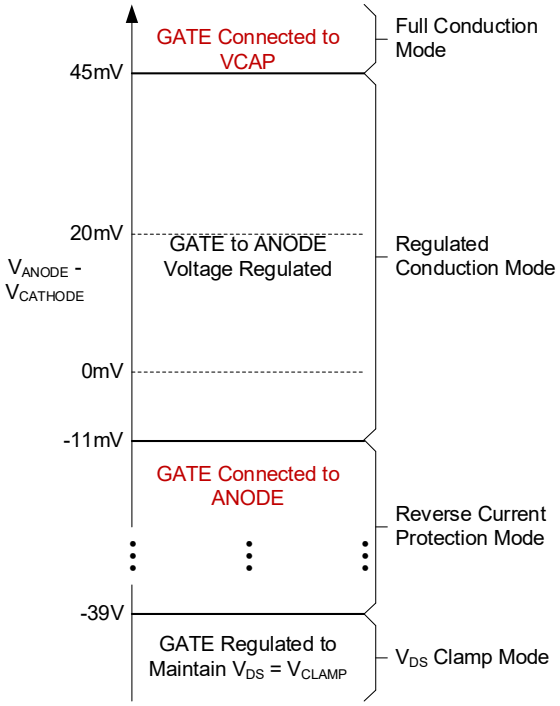


Figure 5. Gate Driver Mode Transitions

Battery Voltage Monitoring (SW)

The SGM25730Q is equipped with an SW pin that enables battery voltage monitoring in automotive systems. When enabled, an internal switch connects SW to ANODE to facilitate this measurement. This feature is implemented via an external resistor divider connected between the SW pin and GND, enabling accurate battery voltage monitoring. Pulling the EN pin low places the SGM25730Q in shutdown mode, at which point the internal switch between the SW and ANODE pins will disconnect. This mechanism prevents the resistor divider from drawing quiescent current when the system operates in low-power shutdown mode. The SW pin must remain floating if the function is not utilized.

DETAILED DESCRIPTION (continued)

Device Functional Modes

Shutdown Mode

When the voltage on the EN pin of the SGM25730Q dips below the input low threshold V_{EN_IL}, the device will enter the shutdown mode. In the shutdown mode, both the gate driver and the charge pump are deactivated, and it operates with a low quiescent current. During this time, the ANODE pin consumes a current as low as 1μA. While the SGM25730Q is in the shutdown mode, the forward current passing through the external MOSFET continues without disruption. Instead, it conducts through the body diode of the external MOSFET. When $V_{EN} < V_{EN_IL}$, the charge pump and gate driver are disabled, causing the SGM25730Q to enter the shutdown mode. During the shutdown mode, the SGM25730Q operates in a low-quiescent-current (low-I_Q) state. Specifically, the ANODE pin only consumes a current of 1μA. In shutdown mode, the SGM25730Q does not interrupt forward current flow through the external MOSFET. Instead, the current is conducted through the MOSFET's body diode.

Conduction Mode

When the gate driver is activated, the SGM25730Q enters the conduction mode. In this conduction mode, the device's operation can be divided into three distinct regions, which are determined by the voltage difference between the ANODE and the CATHODE. These three modes are detailed in the sections below.

Regulated Conduction Mode

To allow the SGM25730Q to function in regulated conduction mode, the gate driver should be activated as specified in the Gate Driver section. Additionally, the current passing from the source to the drain of the external MOSFET should be in the range that enables the ANODE pin to CATHODE pin voltage drop from -11mV to 45mV. In forward regulation mode, the ANODE-to-CATHODE voltage is controlled at 20mV by adjusting the GATE-to-ANODE voltage. This closed loop regulation mechanism allows the MOSFET to turn off smoothly under extremely light loads and guarantees that no DC reverse current occurs.

Full Conduction Mode

To allow the SGM25730Q to function in full conduction mode, the gate driver should be activated as specified in the Gate Driver section. Additionally, the current flowing from the source to the drain of the external MOSFET should be large enough that it causes the ANODE pin to CATHODE pin voltage drop greater than 45mV typical. Once these conditions are met, the GATE pin is internally connected to the VCAP pin. Consequently, the voltage between the GATE and the ANODE approximates that between the VCAP and the ANODE. Connecting the GATE pin to the VCAP pin leads to the minimization of the external MOSFET's R_{DSON}, thereby reducing power loss in the MOSFET during high forward current conditions.

V_{DS} Clamp Mode

The SGM25730Q integrates a V_{DS} clamp that operates the external MOSFET as an active clamp, dissipating energy from automotive EMC transients (e.g., ISO7637-2 pulse 1) in systems without output hold-up requirements. For tests that mandate a stable output, such as input short interruptions (LV124 E-10, ISO16750-2), the clamp threshold is calibrated to avoid engagement. This ensures the FET remains off during the reverse current blocking (RCB) state.

When an ISO7637-2 pulse 1 transient occurs at the input:

1. Once the ANODE-to-CATHODE voltage drop reaches the V_{AK_REV} threshold, the device pulls the GATE pin low to turn off the MOSFET.

2. When the drain-to-source voltage of the MOSFET rises to the minimum V_{CLAMP} level (34V), the GATE is driven high again. This operates the MOSFET in saturation as an active clamp, dissipating the transient energy. The typical circuit operation during this event is illustrated in Figure 6.

DETAILED DESCRIPTION (continued)

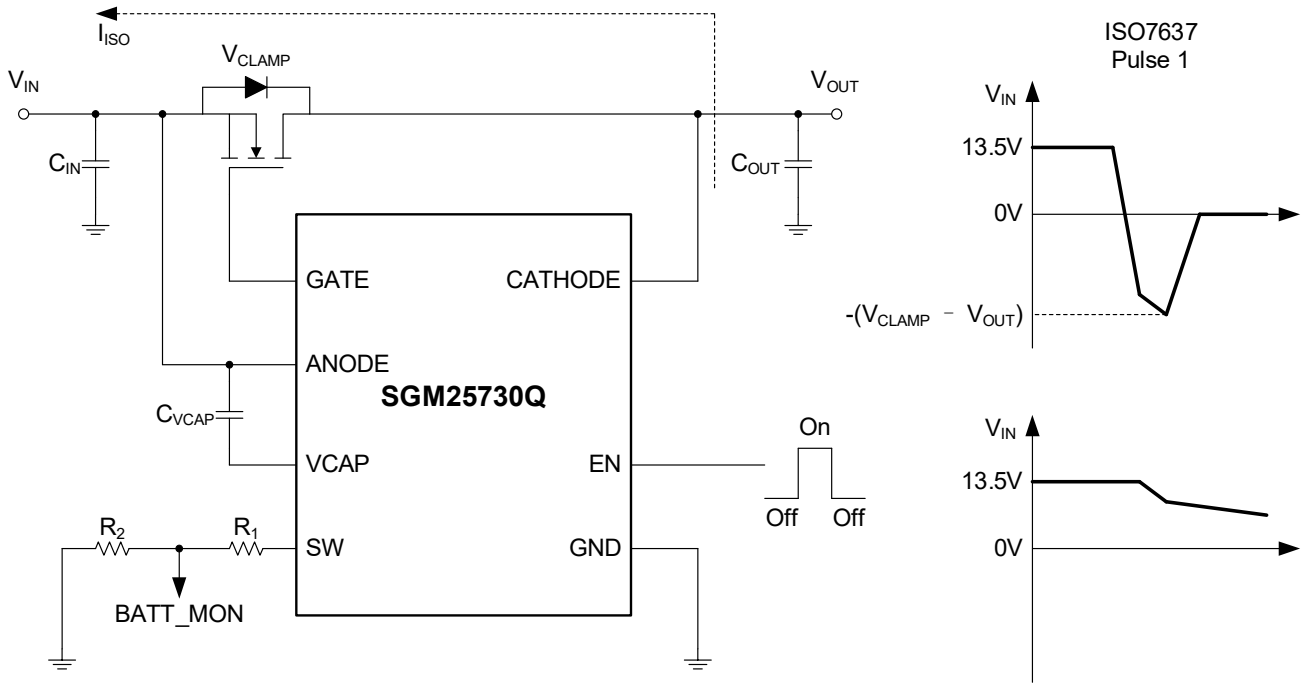


Figure 6. SGM25730Q Operation during V_{DS} Clamp Mode

Note that during the ISO7637 pulse 1 transient event, current flows in reverse from V_{OUT} back toward the input, which depletes the charge of the V_{OUT} capacitor. The CATHODE pin of the SGM25730Q is capable of withstanding negative voltage. However, if the loads connected to the output of SGM25730Q cannot tolerate negative voltage, the output hold-up capacitor must be carefully selected to ensure that V_{OUT} does not become negative during the ISO7637 pulse 1 test. For the remaining ISO7637 pulses (specifically pulse 2a, 2b, 3a, and 3b) which are short-duration transients that effectively suppressed by the filtering provided by the input and output capacitors. For more information on the system level EMC performance of the SGM25730Q, see the APPLICATION INFORMATION section.

Reverse Current Protection Mode

To allow the SGM25730Q to function in reverse current protection mode, the gate driver should be activated as specified in the Gate Driver section. Additionally, the current in the external MOSFET must flow from the drain to the source. When the ANODE-to-CATHODE voltage falls below approximately -11mV, reverse current protection mode is activated, and the GATE pin is internally connected to the ANODE pin. This connection disables the external MOSFET. The flow of reverse current from the drain to the source is interrupted by the body diode integrated within the MOSFET.

APPLICATION INFORMATION

Typical Application

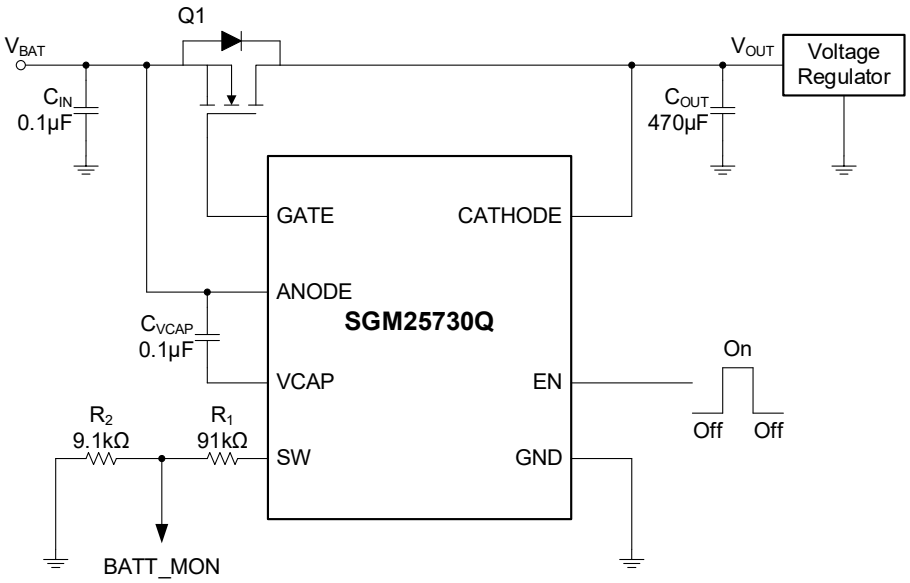


Figure 7. Typical Application Circuit

In a typical reverse polarity protection use case, the SGM25730Q is used in conjunction with an NMOS. Figure 7 presents the schematic for the 12V battery protection application. In this setup, the MOSFET is driven by connecting the SGM25730Q and a battery in series. The integrated V_{DS} clamp feature eliminates the need for an external input TVS diode. Meanwhile, the output capacitor C_{OUT} is highly recommended to help maintain a stable output by preventing abrupt voltage drops during line disturbances and ensuring the output remains positive during all system EMC transients.

Design Requirements

A design sample is shown, where the system design parameters are detailed in Table 1.

Table 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input Voltage Range	12V battery, 13.5V TYP with 3.2V cold crank and 35V load dump.
Output Voltage	3.2V during cold crank to 35V load dump.
Output Current Range	3A TYP, 6A MAX.
Output Capacitance	470μF TYP hold up capacitance
Automotive EMC Compliance	ISO7637-2 and ISO16750-2

Detailed Design Procedure

Design Considerations

- Input operating voltage range, accounting for cold crank and load dump scenarios
- Typical load current and maximum load current requirements
- EMC robustness against key automotive transients (e.g., ISO7637-2, LV124)

MOSFET Selection

Key MOSFET electrical parameters include the maximum continuous drain current I_D, maximum drain-to-source voltage V_{DS_MAX}, Safe Operating Area (SOA), maximum source current through the body diode, and the drain-to-source on-resistance R_{DSON}.

The I_D rating should be higher than the maximum continuous load current.

APPLICATION INFORMATION (continued)

To minimize the conduction losses of the MOSFET, it is preferable to choose a device with the lowest possible R_{DSON}. Nevertheless, choosing a MOSFET merely because of its low R_{DSON} might not consistently lead to favorable results. A higher R_{DSON} value offers enhanced voltage information to the reverse comparator of the SGM25730Q even at a relatively low reverse current. This means that reverse current detection becomes more effective when the R_{DSON} is increased. Under nominal load conditions, it is suggested to operate the MOSFET in the regulated conduction mode. When selecting the MOSFET, the R_{DSON} should be chosen in such a way that, at the maximum operating current, the forward voltage drop V_{DS} does not exceed 45mV.

The external MOSFET must have a maximum drain-to-source voltage, V_{DS_MAX}, rating sufficient for the application's highest differential voltage. In the SGM25730Q design, maximum voltage across the MOSFET is limited by its V_{CLAMP} (MAX, 43V). A 60V V_{DS} rating is recommended to ensure the robustness against all automotive transients and unforeseen faults.

During an ISO7637-2 pulse 1 event, the MOSFET experiences a maximum V_{DS} of V_{DS_CLAMP} (43V). The Equation 2 should be used to determine the peak current.

$$I_{ISO_PEAK} = \left(V_{ISO} + V_{OUT} - V_{DS_CLAMP_MAX}\right) / R_S \quad (2)$$

where

V_{ISO} is the negative peak of the ISO7637-2 pulse 1;

V_{OUT} is the initial level of the VBATT before ISO pulse is applied;

V_{DS_CLAMP} is maximum V_{CLAMP} threshold of SGM25730Q;

R_S is the ISO7637 pulse generator input impedance (10Ω).

For an ISO7637-2 Pulse 1 event (-100V amplitude, 13.5V output), MOSFET Q1 carries a peak reverse current of 7A, which tapers to zero as shown in *Response to ISO7367-2 Pulse 1*. The resulting average current is approximately 2.4A over the 1ms clamp duration. A suitable MOSFET must have a Safe Operating Area (SoA) that supports at least half of the peak current (3.5A in this case) at 43V V_{DS} for 1ms.

Figure 8 illustrates the typical Safe Operating Area (SoA), indicating the maximum drain current the MOSFET can support for 1ms. Since datasheet SoA curves are typically specified at ambient temperature, sufficient design margin must be included to ensure safe operation across the entire desired temperature range.

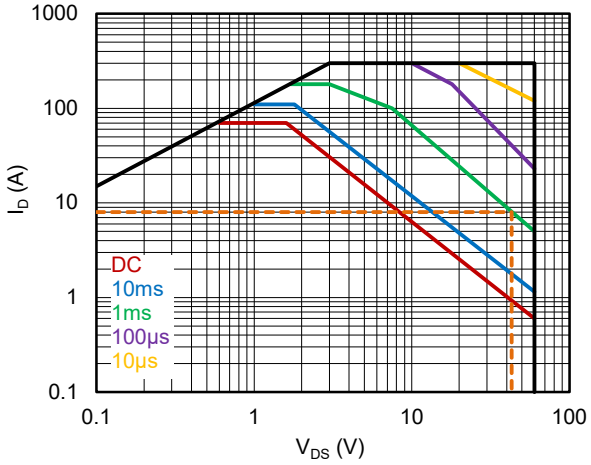


Figure 8. Typical MOSFET SoA Characteristics

The thermal performance of the external MOSFET, which dissipates the ISO7637-2 pulse 1 energy, requires careful assessment. Equation 3 can be used to calculate the average power dissipation for this evaluation.

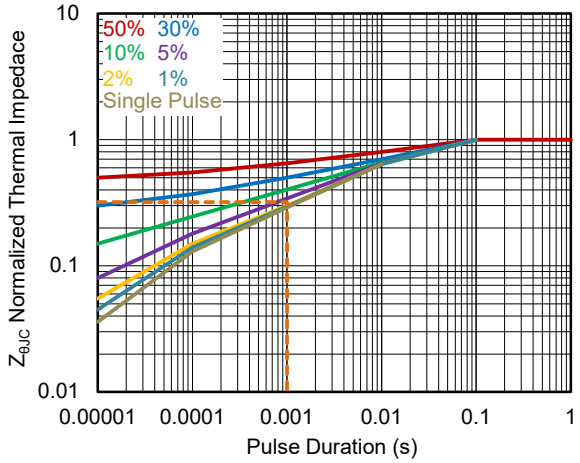
$$P_{D_AVG} = VDS_{CLAMP_MAX} \times I_{ISO_AVG} \quad (3)$$

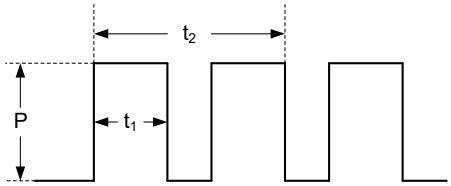
For the given design example, the average power dissipation is calculated to be approximately.

$$P_{D_AVG} = 43V \times 2.4A = 103.2W \quad (4)$$

The ISO7637-2 pulse 1 event has a 2ms duration and a 1% duty cycle (200ms period). To calculate the associated MOSFET temperature rise, refer to the transient thermal impedance curve in the MOSFET datasheet. Figure 9 provides an example of this estimation.

APPLICATION INFORMATION (continued)





$$\text{Duty Cycle} = \frac{t_1}{t_2}$$

$$R_{\theta JC}(MAX) = 0.6°C/W$$

$$\Delta T_J = P \times Z_{\theta JC} \times R_{\theta JC}$$

Figure 9. Typical MOSFET Transient Thermal Impedance

Since the SGM25730Q's maximum gate drive, V_{GS}, is 12.1V, the selected MOSFET must support a minimum V_{GS} rating of 15V.

Based on a comprehensive review, recommended 60V MOSFETs include the BUK7Y4R8-60E, SQJ460AEP, and STL130N6F7.

Charge Pump C_{VCAP}, Input and Output Capacitance

The minimum required capacitance values for the charge pump are as follows:

- C_{VCAP}: A minimum of 0.1μF is required, with a recommended value of C_{VCAP} (μF) ≥ 10 × C_{ISS_MOSFET} (μF).
- C_{IN}: A minimum of 100nF for input capacitance.

Output Capacitance (C_{OUT})

While the SGM25730Q's CATHODE pin can handle negative voltage, the connected loads are not negative-voltage tolerant. To prevent negative output voltage during ISO7637-2 pulse 1 for the loads, a sufficient output capacitor is required. The necessary value can be calculated using Equation 5.

$$C_{OUT} = \left(I_{LOAD} + I_{ISO_AVG}\right) \times 1ms / \Delta V_{OUT} \quad (5)$$

where

ΔV_{OUT} is difference between output voltage at the start and the end of ISO7637-2 pulse 1.

What to Do and What Not to Do

- The input decoupling capacitor (C_{IN}) should be placed as close as possible to the ANODE pin.
- External MOSFET is used to dissipate transient energy in ISO7637-2 pulse 1 event. For the MOSFET with exposed thermal pad, make sure exposed thermal pad is in firm contact with PCB copper plane for efficient thermal transfer. Follow PCB layout and soldering guidelines mentioned in the MOSFET data sheet.

ORing Application Configuration

A fundamental redundant power architecture consists of two or more voltage or power supply sources that power a single load. In its most elementary configuration, the ORing approach for redundant power supplies is constituted by Schottky ORing diodes. These diodes serve to defend the system from situations where the input power supply malfunctions. While diode ORing solution offers an efficient and cost-effective solution with minimal components, the forward voltage drop across the diodes leads to permanent efficiency losses. This is because each diode in an ORing setup primarily operates in forward conduction mode, resulting in continuous power dissipation. These power dissipations enhance the specifications for heat management and expand the required footprint on the printed circuit board.

APPLICATION INFORMATION (continued)

As depicted in Figure 10, the SGM25730Q ICs, along with external NMOSs, can be utilized within an ORing Solution. During normal operation, the external NMOS turns on, minimizing the forward diode drop. The SGM25730Q is capable of quickly detecting reverse current. Upon detecting reverse current, it rapidly pulls down the gate of the MOSFET. This mechanism allows the body diode of the MOSFET to prevent the reverse current from passing through. To ensure an efficient ORing solution, rapid response is critical to minimize both the magnitude and duration of reverse current. In the ORing configuration, the SGM25730Q constantly monitors the voltage disparity between its Anode and Cathode pins. The Anode pin represents the voltage at the power sources (V_{IN1}, V_{IN2}), while the Cathode pin represents the voltage at the shared load point. The SGM25730Q uses its Anode and Cathode pins to sense the source to drain voltage V_{DS} of each MOSFET. When the voltage difference V_{IN} - V_{OUT} drops below -11mV, a high speed comparator quickly disables the Gate Drive by pulling it down within 0.4μs (TYP). Conversely, when the forward voltage differential V_{IN} - V_{OUT} exceeds 45mV, the Gate is activated with an 8mA gate charge current.

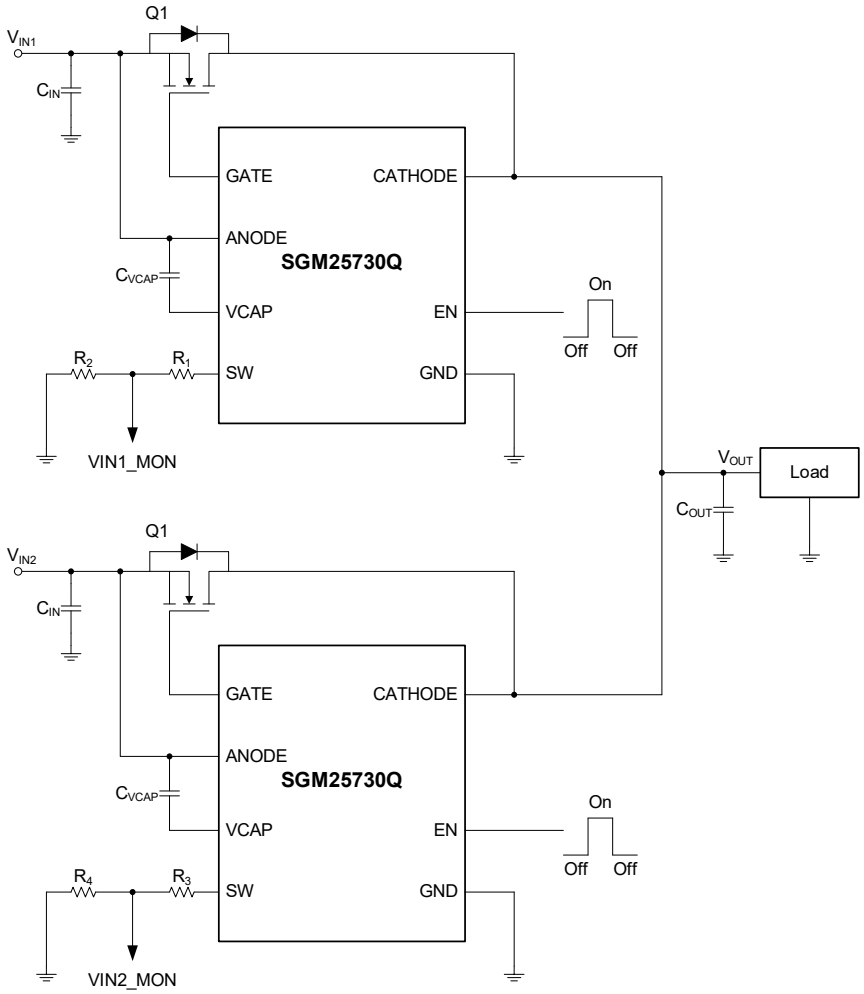


Figure 10. Typical ORing Application

APPLICATION INFORMATION (continued)

Power Supply Recommendations

The SGM25730Q Ideal Diode Controller is designed to operate within a supply voltage range of 3.2V ≤ V_{ANODE} ≤ 65V. When the input supply is situated several inches or more away from the device, it's best to employ an input ceramic bypass capacitor with a capacitance greater than 100nF. To avoid damage to the SGM25730Q and its surrounding components in the event of a direct output short circuit, a power supply offering overload and short circuit protection is essential.

Layout Guidelines

- Connect the ANODE, GATE, and CATHODE pins of SGM25730Q near the corresponding SOURCE, GATE, and DRAIN pins of the MOSFET.
- Ensure the source and drain traces of the MOSFET are wide enough to handle the high current flow and reduce resistive losses.
- Keep the charge pump capacitor between VCAP and ANODE pins away from the MOSFET to minimize thermal impact on its capacitance.
- Use a short and robust trace to connect the SGM25730Q's GATE pin to the MOSFET gate, avoiding thin or lengthy traces.
- Place the GATE pin as close as possible to the MOSFET to reduce turn-off delays resulting from trace resistance.
- Acceptable results can be obtained with different layout designs, but the layout in Figure 11 is a recommended approach for achieving good performance.

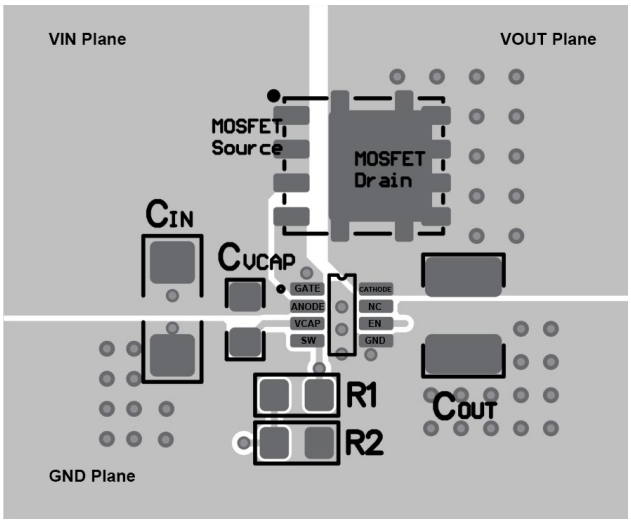


Figure 11. Layout Example

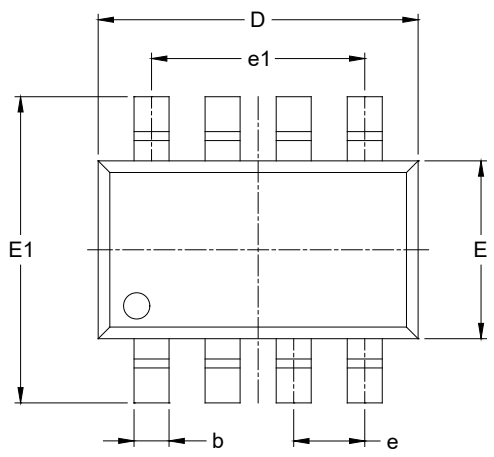
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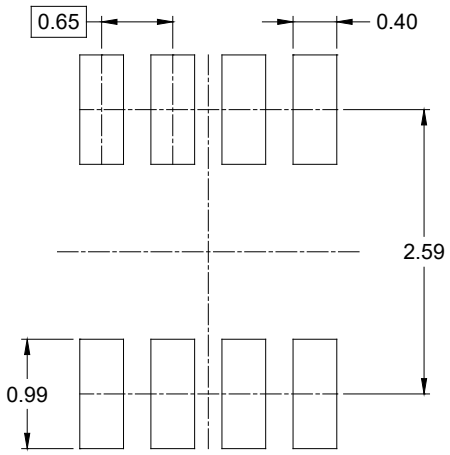
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original to REV.A (DECEMBER 2025)	Page
Changed from product preview to production data	All

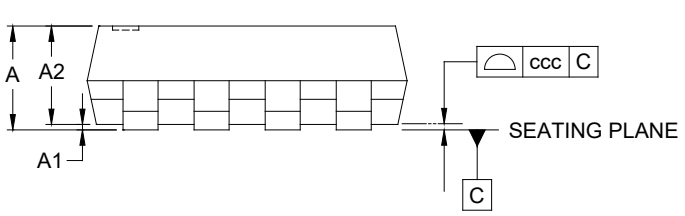
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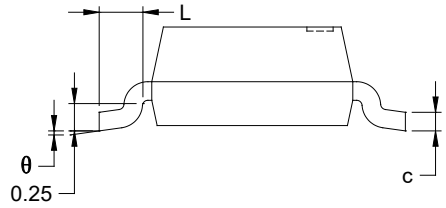
TSOT-23-8





RECOMMENDED LAND PATTERN (Unit: mm)



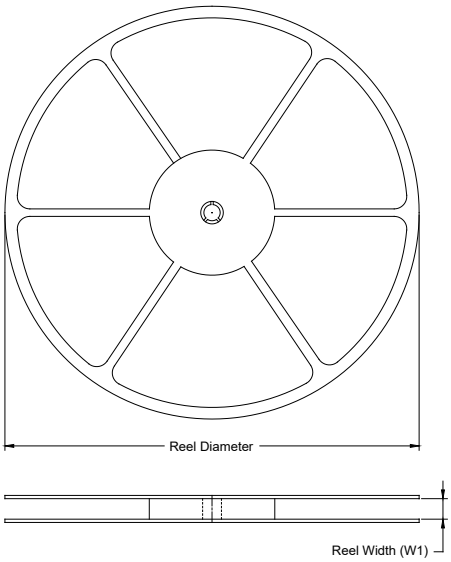


Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	1.100
A1	0.000	-	0.100
A2	0.700		1.000
b	0.220	-	0.380
c	0.080		0.200
D	2.750	-	3.050
E	1.450	-	1.750
E1	2.550	-	3.050
e	0.650 BSC		
e1	1.950 BSC		
L	0.300	-	0.600
θ	0°	-	8°
ccc	0.100		

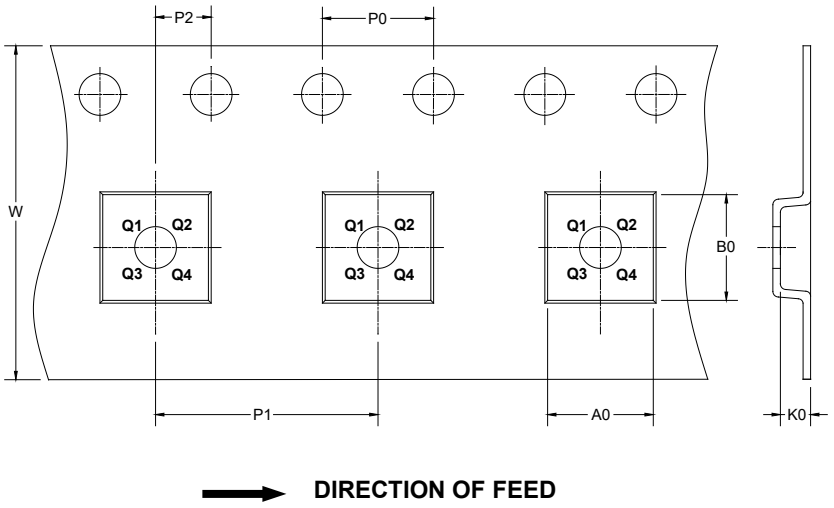
NOTES:
1. This drawing is subject to change without notice.
2. The dimensions do not include mold flashes, protrusions or gate burrs.
3. Reference JEDEC MO-193.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



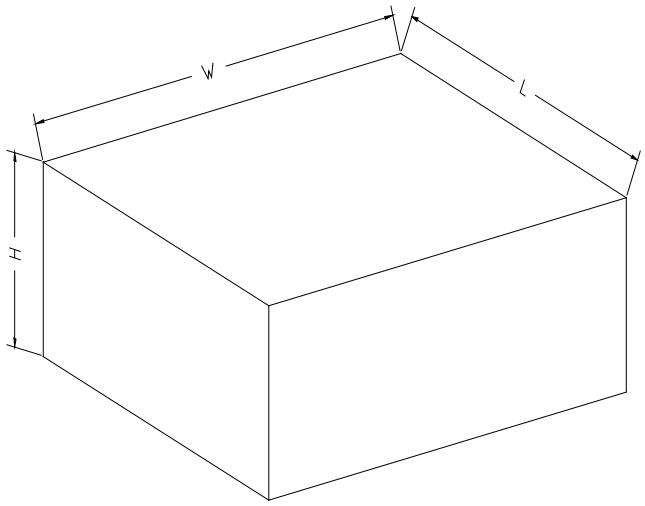
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TSOT-23-8	7"	9.5	3.20	3.10	1.10	4.0	4.0	2.0	8.0	Q3

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18

DD0002