Automotive CIS/CCM PMIC for Ultra Compact Camera and High Image Quality System

1 General Description

The RTQ2072A-QT/RTQ2072B-QT is a highly integrated PMIC designed for automotive camera applications. It includes three buck converters and one high PSRR low-dropout (LDO) regulator. The high-voltage buck converter operates with an input voltage range of up to 18.5V, suitable for Power Over Coax (POC) connections. Two low-voltage buck converters provide a constant output voltage. All buck converters operate in a forced fixed-frequency PWM mode.

The LDO output voltage can be easily set via an external resistor. The RTQ2072A-QT/RTQ2072B-QT supports 10 power sequences, configurable through a resistor. The ICQ is available in a WETD-VQFN-16L 3x3 package with dimple lead type wettable flanks.

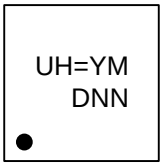
The recommended junction temperature range is –40°C to 150°C and the recommended ambient temperature range is –40°C to 125°C.

2 Applications

- Automotive Camera Modules
  - Surround View Cameras
  - Front View Cameras
  - Rear View Cameras
  - Dash Cam DVR
  - Driver Monitoring Systems
  - Cabin Monitors
  - E-mirrors

3 Marking Information

RTQ2072BAGQVT-QT-11

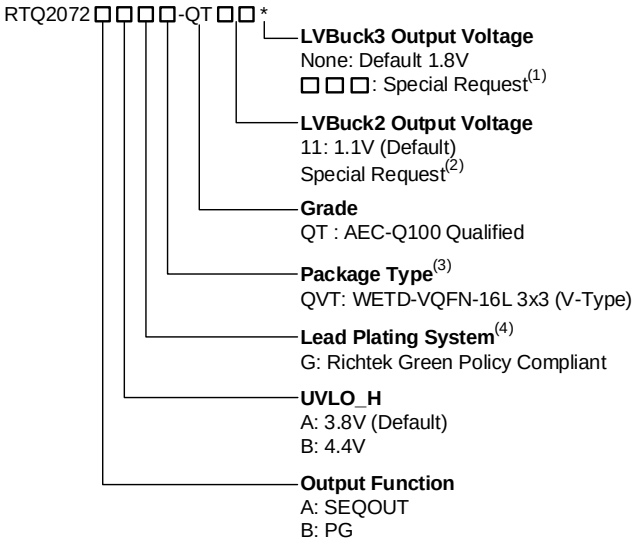


UH= : Product Code
YMDNN : Date Code

4 Features

- **AEC-Q100 Grade 1 Qualified**
- **FMEA Compliant Pin Placement and Protection Mechanisms**
- **Three Buck Converters (HVBuck1, LVBuck2, and LVBuck3)**
  - **Peak Current Mode PWM Operation**
  - **Fixed Switching Frequency at 2.1MHz**
  - **EMI Reduction Features including Spread Spectrum and Phase Shift Operation**
  - **HVBuck1 Supports Input Voltage from 4V to 18.5V, Adjustable Output Voltage, and up to 2A Output Current**
  - **LVBuck2 Supports Input Voltage from 2.7V to 5V, Fixed Output Voltage, and 1.5A Output Current**
  - **LVBuck3 Supports Input Voltage from 2.7V to 5V, Fixed Output Voltage, and 750mA Output Current**
  - **Pins Related to LVBuck2/LVBuck3 Can Float if the Channel is Unused**
- **Low Dropout Regulator (LDO)**
  - **Input Voltage from 2.7V to 5V and 300mA Output Current**
  - **10 Adjustable Output Voltage Settings via the RSET Pin**
  - **High PSRR: 60dB at 100kHz, 40dB at 1MHz**
- **Output Function**
  - **Sequence Control for External Power IC via SEQOUT (RTQ2072A-QT)**
  - **Power Status Indication via PG (RTQ2072B-QT)**
- **10 Flexible Power Sequence Settings via the SEQ Pin**
- **Small Form Factor WETD-VQFN-16L 3x3 Wettable Flanks Package**

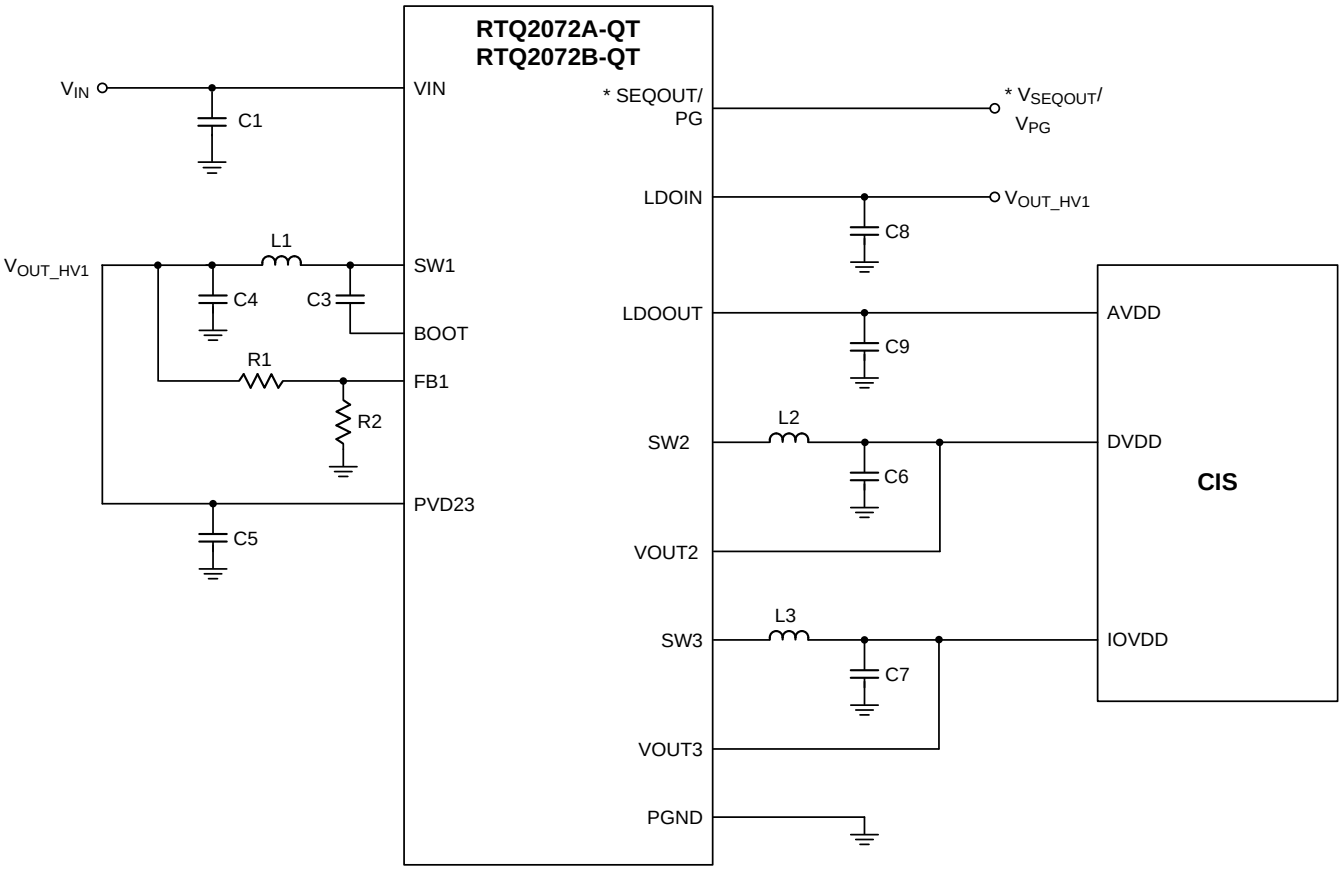
5 Ordering Information



Note 1.

- Marked with (1) indicated: Special Request: For example, 095 means 0.95V.
- Marked with (2) indicated: Special Request: Available voltage between 0.6V to 2.1V with 100mV step under specific business agreement.
- Marked with (3) indicated: Compatible with the current requirements of IPC/JEDEC J-STD-020.
- Marked with (4) indicated: Richtek products are Richtek Green Policy compliant.

6 Simplified Application Circuit



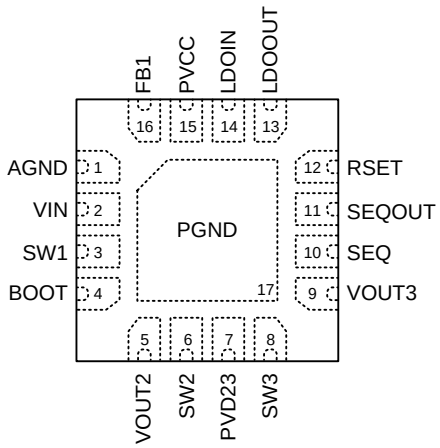
Note 2. The SEQOUT pinout is for the RTQ2072A-QT; the PG pinout is for the RTQ2072B-QT.

Table of Contents

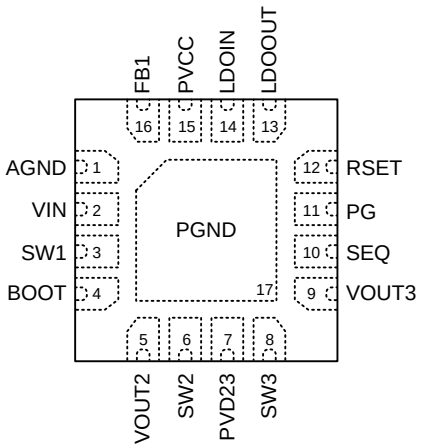
1 General Description 1
2 Applications 1
3 Marking Information 1
4 Features 1
5 Ordering Information 2
6 Simplified Application Circuit 2
7 Pin Configuration 4
8 Functional Pin Description 4
9 Functional Block Diagram 6
9.1 RTQ2072A-QT 6
9.2 RTQ2072B-QT 6
10 Absolute Maximum Ratings 7
11 Recommended Operating Conditions 7
12 Electrical Characteristics 8
12.1 System Characteristics 11
13 Typical Application Circuit 14
13.1 RTQ2072A-QT 14
13.2 RTQ2072B-QT 14
14 Typical Operating Characteristics 16
15 Operation 18
15.1 System Undervoltage Protection and Overvoltage Protection 18
15.2 Over-Temperature Protection 18
15.3 Pre-Regulator 18
15.4 Peak Current Mode Control 18
15.5 Spread-Spectrum Operation 18
15.6 Phase-Shifted Operation 19
15.7 Allowable Channel Floating 19
15.8 Power-Good Indication 19
15.9 External Control Output 19
16 Application Information 20
16.1 Power Sequence Control 20
16.2 Output Voltage Setting 22
16.3 Channel Protection Features 23
16.4 Input and Output Capacitor Selection 25
16.5 Thermal Considerations 25
16.6 Layout Considerations 26
17 Outline Dimension 28
18 Footprint Information 29
19 Packing Information 30
19.1 Tape and Reel Data 30
19.2 Tape and Reel Packing 31
19.3 Packing Material Anti-ESD Property 32
20 Datasheet Revision History 33

7 Pin Configuration

(TOP VIEW)



WETD-VQFN-16L 3x3 (RTQ2072A-QT)



WETD-VQFN-16L 3x3 (RTQ2072B-QT)

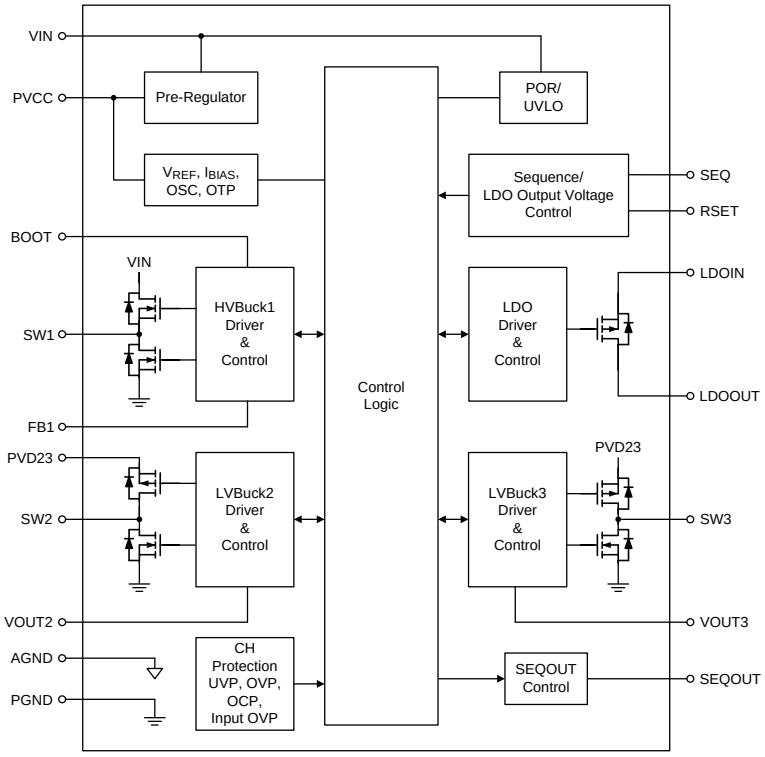
8 Functional Pin Description

Pin No.	Pin Name	Pin Function
1	AGND	Analog ground.
2	VIN	Supply voltage input of HVBuck1. Connect a 4.7μF or larger decoupling ceramic capacitor between this pin and ground.
3	SW1	HVBuck1 switch node.
4	BOOT	Bootstrap capacitor connection pin for HVBuck1. Connect a 0.1μF ceramic capacitor between this pin and SW1.
5	VOUT2	Output voltage feedback input of LVBuck2. Directly connect the output capacitor node to this pin for better regulation.
6	SW2	LVBuck2 switch node.
7	PVD23	Supply voltage input of LVBuck2 and LVBuck3. Connect a 4.7μF or larger decoupling ceramic capacitor between this pin and ground.
8	SW3	LVBuck3 switch node.
9	VOUT3	Output voltage feedback input of LVBuck3. Directly connect the output capacitor node to this pin for better regulation.
10	SEQ	Power sequence selection.
11	SEQOUT	Sequence control output with open drain structure for external power IC. (RTQ2072A-QT)
	PG	Power status indication pin with open-drain structure for HVBuck1, LVBuck2, LVBuck3 and LDO. PG at high state indicates all outputs work well. (RTQ2072B-QT)
12	RSET	LDO output voltage selection.
13	LDOOUT	LDO output. Connect a 2.2μF ceramic decoupling capacitor between this pin and ground.

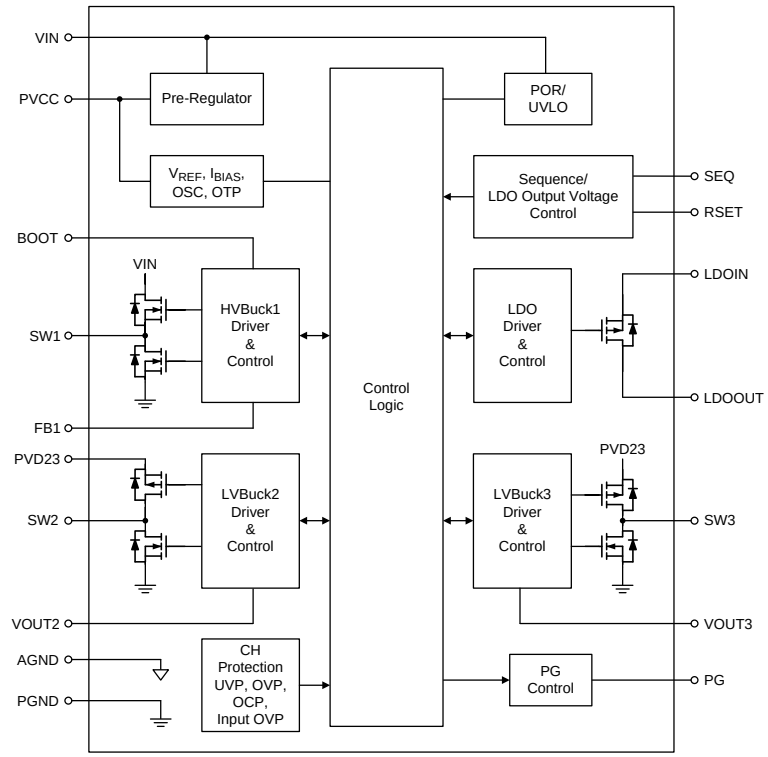
Pin No.	Pin Name	Pin Function
14	LDOIN	Supply voltage input of LDO. Connect a 2.2μF or larger decoupling ceramic capacitor between this pin and ground.
15	PVCC	Internal analog power output. Connect a 1μF ceramic decoupling capacitor between this pin and ground. Note additional external loading on this pin is forbidden.
16	FB1	Output voltage feedback input of HVBuck1.
17 (Exposed Pad)	PGND	IC thermal pad and power ground. It must connect to main ground plane for proper operation.

9 Functional Block Diagram

9.1 RTQ2072A-QT



9.2 RTQ2072B-QT



10 Absolute Maximum Ratings

(Note 3)

- VIN ---------- –0.3V to 24V
- SW1 ---------- –0.3V to 24V
- BOOT ---------- –0.3V to 28V
- BOOT to SW1 ---------- –0.3V to 5V
- VOUT2, PVD23, VOUT3, SEQ, SEQOUT (RTQ2072A-QT),
  PG (RTQ2072B-QT), RSET, LDOOUT, LDOIN, PVCC, FB1 ---------- –0.3V to 6.5V
- SW2, SW3 ---------- –0.3V to 6.5V
- Power Dissipation, P_D @ T_A = 25°C
  WETD-VQFN-16L 3x3 ---------- 4.16W
- Package Thermal Resistance (Note 4)
  WETD-VQFN-16L 3x3, θ_{JA} ---------- 30°C/W
  WETD-VQFN-16L 3x3, θ_{JC} ---------- 4.4°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 5)
  HBM (Human Body Model) ---------- 2kV

Note 3. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 4. θ_{JA} is simulated under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is simulated at the bottom of the package.

Note 5. Devices are ESD sensitive. Handling precautions are recommended.

11 Recommended Operating Conditions

(Note 6)

- Supply Voltage, V_{IN} ---------- 4V to 18.5V
- Supply Voltage, V_{PVD23}, V_{LDOIN} ---------- 2.7V to 5V
- Ambient Temperature Range ---------- –40°C to 125°C
- Junction Temperature Range ---------- –40°C to 150°C

Note 6. The device is not guaranteed to function outside its operating conditions.

12 Electrical Characteristics

(T_A = T_J = –40°C to 125°C, V_{IN} = 6V, V_{OUT_HV1} = 3.6V, V_{OUT_LV2} = 1.1V, V_{OUT_LV3} = 1.8V, V_{OUT_LDO} = 3.3V, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System						
Undervoltage-Lockout Threshold	V_{UVLO_H}	V_{IN} rising	3.6	3.8	4	V
	V_{UVLO_L}	V_{IN} falling	3.15	3.3	3.45	V
Input Overvoltage Protection	V_{OVP_VIN}		18.6	20	21.5	V
CH1 HVBuck1						
Input Voltage Range	V_{IN}		4	--	18.5	V
Output Voltage Range	V_{OUT_HV1}	Buck mode operation. Switching frequency, minimum on-time and minimum off-time need to be considered.	2.7	--	5	V
Output Feedback Voltage Accuracy	V_{FB1_ACC}		0.788	0.8	0.812	V
Switching Frequency	f_{SW_HV1}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	$SS_{_HV1}$		--	6	--	%
Switching Minimum On Time	$t_{ON_MIN_HV1}$		--	--	55	ns
Switching Minimum Off Time	$t_{OFF_MIN_HV1}$		--	--	50	ns
High-Side MOSFET On Resistance	$R_{ON_HS_HV1}$	From VIN pin to SW1 pin	115	210	340	mΩ
Low-Side MOSFET On Resistance	$R_{ON_LS_HV1}$	From SW1 pin to PGND pin	40	110	200	mΩ
Inductor Peak Current Limit	$I_{CL_PK_HV1}$		2.4	3	3.6	A
Inductor Valley Current Limit	$I_{CL_VL_HV1}$		--	2.7	--	A
Negative Inductor Peak Current Limit	$I_{CL_NPK_HV1}$		1	2.5	4	A
Output Discharge Resistor	R_{DISCHG_HV1}		220	270	360	Ω
Output Undervoltage Falling Threshold	$UVP_{_F_HV1}$		40	50	60	%
Output Feedback Overvoltage Rising Threshold	$OVP_{_R_HV1}$		--	110	--	%
CH2 LVBuck2 (V_{IN_PVD23} = 3.6V)						
Input Voltage Range	V_{IN_PVD23}		2.7	--	5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OUT_LV2}		--	1.1	--	V
Output Voltage Accuracy	$V_{OUT_ACC_LV2}$		–1.5	--	1.5	%
Switching Frequency	f_{SW_LV2}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	$SS_{_LV2}$		--	6	--	%
Switching Minimum On Time	$t_{ON_MIN_LV2}$		--	--	44	ns
High-Side MOSFET On Resistance	$R_{ON_HS_LV2}$	From PVD23 pin to SW2 pin	110	150	215	mΩ
Low-Side MOSFET On Resistance	$R_{ON_LS_LV2}$	From SW2 pin to PGND pin	60	90	145	mΩ
Inductor Peak Current Limit	$I_{CL_PK_LV2}$		1.8	2.2	2.6	A
Inductor Valley Current Limit	$I_{CL_VL_LV2}$		--	1.8	--	A
Negative Inductor Peak Current Limit	$I_{CL_NPK_LV2}$		0.7	1.7	2.9	A
Output Discharge Resistor	R_{DISCHG_LV2}		6	9	14	Ω
Output Undervoltage Falling Threshold	$UVP_{_F_LV2}$		40	50	60	%
Output Overvoltage Rising Threshold	$OVP_{_R_LV2}$		--	120	--	%
Output Overvoltage Falling Threshold	$OVP_{_F_LV2}$		--	110	--	%
Input Overvoltage Rising Threshold	$OVP_{_IN_R_LV2}$		5.35	5.8	6.25	V
Input Overvoltage Hysteresis	$OVP_{_IN_HYS_LV2}$	V_{IN_PVD23} falling	--	580	--	mV
CH3 LVBuck3 (V_{IN_PVD23} = 3.6V)						
Input Voltage Range	V_{IN_PVD23}		2.7	--	5	V
Output Voltage	V_{OUT_LV3}		--	1.8	--	V
Output Voltage Accuracy	$V_{OUT_ACC_LV3}$		–1.5	--	1.5	%
Switching Frequency	f_{SW_LV3}		1.89	2.1	2.31	MHz
Spread-Spectrum Range	$SS_{_LV3}$		--	6	--	%
Switching Minimum On Time	$t_{ON_MIN_LV3}$		--	--	44	ns

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-Side MOSFET On Resistance	$R_{ON_HS_LV3}$	From PVD23 pin to SW3 pin	240	310	440	mΩ
Low-Side MOSFET On Resistance	$R_{ON_LS_LV3}$	From SW3 pin to PGND pin	170	230	360	mΩ
Inductor Peak Current Limit	$I_{CL_PK_LV3}$		0.96	1.2	1.44	A
Inductor Valley Current Limit	$I_{CL_VL_LV3}$		--	1.08	--	A
Negative Inductor Peak Current Limit	$I_{CL_NPK_LV3}$		0.7	1.7	2.9	A
Output Discharge Resistor	R_{DISCHG_LV3}		7	10	15	Ω
Output Undervoltage Falling Threshold	$UVP_{_F_LV3}$		40	50	60	%
Output Overvoltage Rising Threshold	$OVP_{_R_LV3}$		--	120	--	%
Output Overvoltage Falling Threshold	$OVP_{_F_LV3}$		--	110	--	%
Input Overvoltage Rising Threshold	$OVP_{_IN_R_LV3}$		5.35	5.8	6.25	V
Input Overvoltage Hysteresis	$OVP_{_IN_HYS_LV3}$	V_{IN_PVD23} falling	--	580	--	mV
CH4 LDO (V_{IN_LDO} = 3.6V)						
Input Voltage Range	V_{IN_LDO}		2.7	--	5	V
Output Voltage Range	V_{OUT_LDO}	V_{OUT_LDO} setting via RSET	1.8	--	3.5	V
Output Voltage Accuracy	$V_{OUT_ACC_LDO}$	V_{IN_LDO} - V_{OUT_LDO} > 0.3V, I_{OUT_LDO} = 0mA to 300mA	−1.5	--	1.5	%
Maximum Output Current	$I_{OUT_MAX_LDO}$		300	--	--	mA
Dropout Voltage	$V_{DROP_300_LDO}$	I_{OUT_LDO} = 300mA (Note 7)	--	--	300	mV
	$V_{DROP_150_LDO}$	I_{OUT_LDO} = 150mA (Note 7)	--	--	150	
Output Current Limit	I_{CL_LDO}	(Note 8)	345	450	555	mA
Output Discharge Resistor	R_{DISCHG_LDO}		48	76	104	Ω
Output Undervoltage Falling Threshold	$UVP_{_F_LDO}$		30	40	50	%
Output Overvoltage Rising Threshold	$OVP_{_R_LDO}$		--	125	--	%

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Overvoltage Falling Threshold	OVP_{F_LDO}		--	110	--	%
Input Overvoltage Rising Threshold	$OVP_{IN_R_LDO}$		5.35	5.8	6.25	V
Input Overvoltage Hysteresis	$OVP_{IN_HYS_LDO}$	V_{IN_LDO} falling	--	500	--	mV
PVCC (Note 9)						
Internal Regulator Output Voltage	V_{OUT_PVCC}		4.33	4.58	4.83	V
Overcurrent Limit	I_{CL_PVCC}		150	--	300	mA
SEQOUT (RTQ2072A-QT)						
Output Low Voltage		Current into SEQOUT pin equal to 2mA	--	--	200	mV
Input Leakage Current	I_{LEAK_SEQOUT}	1.8V applied on SEQOUT pin	--	--	1	µA
Power-Good Indicator (RTQ2072B-QT)						
Pull Down Voltage	$V_{OUT_L_PG}$	Current into the PG pin is equal to 5mA	--	--	200	mV
Input Leakage Current	I_{LK_PG}	1.8V is applied to the PG pin	--	--	1	µA
Timing						
Soft-Start Time	t_{SS_HV1}	Time from V_{OUT_HV1} 0% rise to 90% of target value, no load	500	1000	1500	µs
	t_{SS_LV2}	Time from V_{OUT_LV2} 0% rise to 90% of target value, no load	500	1000	1500	
	t_{SS_LV3}	Time from V_{OUT_LV3} 0% rise to 90% of target value, no load	500	1000	1500	
	t_{SS_LDO}	Time from the previous turn on channel's output voltage reaching 90% of target value to V_{OUT_LDO} rise to 90% of target value. (Note 10)	200	700	1100	
PG Delay Time	t_{DLY_PG}	(RTQ2072B-QT)	9	10	11	ms

12.1 System Characteristics

The following specifications are guaranteed by design and are not performed in production testing. (T_A = T_J = –40°C to 125°C, V_{IN} = 6V, V_{OUT_HV1} = 3.6V, V_{OUT_LV2} = 1.1V, V_{OUT_LV3} = 1.8V, V_{OUT_LDO} = 3.3V, unless otherwise specified.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
System						
Over-Temperature Protection	T_{OTP}		--	160	--	°C
Over-Temperature Protection Hysteresis	T_{OTP_HYS}		--	20	--	°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CH1 HVBuck1						
Maximum Output Current	$I_{OUT_MAX_HV1}$		2	--	--	A
Load Regulation	$V_{LOAD_REG_HV1}$	I_{OUT_HV1} = 0A to 2A	--	--	0.1	%/A
Line Regulation	$V_{LINE_REG_HV1}$	V_{IN} = 5V to 18.5V, I_{OUT_HV1} = 2A	--	--	1	%
Load Transient	$V_{LOAD_TR_HV1}$	I_{OUT_HV1} = 10mA to 500mA to 10mA, 1μs	–150	--	150	mV
Line Transient	$V_{LINE_TR_HV1}$	V_{IN} = 5V to 18.5V to 5V, 100μs, I_{OUT_HV1} = 10mA/500mA	–50	--	50	mV
Output Ripple	V_{RIPPLE_HV1}	Peak to peak in one switching cycle	--	--	20	mVpp
CH2 LVBuck2 (V_{IN_PVD23} = 3.6V)						
Maximum Output Current	$I_{OUT_MAX_LV2}$		1.5	--	--	A
Load Regulation	$V_{LOAD_REG_LV2}$	I_{OUT_LV2} = 0A to 1.5A	--	--	0.1	%/A
Line Regulation	$V_{LINE_REG_LV2}$	V_{IN_PVD23} = 2.7V to 5V, I_{OUT_LV2} = 1.5A	--	--	1	%
Load Transient	$V_{LOAD_TR_LV2}$	I_{OUT_LV2} = 10mA to 500mA to 10mA, 1μs	–50	--	50	mV
Line Transient	$V_{LINE_TR_LV2}$	V_{IN_PVD23} = 3V to 5V to 3V, 50μs, I_{OUT_LV2} = 10mA/1A	–50	--	50	mV
Output Ripple	V_{RIPPLE_LV2}	Peak to peak in one switching cycle	--	--	10	mVpp
CH3 LVBuck3 (V_{IN_PVD23} = 3.6V)						
Maximum Output Current	$I_{OUT_MAX_LV3}$		750	--	--	mA
Load Regulation	$V_{LOAD_REG_LV3}$	I_{OUT_LV3} = 0A to 750mA	--	--	0.1	%/A
Line Regulation	$V_{LINE_REG_LV3}$	V_{IN_PVD23} = 2.7V to 5V, I_{OUT_LV3} = 750mA	--	--	1	%
Load Transient	$V_{LOAD_TR_LV3}$	I_{OUT_LV3} = 10mA to 300mA to 10mA, 1μs	–50	--	50	mV
Line Transient	$V_{LINE_TR_LV3}$	V_{IN_PVD23} = 3V to 5V to 3V, 50μs, I_{OUT_LV3} = 10mA/300mA	–50	--	50	mV
Output Ripple	V_{RIPPLE_LV3}	Peak to peak in one switching cycle	--	--	10	mVpp
CH4 LDO (V_{IN_LDO} = 3.6V)						
Power Supply Rejection Ratio	$PSRR_{LDO}$	I_{OUT_LDO} = 100mA, f = 100kHz	--	60	--	dB
		I_{OUT_LDO} = 100mA, f = 1MHz	--	40	--	
Output Noise Voltage	eN_{LDO}	I_{OUT_LDO} = 100mA, f = 100Hz to 100kHz	--	60	--	μV
Load Transient	$V_{LOAD_TR_LDO}$	I_{OUT_LDO} = 10mA to 200mA to 10mA, 1μs	–25	--	25	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Transient	$V_{LINE_TR_LDO}$	All V_{OUT_LDO}, V_{IN_LDO} step 600mV, LDO not in dropout condition, 10μs, I_{OUT_LDO} = 1mA/300mA	−25	--	25	mV
Component Requirement (Note 6)						
Effective Input Capacitance	C_{IN_HV1}		1.5	4.7	10	μF
	C_{IN_PVD23}		1.5	4.7	10	
	C_{IN_LDO}		0.7	2.2	4	
Effective Output Capacitance	C_{OUT_HV1}		3.3	10	14	μF
	C_{OUT_LV2}		4.5	10	14	
	C_{OUT_LV3}		4.5	10	14	
	C_{OUT_LDO}		0.7	2.2	4	
Output Inductance	L_{HV1}		1	1.5	2	μH
	L_{LV2}		0.68	1	1.2	
	L_{LV3}		0.68	1	1.2	
Effective Boot Capacitance	C_{BOOT}		0.07	0.1	0.13	μF
Effective PVCC Capacitance	C_{PVCC}		0.3	1	1.4	μF

Note 7. The Dropout voltage is the voltage difference between the input and the output at which the output voltage drops to 100 mV below its nominal value.

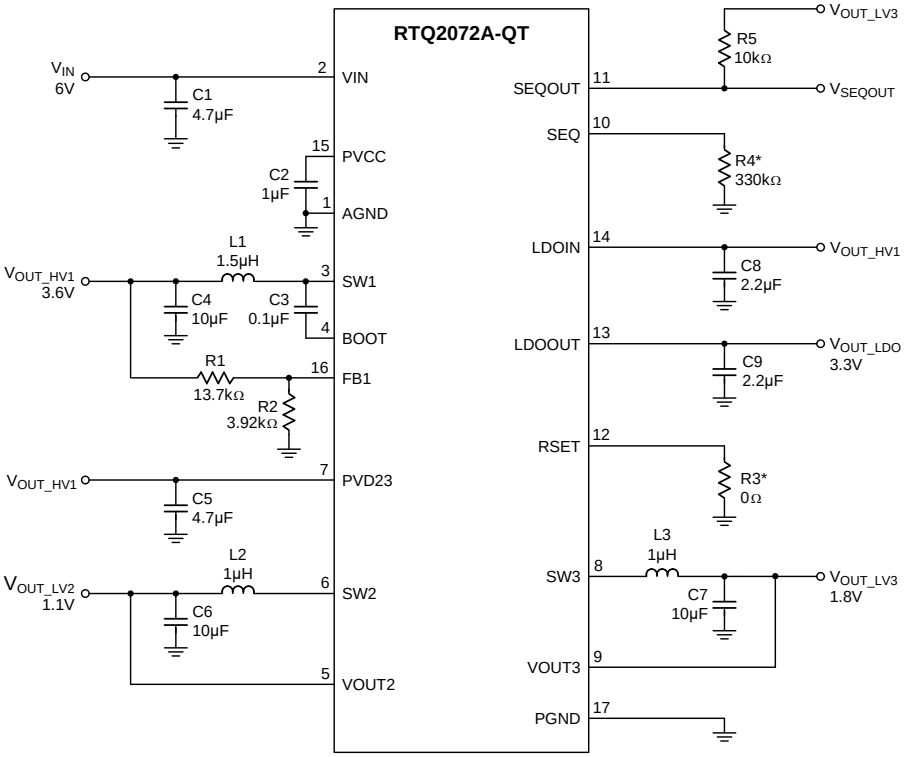
Note 8. It only supports LDO loading smaller than 150mA (typical) to power up successfully. The current limit changes back to 450mA after LDO rail enabled after 8ms.

Note 9. PVCC is the pre-regulator output voltage only for internal circuitry. External loading on the PVCC pin is forbidden.

Note 10. The t_{SS_LDO} depends on LDO total output capacitance. It can calculate the soft-start time without loading condition as formula: $t_{SS_LDO} = (C_{OUT_LDO} \times V_{OUT_LDO}) / 0.15$.

13 Typical Application Circuit

13.1 RTQ2072A-QT



13.2 RTQ2072B-QT

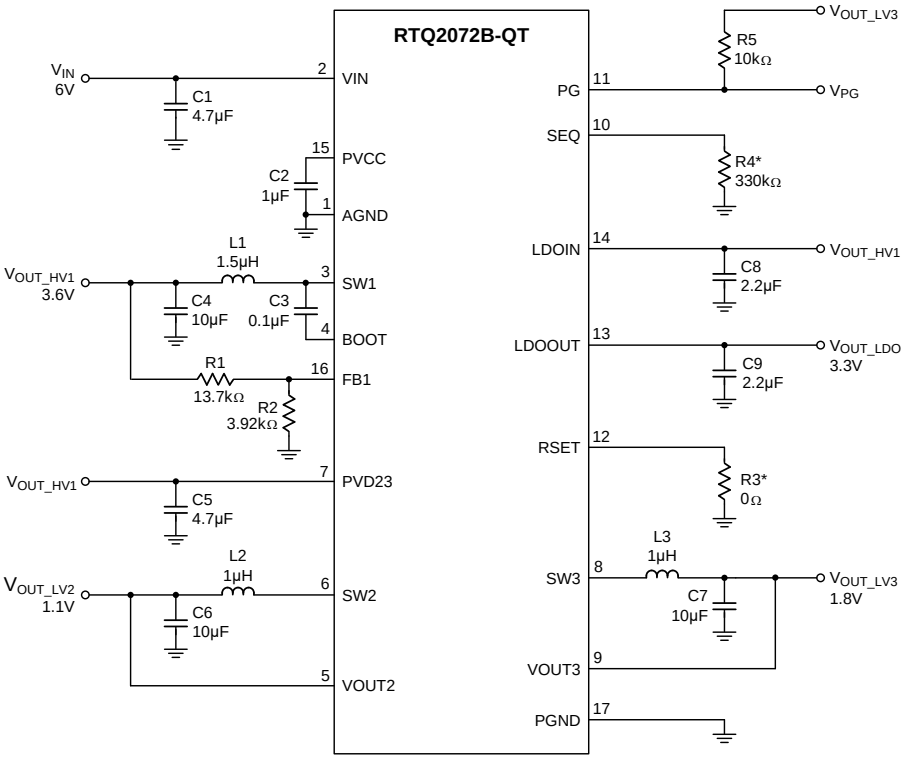


Table 1. Component List of Evaluation Board

Reference	Qty	Part Number	Description	Package	Manufacturer
C1	1	GCJ31CR71E475KA12	4.7μF/25V/X7R	1206	MURATA
C2	1	GRT155C81A105KE01	1μF/10V/X6S	0402	MURATA
C3	1	GRT155R71C104KE01	0.1μF/16V/X7R	0402	MURATA
C4, C6, C7	1	GRT188C81A106ME13	10μF/10V/X6S	0603	MURATA
C5	1	GRT188C81C475KE13	4.7μF/16V/X6S	0603	MURATA
C8, C9	1	GRT155C81A225KE13	2.2μF/10V/X6S	0402	MURATA
L1	1	TFM201610ALMA1R5MTAA	1.5μH/3.1A/85mΩ	0806	TDK
L2, L3	1	TFM201610ALMA1R0MTAA	1μH/3.7A/50mΩ	0806	TDK
R1	1	MR02X1372FAL	13.7kΩ/1%	0201	WALSIN
R2	1	MR02X3921FAL	3.92kΩ/1%	0201	WALSIN
R3 (Note 11)	1	MR02X000 PAL	0Ω/Jumper	0201	WALISN
R4 (Note 11)	1	MR02X3303FAL	330kΩ/1%	0201	WALSIN
R5	1	MR02X1002FAL	10kΩ/1%	0201	WALSIN

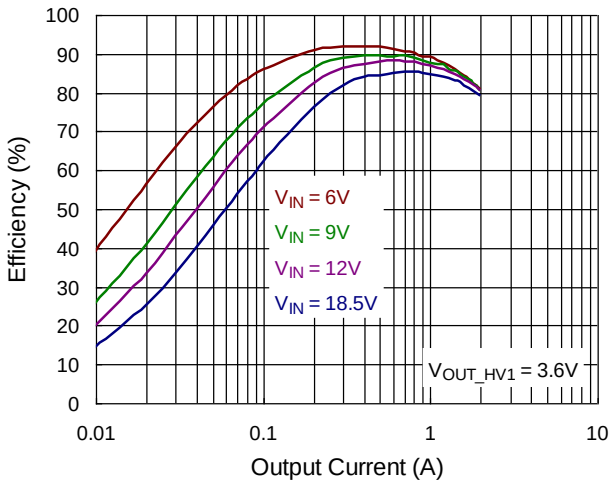
Note 11.

R3: The resistor is adjustable with different LDO output voltages.

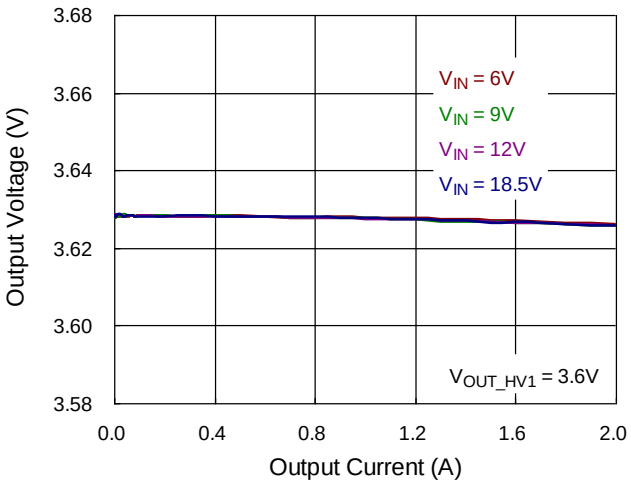
R4: The resistor is adjustable with different power-on sequences.

14 Typical Operating Characteristics

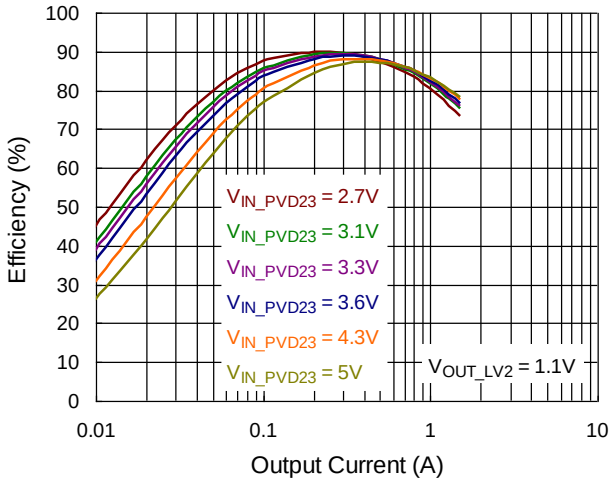
HVBuck1 Efficiency



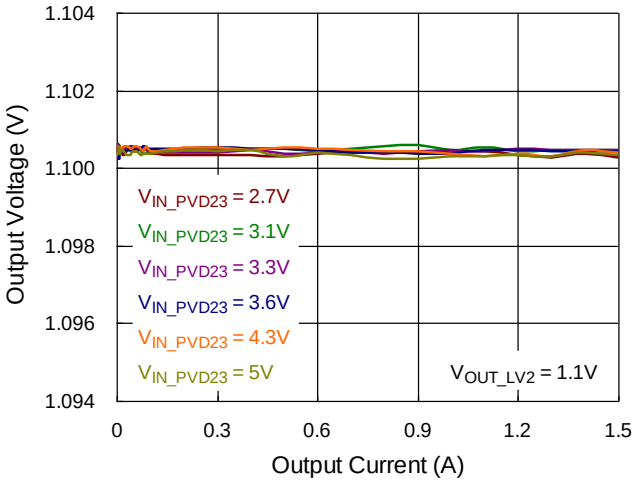
HVBuck1 Load Regulation



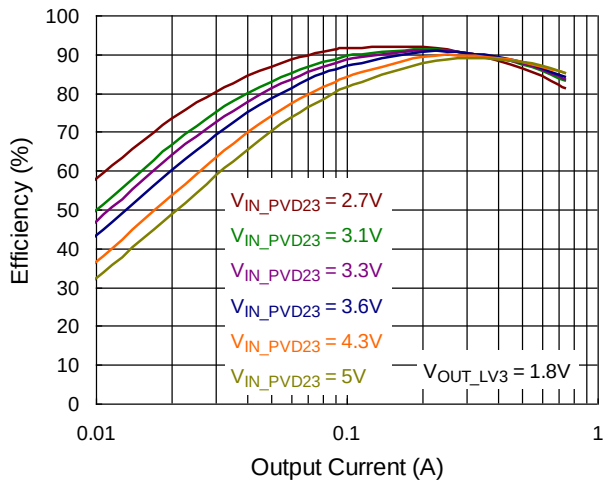
LVBuck2 Efficiency



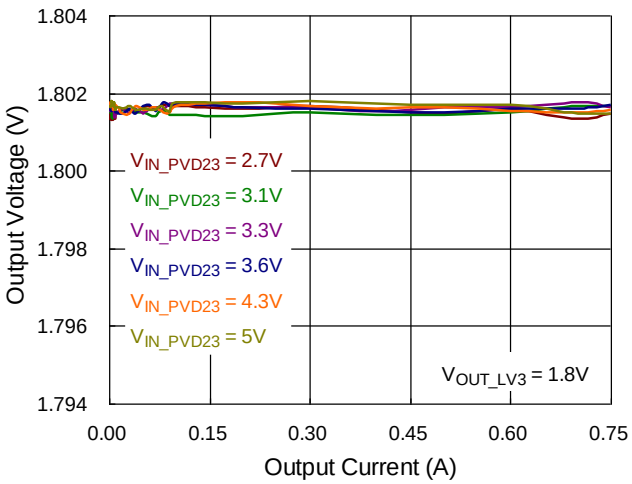
LVBuck2 Load Regulation



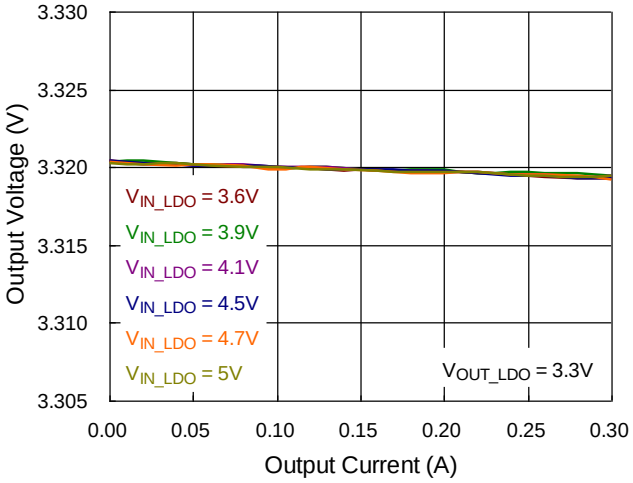
LVBuck3 Efficiency



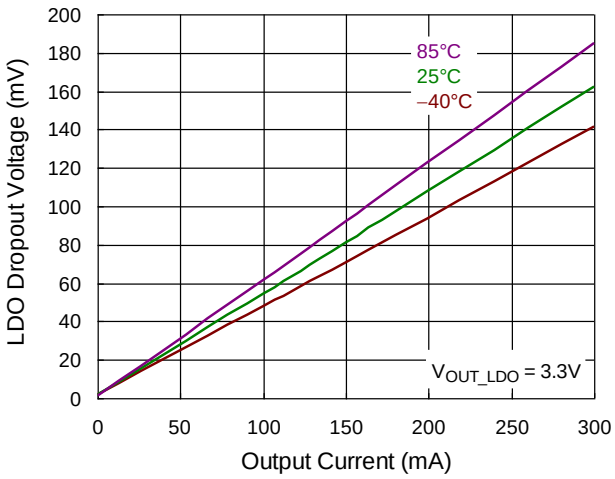
LVBuck3 Load Regulation



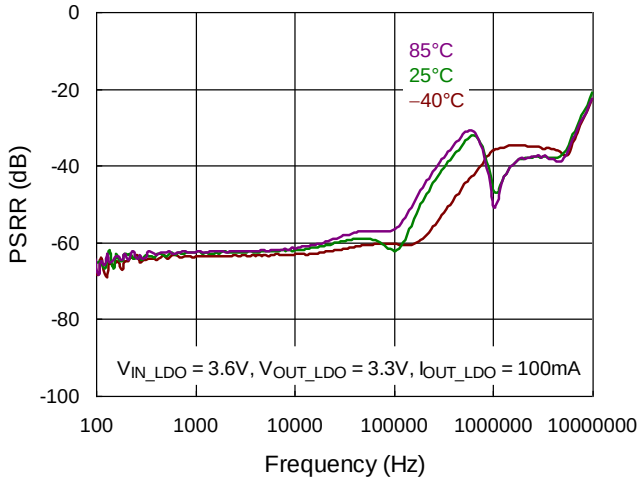
LDO Load Regulation



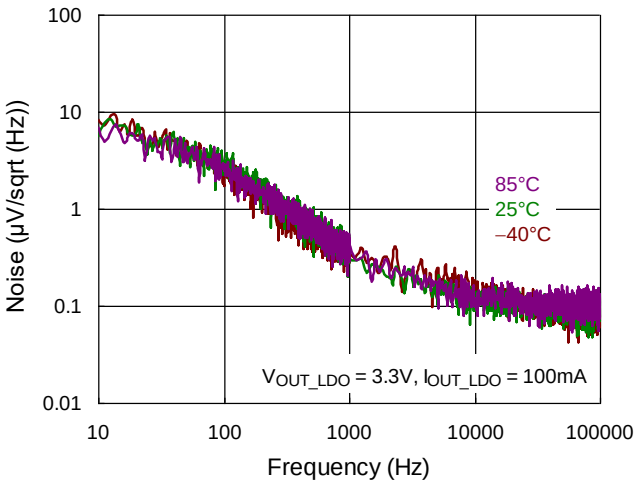
LDO Dropout Voltage vs. Output Current



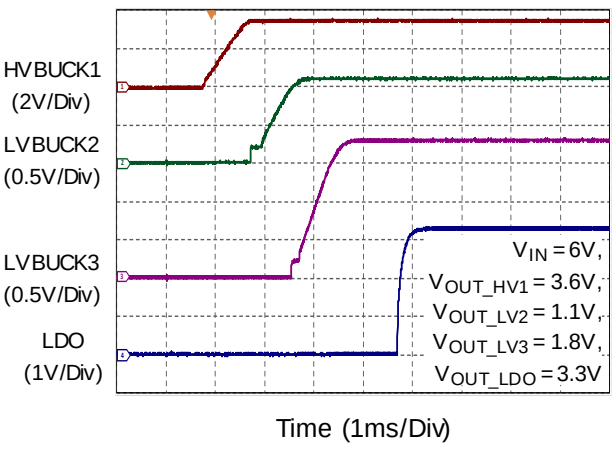
LDO PSRR



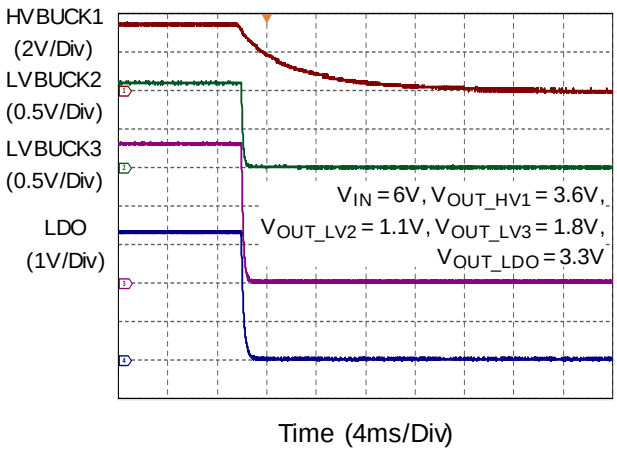
LDO Output Noise



SEQ9 Power On



SEQ9 Power Off



15 Operation

The RTQ2072A-QT/RTQ2072B-QT is a highly integrated power management integrated circuit (PMIC) for automotive camera system. It includes three buck converters (CH1 HVBuck1, CH2 LVBuck2, CH3 LVBuck3) and one generic LDO (CH4 LDO).

15.1 System Undervoltage Protection and Overvoltage Protection

The RTQ2072A-QT/RTQ2072B-QT stops operating if the V_{IN} voltage falls below the Undervoltage Lockout level (UVLO_L). A typical 500mV hysteresis is implemented to avoid unstable on/off behaviors. The shift values of UVLO_H and UVLO_L both move in the same direction (either positive or negative at the same time). The device is initialized to its default state after V_{IN} voltage recovering from UVLO_H. When the V_{IN} voltage reaches the overvoltage protection level, the buck converters, LDO, and SEQOUT (RTQ2072A-QT) are disabled immediately. The IC then enters latch-off state and can only be re-started by toggling the V_{IN} power. Meanwhile, the PG status will be set to 0V to indicate an IC fault condition.

15.2 Over-Temperature Protection

The RTQ2072A-QT/RTQ2072B-QT features over-temperature protection (OTP). When the junction temperature exceeds the typical threshold of 160°C, OTP is activated, disabling all outputs as the device enters a latch-off state. Once the RTQ2072A-QT/RTQ2072B-QT recovers from OTP, the device can only be re-started by toggling the V_{IN} power.

15.3 Pre-Regulator

The device integrates a 4.45V linear regulator (PVCC) supplied by V_{IN} to provide power to the internal circuitry. The PVCC can be used as the pull-up supply for the RSET and SEQ pins, but it is “NOT” allowed to power any other device or circuitry. A 1μF decoupling capacitor must be connected between PVCC and AGND to filter noise and it should be placed as close as possible to the PVCC pin.

15.4 Peak Current Mode Control

The three buck converters utilize the peak current mode control. An internal oscillator initiates the turn-on of the high-side MOSFET switch. At the beginning of each clock cycle, the internal high-side MOSFET switch turns on, allowing current to ramp up in the inductor. By comparing the inductor peak current signal during the high-side MOSFET switch on interval with the internal compensation signal derived from the sensed feedback voltage and reference voltage, the high-side MOSFET switch is turned off and the inductor current continues to flow through the low-side MOSFET switch. This cycle repeats at the next clock cycle. In this way, the regulated inductor current controls duty-cycle and output voltage of the converter.

15.5 Spread-Spectrum Operation

The periodic nature of switching signals trends to concentrate energy at specific frequencies and their harmonics, which can be radiated and potentially cause EMI issues. To address this, the RTQ2072A-QT/RTQ2072B-QT incorporates a spread-spectrum function to meet CISPR and automotive EMI compliances requirements. The spread-spectrum function utilizes a pseudo-random sequence to modulate the switching frequency by +6%. For example, with a typical switching frequency of 2.1 MHz, the frequency range varies from 2.1MHz to 2.226MHz. This ensures that the 2.1MHz switching frequency does not fall within the 1.8MHz AM band limit, thereby minimizing the risk of EMI problems.

15.6 Phase-Shifted Operation

The RTQ2072A-QT/RTQ2072B-QT supports phase-shifted operation to prevent all buck converters from switching simultaneous, thereby further reducing the radiation energy. The internal clock is automatically shifted to different respective sub-clocks for buck converters. For example, in a two-buck converter application, the turn-on times of the high-side MOSFETs are offset by 180 degrees. In three-buck converter application, the phase difference is 120 degrees between each converter.

15.7 Allowable Channel Floating

To save PCB layout space and reduce material costs, the unused low-voltage buck converters (CH2/CH3) can be left with floating pins (SW2/SW3), eliminating the need for inductors and output capacitors. The PVD23 pin must be connected to a fixed voltage for floating detection, and it is permissible to omit the capacitor placement. The RTQ2072A-QT/RTQ2072B-QT automatically detects the pin status during the power-on procedure to determine whether the channel is used. After this detection, any malfunction in an unused channel will not impact the device's operation.

Table 2. Unused Channel Pin Connection

Unused Channel	Unused Pin Number	Unused Pin Name	Pin Configuration
LVBuck2	5	VOUT2	Floating
	6	SW2	Floating
	7	PVD23	Connect to a fixed voltage
LVBuck3	7	PVD23	Connect to a fixed voltage
	8	SW3	Floating
	9	VOUT3	Floating

15.8 Power-Good Indication

The RTQ2072B-QT features an open-drain power- good output (PG) to monitor the output voltage status. Connect a pull-up resistor from the PG pin to an external voltage. Note that it is forbidden to use PVCC as the pulled-up voltage for the PG pin. When the last channel in the power-on sequence reaches 90% of its target output voltage, the PG signal is pulled high to indicate a "Power-Good" status after a 10ms delay, until the device is disabled or any other protection is triggered.

15.9 External Control Output

The RTQ2072A-QT provides an open-drain external control output (SEQOUT) for external devices. To use this function, connect a pull-up resistor from the SEQOUT pin to an external voltage. Note: Do not use PVCC as the pull-up voltage for the SEQOUT pin. For detailed information regarding the power-on sequence, refer to Table 3.

16 Application Information

(Note 13)

16.1 Power Sequence Control

The RTQ2072A-QT/RTQ2072B-QT supports 10 power-on sequences for the buck converters and LDO via the dedicated resistor on SEQ pin. SEQ pin is not allowable at floating state and resistance selected out of range is not guaranteed to correct power-on sequence. In addition, there is only simultaneous power-off for all outputs. To fix the resistor selection on SEQ pin before enabling the device. Any change during the power on procedure is not guarantee to the correct power-on sequence. Below table shows the power-on sequence with its corresponding resistance.

Table 3. Power-On Sequence Control

SEQ No.	Resistance on SEQ (Ω)			Sequence				
	Min	Typ	Max					
SEQ0	1.07M	1.1M	1.13M	CH1	CH4	CH3	CH2	SEQOUT
SEQ1	319k	330k	341k	CH1	CH2	CH3	SEQOUT	CH4
SEQ2	164k	169k	174k	CH1	CH2	SEQOUT	CH3	CH4
SEQ3	81.6k	84.5k	87.4k	CH1	SEQOUT	CH2	CH4	CH3
SEQ4	45.4k	47k	48.6k	CH1	CH2, CH3, CH4, SEQOUT			
SEQ5	26.1k	27k	27.9k	CH1, CH2, CH3, CH4, SEQOUT				
SEQ6	14.5k	15k	15.5k	CH1	CH3	CH2	CH4	SEQOUT
SEQ7	7.78k	8.06k	8.34k	CH1	CH3	CH4	CH2	SEQOUT
SEQ8	Short to PVCC			CH1	SEQOUT	CH2	CH3	CH4
SEQ9	Short to PGND			CH1	CH2	CH3	CH4	SEQOUT

Note 12.

1. The SEQOUT output exists only in the RTQ2072A-QT. After the SEQOUT output high state 1ms passed, the next channel continues to proceed power on sequence.
2. For RTQ2072B-QT, 1ms time interval will substitute the SEQOUT output. Below is the SEQ1 example.

   For RTQ2072A-QT, CH1 → CH2 → CH3 → SEQOUT → CH4

   For RTQ2072B-QT, CH1 → CH2 → CH3 → 1ms → CH4

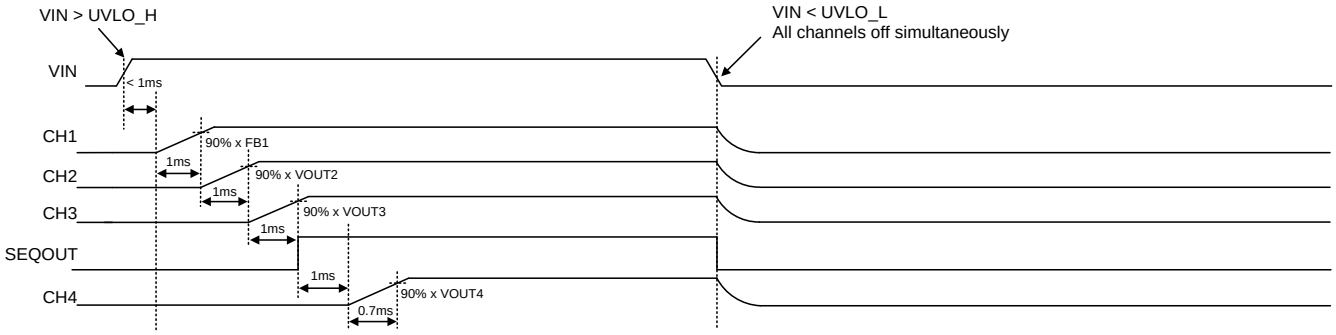


Figure 1. Example SEQ1 for RTQ2072A-QT

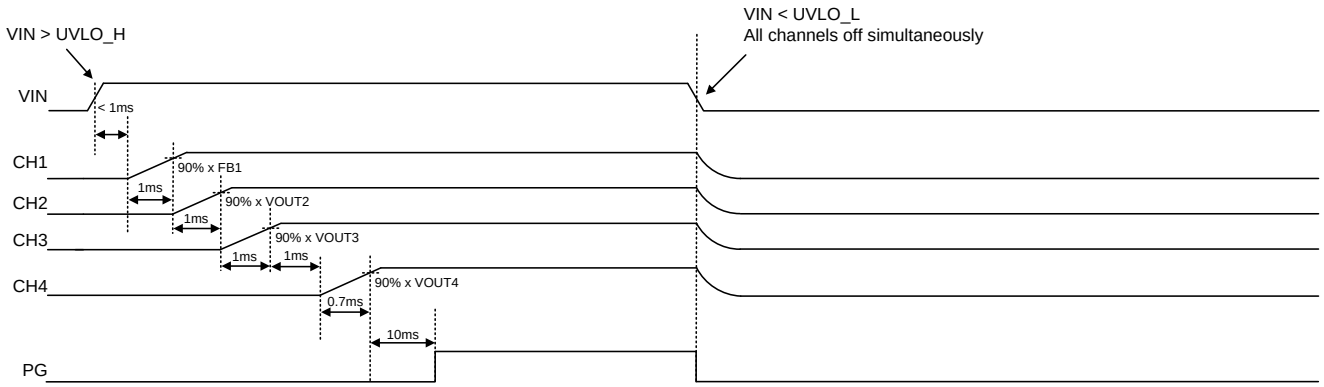


Figure 2. Example SEQ1 for RTQ2072B-QT

16.2 Output Voltage Setting

The section describes how to set the output voltages for each channel.

16.2.1 HVBuck1

The output voltage set by external feedback resistors is expressed in the following equation:

$$V_{OUT_HV1} = \left(1 + \frac{R1}{R2}\right) \times V_{FB1}$$

where the reference voltage V_{FB1} is 0.8V (typical).

The placement of the resistive divider should be as close as possible to the FB1 pin. For better output voltage accuracy, the divider resistors with ±1% tolerance or better should be used. The recommended resistance ranges from a few kΩ to hundreds of kΩ.

16.2.2 LVBuck2 and LVBuck3

The output voltage of LVBuck2 is fixed at 1.1V.

The output voltage of LVBuck3 is fixed at 1.8V.

16.2.3 LDO

The LDO output voltage is controlled by setting the dedicated resistor on the RSET pin. The RSET pin must not be left floating, and resistance selected out of range is not guaranteed to result in the correct output voltage. Changing the output voltage in real-time is not recommended. Ensure the resistor selection on the RSET pin is fixed before enabling the device.

Table 4. LDO Output Voltage

RSET No.	Resistor on REST (Ω)			Voltage (V)
	Min	Typ	Max	
RSET0	1.07M	1.1M	1.13M	3.5
RSET1	319k	330k	341k	3.4
RSET2	164k	169k	174k	3.2
RSET3	81.6k	84.5k	87.4k	3.1
RSET4	45.4k	47k	48.6k	3.0
RSET5	26.1k	27k	27.9k	2.8
RSET6	14.5k	15k	15.5k	2.7
RSET7	7.78k	8.06k	8.34k	1.8
RSET8	Short to PVCC			2.9
RSET9	Short to PGND			3.3

16.3 Channel Protection Features

The RTQ2072A-QT/RTQ2072B-QT is equipped with protections to prevent the device from being damaged by abnormal operations or fault conditions (For example, over-load, short-circuit, soldering issues, etc.).

16.3.1 Undervoltage Protection (UVP)

- **HVBuck1, LVBuck2, LVBuck3, and LDO**

The device disables all channels and enters the latch-off state if a buck converter or LDO output under voltage fault is detected continuously over the deglitch time. The device can only be re-started by toggling the V_{IN} power.

16.3.2 Overvoltage Protection (OVP)

- **HVBuck1**

  When an overvoltage fault is detected at the FB1 pin, the high-side and low-side MOSFETs turn off immediately and auto-recover to switch until the FB1 pin's voltage decreases to the reset level.

- **LVBuck2, LVBuck3, and LDO**

  The device disables all channels when a buck converter or LDO output overvoltage fault is detected continuously over the deglitch time. When the fault is cleared, the device auto-restarts all channels in sequence.

16.3.3 Overcurrent Protection (OCP)

- **HVBuck1, LVBuck2, and LVBuck3**

  The buck converter includes a cycle-by-cycle high-side MOSFET overcurrent protection against the condition where the inductor current increases abnormally, even over the inductor saturation current rating. If an over-current condition occurs, the controller will immediately turn off the high-side MOSFET and turn on the low-side MOSFET to prevent the inductor current from exceeding the peak current-limit level. After the inductor current decreases below the valley current limit, the high-side MOSFET resumes switching on. If an overcurrent fault is further detected continuously over the deglitch time, the device disables all channels and enters latch-off state. The device can only be re-started by toggling the V_{IN} power.

- **LDO**

  When the load reaches the current limit threshold, the current sent to the output will be kept at current limit level. If overcurrent fault detected continuously over the deglitch time, the device disables all channels and enters the latch off state and the device only can re-start with V_{IN} ON/ OFF.

16.3.4 Input Overvoltage Protection (OVP)

- **LVBuck2, LVBuck3, and LDO**

  If the input voltage of the buck converters (LVBuck2, LVBuck3) or LDO reaches the overvoltage protection level, the device disables all channels. After the fault is removed, it auto-restarts all channels in sequence.

Table 5. Protection Behavior

Channel	Type	Threshold (Typical)	Deglitch Time (Typical)	Protection	Reset and Threshold (Typical)
System	UVLO	$V_{IN} \leq 3.3V$ (after IC Operation)	32μs	Disable all channels	$V_{IN} \geq 3.8V$
	OVP	$V_{IN} \geq 20V$	5ms	Disable all channels and then enter latch-off protection	$V_{IN} \leq 3.3V$, then $V_{IN} \geq 3.8V$

Channel	Type	Threshold (Typical)	Deglitch Time (Typical)	Protection	Reset and Threshold (Typical)
	OTP	T_J ≥ 160°C	5μs	Disable all channels and then enter latch-off protection	T_J ≤ 140°C and V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
CH1 HVBuck1	UVP	V_{FB1} ≤ 0.8V x 50%	5μs	Disable all channels and then enter latch-off protection	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	OVP	V_{FB1} ≥ 0.8V x 110%	NA	High/Low-side MOSFETs off, low-side MOSFET conditionally ON to charge the BOOT capacitor for driving high-side MOSFET.	V_{FB1} < 0.8V x 110%
	OCP	I_{L1_peak} ≥ 3A	10ms	Cycle-by-cycle detection If the condition persists for10ms, disable all channels and then enter latch-off protection	If latch-off protection, V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
CH2 LVBuck2	UVP	V_{OUT_LV2} ≤ 1.1V x 50%	5μs	Disable all channels and then enter latch-off protection	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	OVP	V_{OUT_LV2} ≥ 1.1V x 120%	5ms	Disable all channels	V_{OUT2} ≤ 1.1V x 110% with deglitch 5ms
	OCP	I_{L2_peak} ≥ 2A	10ms	Cycle-by-cycle detection If the condition persists for10ms, disable all channels then latch-off protection	If latch-off protection, V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	Input OVP	V_{IN_PVD23} ≥ 5.8V	5μs	Disable all channels	V_{IN_PVD23} ≤ 5.22V with deglitch 5μs
CH3 LVBuck3	UVP	V_{OUT_LV3} ≤ 1.8V x 50%	5μs	Disable all channels and then enter latch-off protection	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	OVP	V_{OUT_LV3} ≥ 1.8V x 120%	5ms	Disable all channels	V_{OUT3} ≤ 1.8V x 110% with deglitch 5ms
	OCP	I_{L3_peak} ≥ 1.2A	10ms	Cycle-by-cycle detection If the condition persists for10ms, disable all channels then latch-off protection	If latch-off protection, V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	Input OVP	V_{IN_PVD23} ≥ 5.8V	5μs	Disable all channels	V_{IN_PVD23} ≤ 5.22V with deglitch 5μs
CH4 LDO	UVP	V_{OUT_LDO} ≤ V_{OUT_LDO} setting x 40%	5μs	Disable all channels and then enter latch-off protection	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V
	OVP	V_{OUT_LDO} ≥ V_{OUT_LDO} x 125%	5ms	Disable all channels	V_{OUT_LDO} ≤ V_{OUT_LDO} x 110% with deglitch 5ms
	OCP	I_{OUT_LDO} ≥ 450mA	10ms	Disable all channels and then enter latch-off	V_{IN} ≤ 3.3V, then V_{IN} ≥ 3.8V

Channel	Type	Threshold (Typical)	Deglitch Time (Typical)	Protection	Reset and Threshold (Typical)
				protection	
	Input OVP	V_{IN_LDO} ≥ 5.8V	5μs	Disable all channels	V_{IN_LDO} ≤ 5.3V with deglitch 5μs

16.4 Input and Output Capacitor Selection

16.4.1 HVBuck1, LVBuck2 and LVBuck3

It is recommended at least a 4.7μF input capacitor with a 10μF output capacitor for buck converters. The ripple voltage is an important index for choosing the output capacitor. This portion consists of two parts. One is the product of ripple current with the ESR of the output capacitor, while the other part is formed by the charging and discharging process of the output capacitor. The output ripple can be calculated as below:

$$\Delta V_{OUTRipple} = \Delta V_{ESR} + \Delta V_{OUT} = \Delta V_{ESR} + \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

where $\Delta V_{ESR} = I_{Crms} \times R_{CESR}$

16.4.2 LDO

As with any low dropout regulator, careful selection of external capacitors is essential for the stability and performance of the RTQ2072A-QA/RTQ2072B-QA. A 2.2μF capacitor is recommended for both the input and output of the LDO.

Adding additional output capacitor can further improve noise suppression; however, it may also result in higher input inrush current when the LDO starts up. This trade-off should be carefully considered during design.

16.5 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula:

$P_{D(MAX)} = (T_{J(MAX)} – T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature; T_A is the ambient temperature; and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 150°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WETD-VQFN-16L 3x3 package, the thermal resistance, θ_{JA}, is 30°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four- layer test board. The maximum power dissipation at T_A = 25°C can be calculated as follows:

$P_{D(MAX)}$ = (150°C – 25°C) / (30°C/W) = 4.16W for a WETD-VQFN-16L 3x3 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curve in Figure 3 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

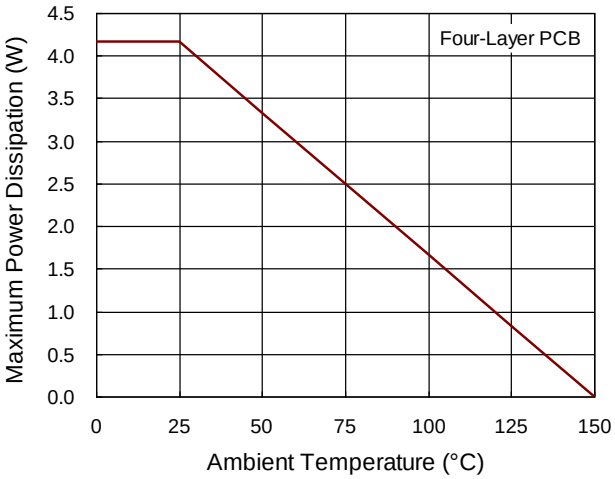


Figure 3. Derating Curve of Maximum Power Dissipation

16.6 Layout Considerations

The PCB layout is an important step to maintain the high performance of the RTQ2072A-QT/RTQ2072B-QT. Both the high current and the fast switching nodes demand full attention to the PCB layout to keep the robustness of the RTQ2072A-QT/RTQ2072B-QT through the PCB layout. Improper layout might lead to the symptoms of poor line or load regulation, ground and output voltage shifts, stability issues, unsatisfying EMI behavior or worsened efficiency. For the best performance of the RTQ2072A-QT/RTQ2072B-QT, the following PCB layout guidelines must be strictly followed.

- The trace from the switching node to the inductor should be kept as short as possible to minimize the switching loop for better EMI.
- Place the input and output capacitors as close as possible to the corresponding input and output pins to ensure optimal filtering performance.
- Keep the main power traces as wide and short as possible.
- Connect the AGND and PGND to a solid ground plane to improve thermal dissipation and enhance noise immunity.
- Directly connect the buck converter’s output capacitor to the feedback network to minimize voltage fluctuations caused by parasitic resistance and inductance in the PCB traces.

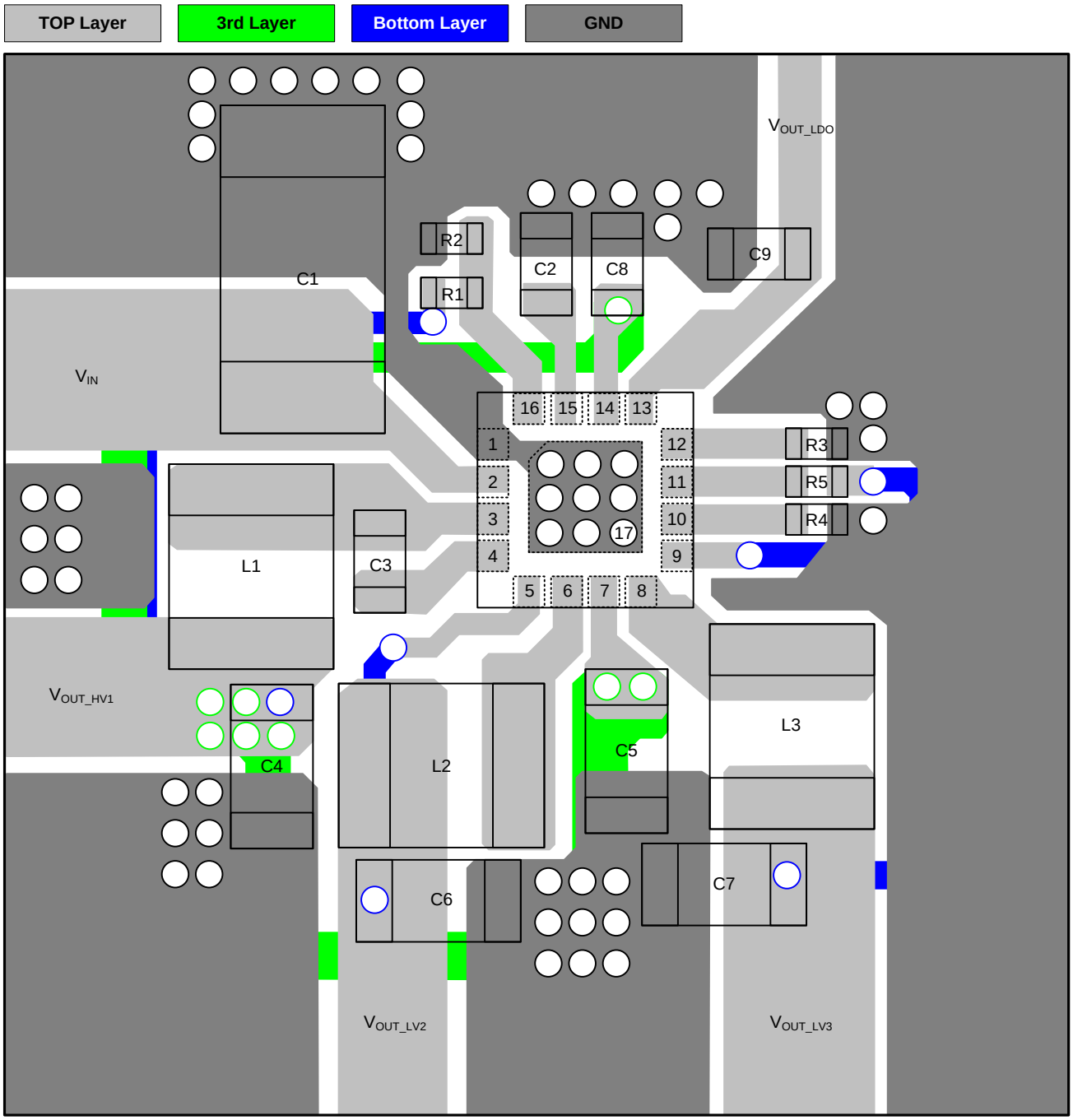
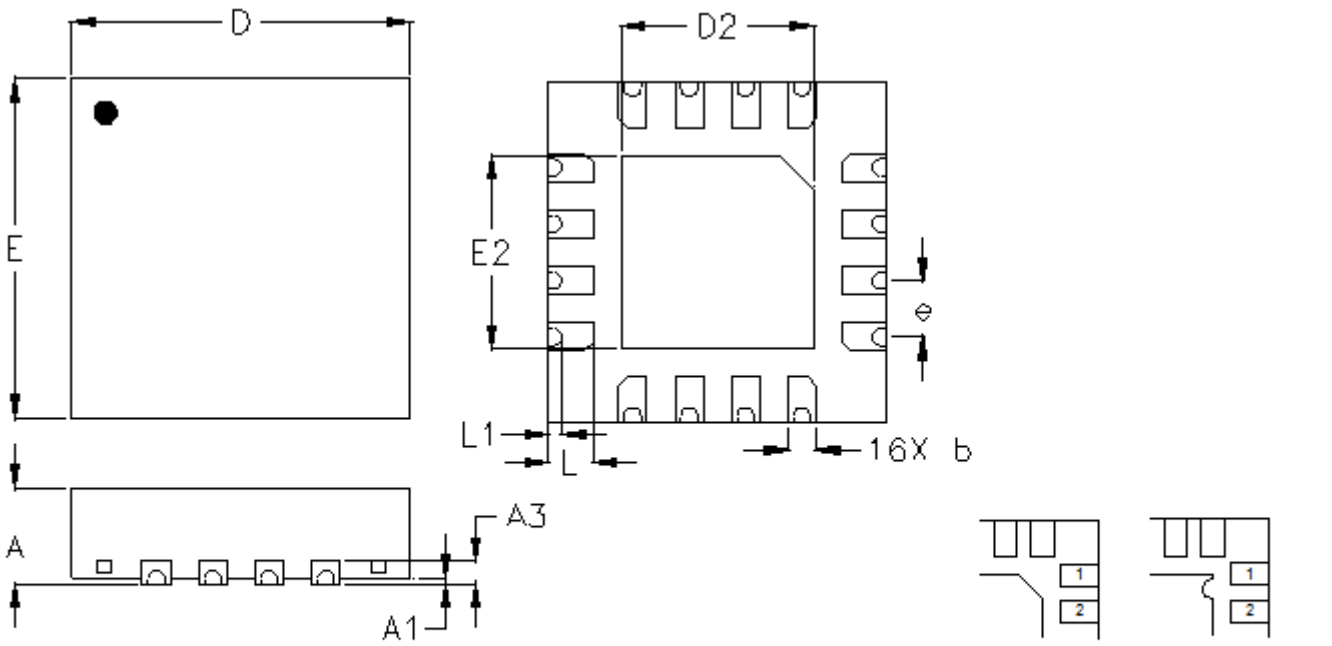


Figure 4. PCB Layout Guide

Note 13. The information provided in this section is for reference only. The customer is solely responsible for the designing, validating, and testing your product incorporating Richtek's product and ensure such product meets applicable standards and any safety, security, or other requirements.

17 Outline Dimension



DETAIL A

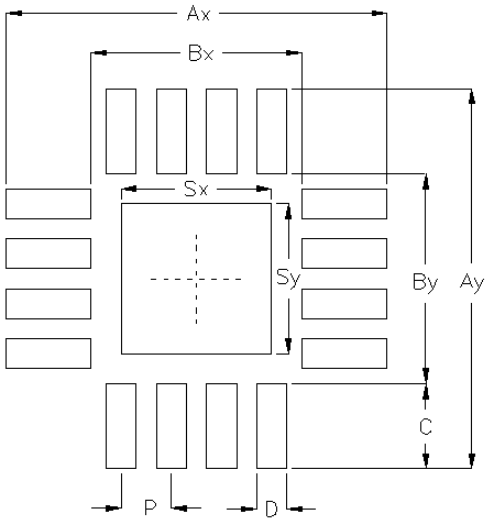
Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.000	0.031	0.039
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.650	1.750	0.065	0.069
E	2.950	3.050	0.116	0.120
E2	1.650	1.750	0.065	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018
L1	0.075	0.175	0.003	0.007

WETD V-Type 16L QFN 3x3 Package

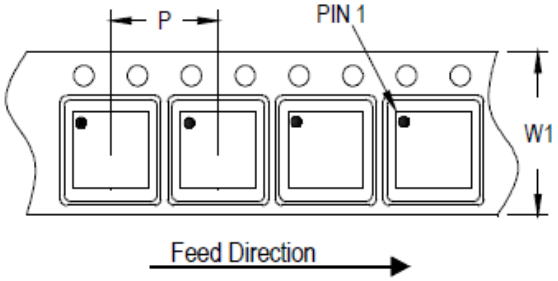
18 Footprint Information

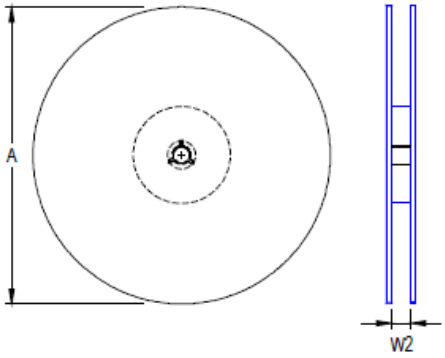


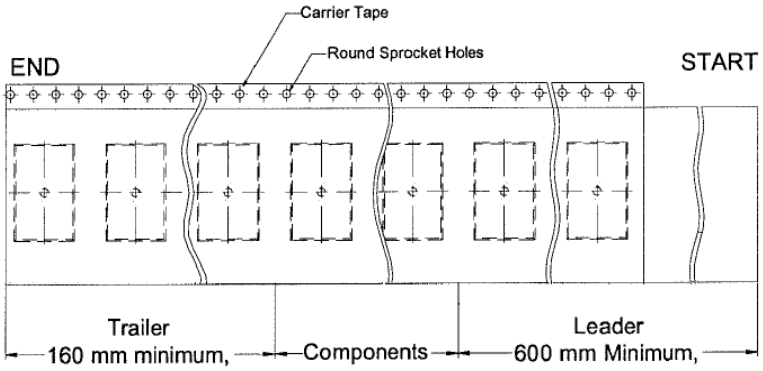
Package	Number of Pin	Footprint Dimension (mm)									Tolerance
		P	Ax	Ay	Bx	By	C	D	Sx	Sy	
WETD-V/W/U/XQFN3x3-16	16	0.50	3.80	3.80	2.10	2.10	0.85	0.30	1.50	1.50	±0.05

19 Packing Information

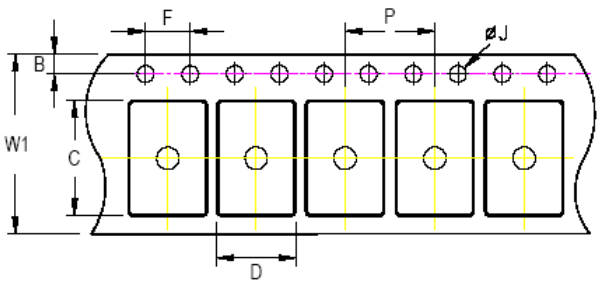
19.1 Tape and Reel Data







Package Type	Tape Size (W1) (mm)	Pocket Pitch (P) (mm)	Reel Size (A)		Units per Reel	Trailer (mm)	Leader (mm)	Reel Width (W2) Min/Max (mm)
			(mm)	(in)				
(V, W) QFN/DFN 3x3	8	4	180	7	3,000	160	600	8.4/9.9



C, D, and K are determined by component size. The clearance between the components and the cavity is as follows:

- For 8mm carrier tape: 0.5mm maximum

Tape Size	W1	P		B		F		ØJ		K		H
	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Max
8mm	8.3mm	3.9mm	4.1mm	1.65mm	1.85mm	3.9mm	4.1mm	1.5mm	1.6mm	1.0mm	1.3mm	0.6mm

19.2 Tape and Reel Packing

Step	Photo/Description	Step	Photo/Description
1	 Reel 7”	4	 3 reels per inner box **Box A**
2	 HIC & Desiccant (1 Unit) inside	5	 12 inner boxes per outer box
3	 Caution label is on backside of Al bag	6	 Outer box **Carton A**

Container / Package	Reel		Box			Carton		
	Size	Units	Item	Reels	Units	Item	Boxes	Unit
(V, W) QFN & DFN 3x3	7”	3,000	Box A	3	9,000	Carton A	12	108,000
			Box E	1	3,000	For Combined or Partial Reel.		

19.3 Packing Material Anti-ESD Property

Surface Resistance	Aluminum Bag	Reel	Cover tape	Carrier tape	Tube	Protection Band
Ω/cm^2	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**	**10^4 to 10^{11}**

20 Datasheet Revision History

Version	Date	Description
02	2023/7/31	Ordering Information on P1 Electrical Characteristics on P9 Application Information on P19 Packing Information on P28, 29, 30
03	2025/9/3	General Description - Modified product number. Ordering Information - Modified notes and updated ordering information Packing Information - Modified packing information.