

SGM48524

Dual 5A, High-Speed, Low-Side Gate Driver with Negative Input Voltage Capability

GENERAL DESCRIPTION

The SGM48524 is a dual high-speed low-side gate driver for power switches. It has rail-to-rail driving capability and can sink or source up to 5A peak current with capacitive loads. The propagation delays are very short and well matched between the two channels that make the device well suited for applications that need accurate dual gate driving such as synchronous rectifiers. The matched propagation delays also allow for paralleling the two channels when higher driving current is required (such as for paralleled switches). The input voltage thresholds are fixed, independent of supply voltage (V_{DD}), and compatible with low voltage TTL and CMOS logic. Noise immunity is excellent due to the wide hysteresis window between the input low and high thresholds. The device has internal pull-up/pull-down resistors on the input pins to ensure low state on the driver output when the input is floating.

The SGM48524 is available in Green SOIC-8, TDFN-3×3-8L and MSOP-8 (Exposed Pad) packages.

APPLICATIONS

Switched-Mode Power Supplies
DC-DC Converters
Motor Control, Solar Power
Gate Drive for Emerging Wide Band-Gap Power
Devices such as GaN

FEATURES

- Two Independent Gate Drive Channels
- 5A Source and 5A Sink Peak Currents
- Wide Supply Voltage Range: 4.5V to 18V
- TTL and CMOS Compatible Logic Threshold
- Logic Levels Independent of Supply Voltage
- Hysteretic Input Logic for High Noise Immunity
- Outputs Held Low When Inputs are Floating
- Fast Propagation Delays: 18ns (TYP)
- Fast Rise Time: 7ns (TYP)
- Fast Fall Time: 7ns (TYP)
- Ringing Suppression
- Negative Voltage Capability on INx Pins:
-10V when $(V_{DD} - V_{INx}) \leq 20V$
- Negative Voltage Capability on ENx Pins:
-10V when $(V_{DD} - V_{ENx}) \leq 20V$
- Negative Voltage Capability on OUTx Pin:
-2V (Pulse < 200ns)
- Comprehensive Protection Features
 - Thermal Shutdown Protection
 - Under-Voltage Lockout
 - Short-Circuit Protection
- -40°C to +125°C Operating Temperature Range
- Available in Green SOIC-8, MSOP-8 (Exposed Pad) and TDFN-3×3-8L Packages

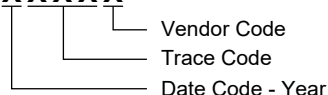
PACKAGE/ORDERING INFORMATION

| MODEL | PACKAGE DESCRIPTION | SPECIFIED TEMPERATURE RANGE | ORDERING NUMBER | PACKAGE MARKING | PACKING OPTION |
|----------|-------------------------|-----------------------------|-------------------|----------------------------|---------------------|
| SGM48524 | SOIC-8 | -40°C to +125°C | SGM48524XS8G/TR | SGM 48524XS8 XXXXX | Tape and Reel, 4000 |
| | MSOP-8 (Exposed Pad) | -40°C to +125°C | SGM48524XPMS8G/TR | SGM48524 XPMS8 XXXXX | Tape and Reel, 4000 |
| | TDFN-3×3-8L | -40°C to +125°C | SGM48524XTDB8G/TR | SGM 48524DB XXXXX | Tape and Reel, 4000 |

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.

XXXXX



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

| | |
|---|--------------------------|
| VDD | -0.3V to 20V |
| Continuous INA, INB when $(V_{DD} - V_{INx}) \leq 20V$ | -10V to $V_{DD} + 0.3V$ |
| Continuous ENA, ENB when $(V_{DD} - V_{ENx}) \leq 20V$ | -10V to $V_{DD} + 0.3V$ |
| Continuous OUTA, OUTB (DC) | -0.3V to $V_{DD} + 0.3V$ |
| Pulse OUTA, OUTB (Pulse < 200ns)..... | -2V to $V_{DD} + 0.3V$ |
| Package Thermal Resistance | |
| SOIC-8, θ_{JA} | 121°C/W |
| MSOP-8 (Exposed Pad), θ_{JA} | 55°C/W |
| TDFN-3×3-8L, θ_{JA} | 70°C/W |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (Soldering, 10s) | +260°C |
| ESD Susceptibility | |
| HBM | 7000V |
| CDM | 1000V |

RECOMMENDED OPERATING CONDITIONS

| | |
|--|-----------------|
| Supply Voltage Range | 4.5V to 18V |
| Operating Junction Temperature Range | -40°C to +125°C |

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

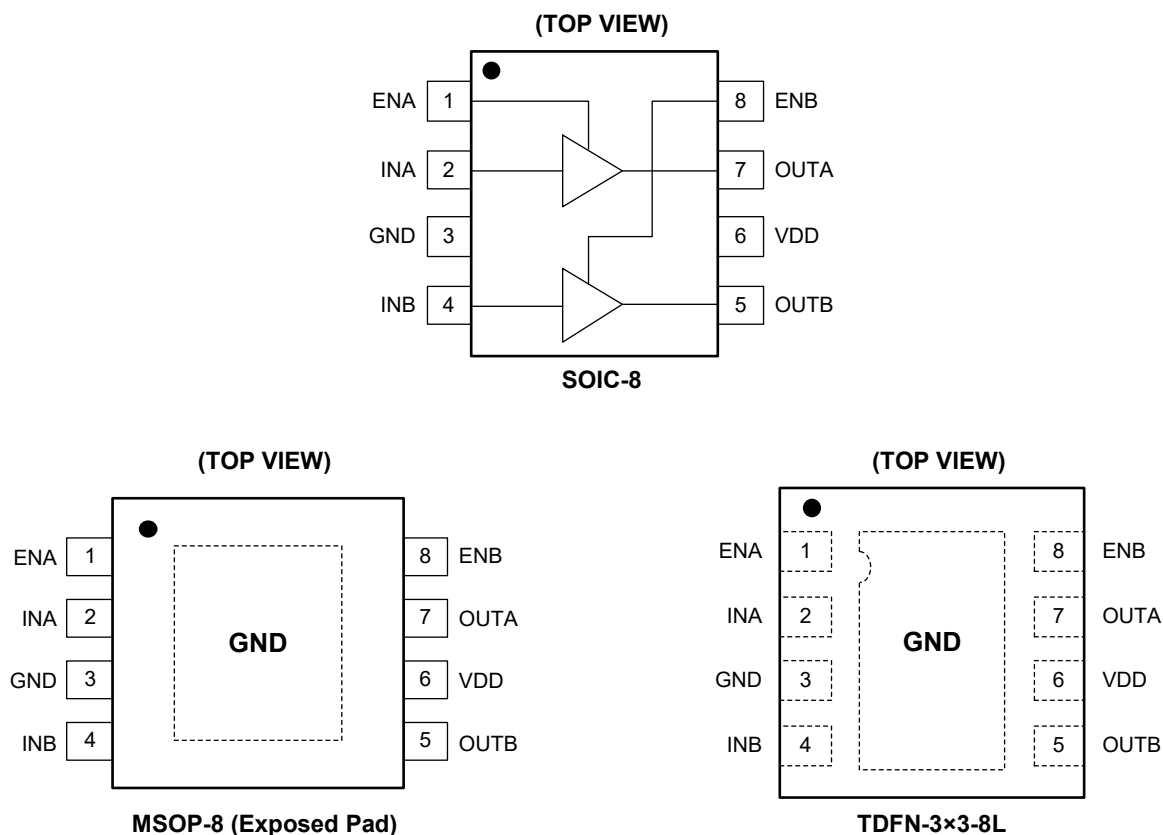
ESD SENSITIVITY CAUTION

This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS



PIN DESCRIPTION

| PIN | NAME | I/O | FUNCTION |
|-------------|------|-----|--|
| 1 | ENA | I | Enable Input for Channel A. ENA biased low disables channel A output regardless of INA state. ENA biased high or floating enables channel A output. |
| 2 | INA | I | Non-Inverting Input to Channel A. OUTA is held low if INA is unbiased or floating. |
| 3 | GND | — | Ground. Reference pin for all signals. |
| 4 | INB | I | Non-Inverting Input to Channel B. OUTB is held low if INB is unbiased or floating. |
| 5 | OUTB | O | Channel B Output. |
| 6 | VDD | I | Power Supply Input. |
| 7 | OUTA | O | Channel A Output. |
| 8 | ENB | I | Enable Input for Channel B. ENB biased low disables channel B output regardless of INB state. ENB biased high or floating enables channel B output. |
| Exposed Pad | GND | — | Exposed Pad. Exposed pad is internally connected to GND. Connect it to a large ground plane to maximize thermal performance; not intended as an electrical connection point. |

NOTE: I: input, O: output.

FUNCTION TABLE

| ENA | ENB | INA | INB | OUTA | OUTB |
|----------|----------|----------|----------|------|------|
| H | H | L | L | L | L |
| H | H | L | H | L | H |
| H | H | H | L | H | L |
| H | H | H | H | H | H |
| L | L | Any | Any | L | L |
| Any | Any | Floating | Floating | L | L |
| Floating | Floating | L | L | L | L |
| Floating | Floating | L | H | L | H |
| Floating | Floating | H | L | H | L |
| Floating | Floating | H | H | H | H |

TYPICAL APPLICATION

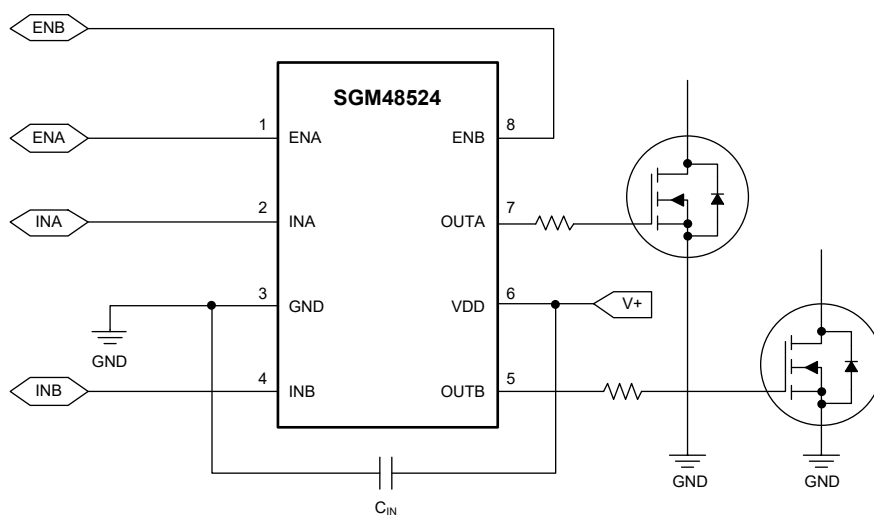


Figure 1. Typical Application Circuit

ELECTRICAL CHARACTERISTICS

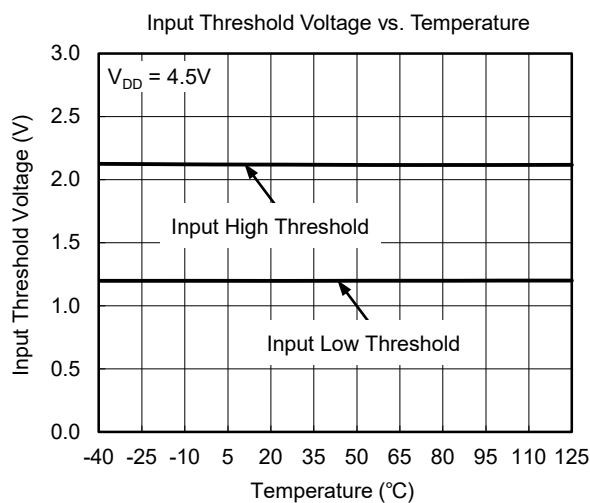
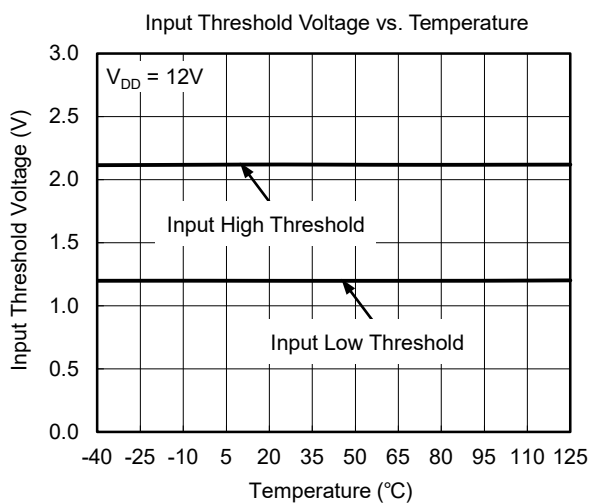
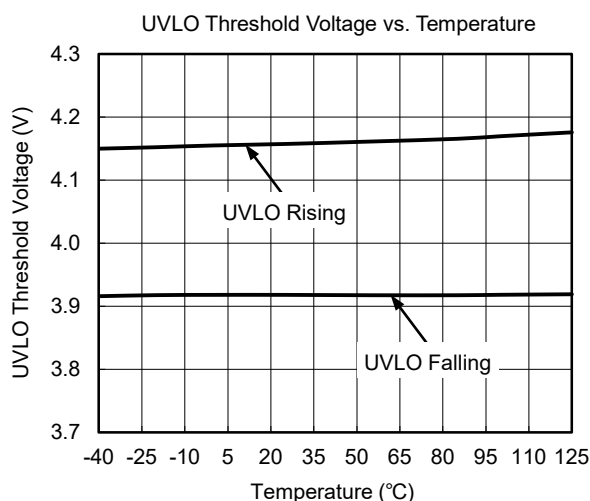
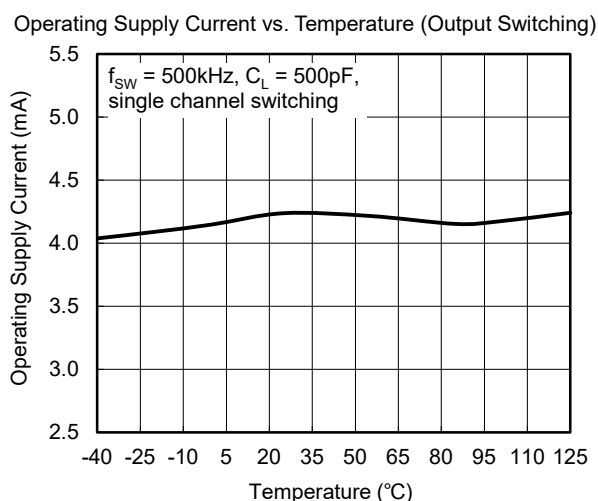
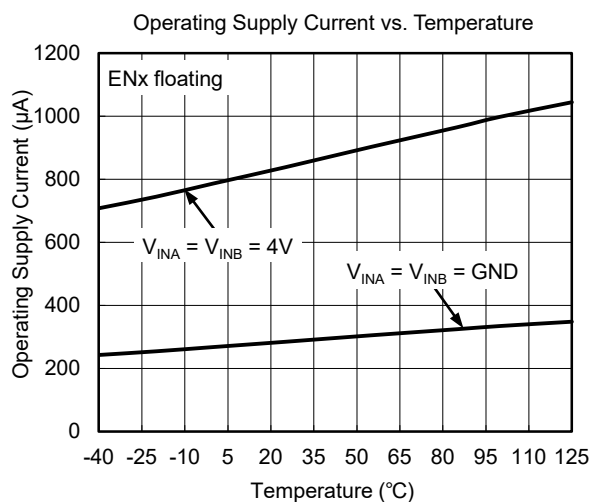
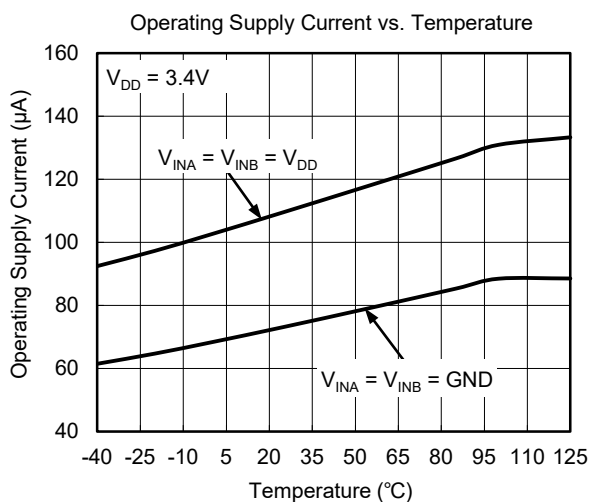
(V_{DD} = 12V, C_{IN} = 4.7μF, T_J = -40°C to +125°C, typical values are at T_J = +25°C, unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------------------------------|---|------|------|------|-------|
| Power Supplies | | | | | | |
| VDD Operating Supply Voltage | V _{DD} | | 4.5 | | 18 | V |
| VDD Operating Supply Current | I _{DD} | V _{DD} = 3.4V, V _{INA} = V _{INB} = GND | | 75 | 120 | μA |
| | | V _{DD} = 3.4V, V _{INA} = V _{INB} = V _{DD} | | 110 | 170 | |
| | | INx and ENx floating | | 285 | 440 | |
| VDD Under-Voltage Lockout Voltage | V _{ON} | | 3.9 | 4.15 | 4.45 | V |
| | V _{OFF} | | 3.65 | 3.9 | 4.2 | V |
| Supply Voltage Hysteresis | V _{HYS} | | 0.15 | 0.25 | 0.35 | V |
| Inputs (INA, INB) | | | | | | |
| Input Signal High Threshold | V _{IN_H} | | 1.9 | 2.1 | 2.3 | V |
| Input Signal Low Threshold | V _{IN_L} | | 1 | 1.2 | 1.4 | V |
| Input Hysteresis | V _{IN_HYS} | | 0.7 | 0.9 | 1.1 | V |
| Input Low Current | I _{IL} | V _{DD} = 18V, T _J = +25°C | | 0.1 | 1 | μA |
| Input High Current | I _{IH} | V _{DD} = 18V, T _J = +25°C | | 100 | 135 | μA |
| Enable (ENA, ENB) | | | | | | |
| Enable Signal High Threshold | V _{EN_H} | | 1.9 | 2.1 | 2.3 | V |
| Enable Signal Low Threshold | V _{EN_L} | | 1 | 1.2 | 1.4 | V |
| Enable Hysteresis | V _{EN_HYS} | | 0.7 | 0.9 | 1.1 | V |
| Enable Low Current | I _{ENL} | V _{DD} = 18V, T _J = +25°C | | 96 | 130 | μA |
| Enable High Current | I _{ENH} | V _{DD} = 18V, T _J = +25°C | | 1.9 | 10 | μA |
| Outputs (OUTA, OUTB) | | | | | | |
| Output Pull-Up Resistance ⁽¹⁾ | R _{OH} | I _{OUT} = 10mA | | 4.6 | 7.2 | Ω |
| Output Pull-Down Resistance | R _{OL} | I _{OUT} = -10mA | | 465 | 800 | mΩ |
| Peak Output Current | I _{PK_SOURCE} | C _L = 0.22μF, f _{SW} = 1kHz | | 5 | | A |
| | I _{PK_SINK} | | | 5 | | A |
| Switching Characteristics | | | | | | |
| Rise Time | t _R | C _L = 1.8nF, see Figure 2 and Figure 3 | | 7 | | ns |
| Fall Time | t _F | C _L = 1.8nF, see Figure 2 and Figure 3 | | 7 | | ns |
| Delay Matching between 2 Channels | t _M | INA = INB, OUTA and OUTB at 50% transition point | | 1 | | ns |
| Input to Output Propagation Delay | t _{D1} , t _{D2} | C _L = 1.8nF, 4V input pulse, see Figure 2 | | 18 | | ns |
| EN to Output Propagation Delay | t _{D3} , t _{D4} | C _L = 1.8nF, 4V enable pulse, see Figure 3 | | 18 | | ns |
| Protection Circuits | | | | | | |
| Thermal Shutdown Temperature | T _{TSD} | | | 165 | | °C |
| Thermal Shutdown Temperature Hysteresis | T _{HYS} | | | 25 | | °C |

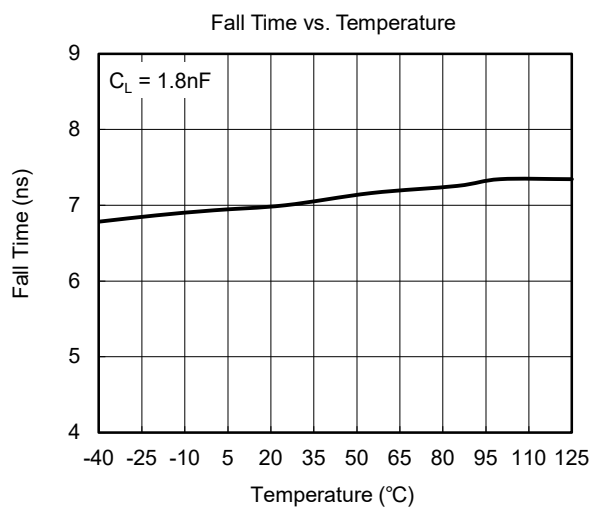
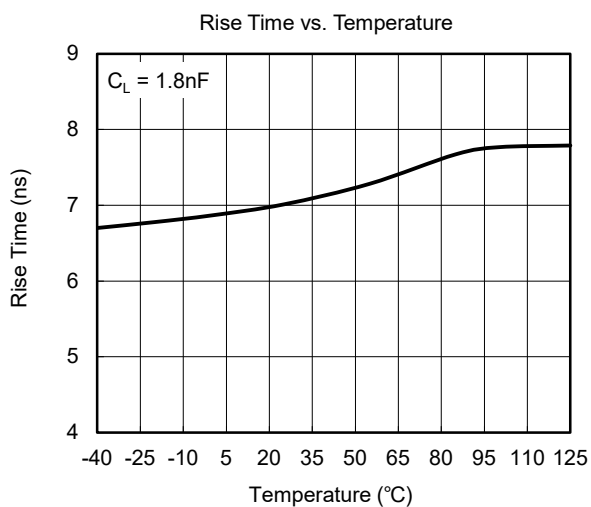
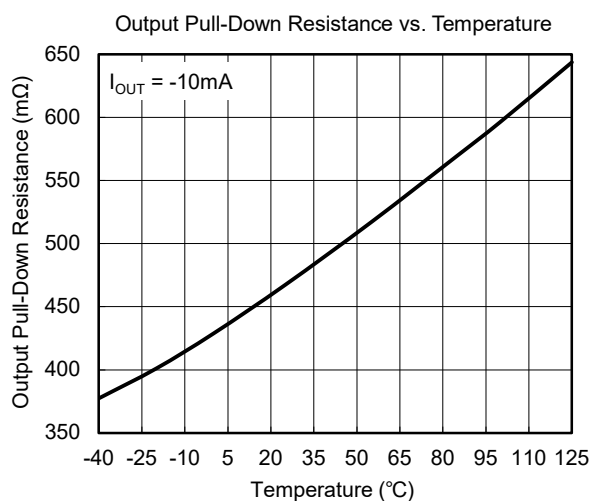
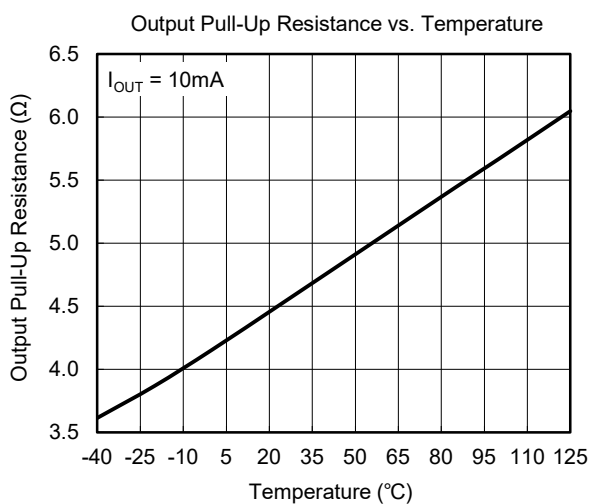
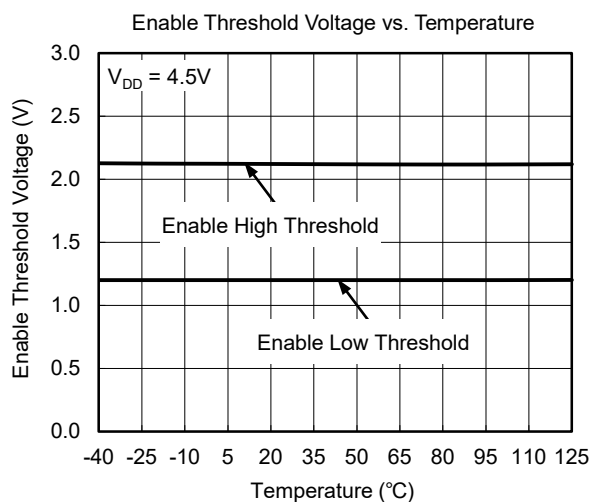
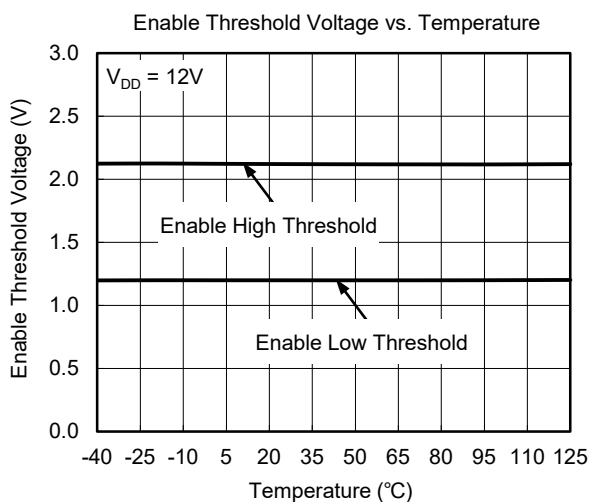
NOTE:

1. R_{OH} represents constant pull-up resistance only. Pull-up resistance R_{OH_PULSE} operates in pulse mode during the output rising stage, R_{OH_PULSE} = 730mΩ (TYP).

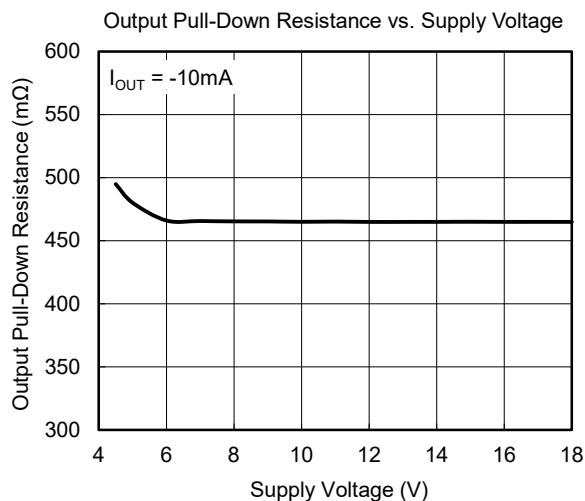
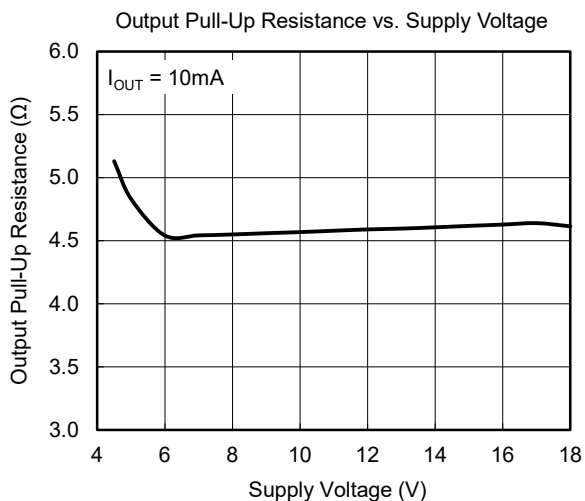
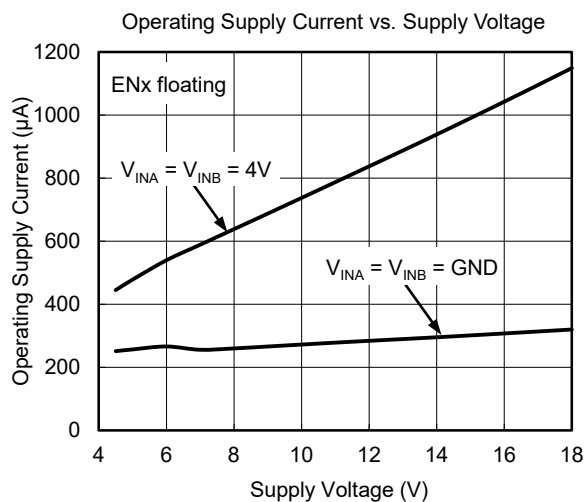
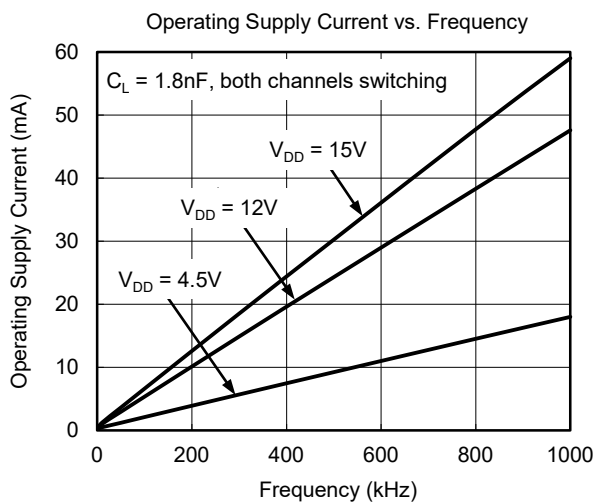
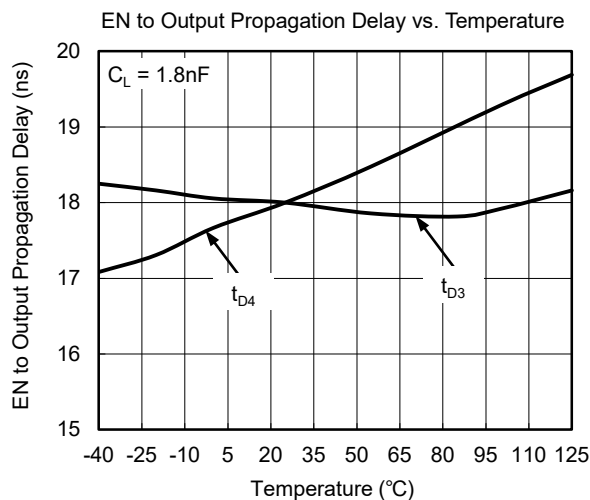
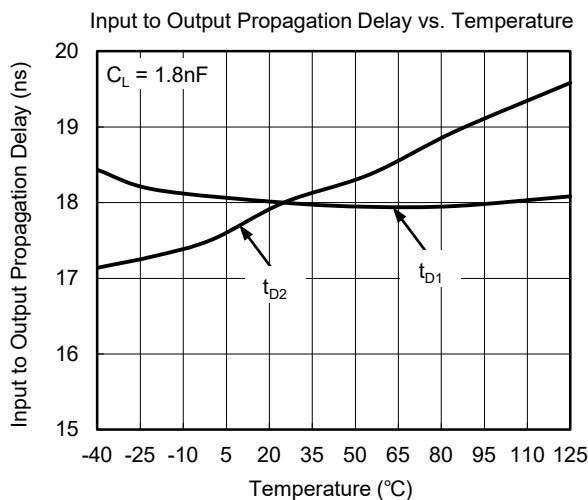
TYPICAL PERFORMANCE CHARACTERISTICS

At $T_J = +25^\circ\text{C}$, $V_{DD} = 12\text{V}$, $C_{IN} = 4.7\mu\text{F}$, unless otherwise noted.

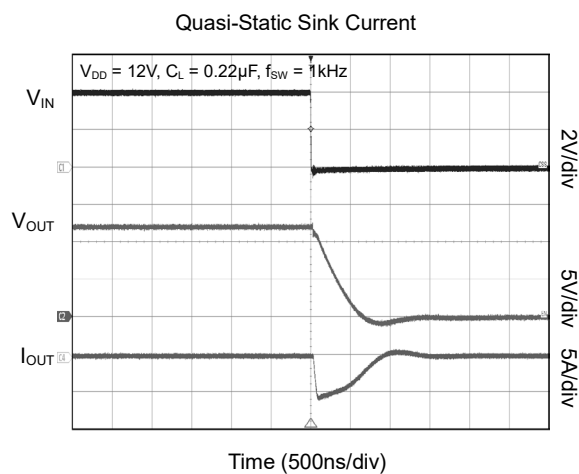
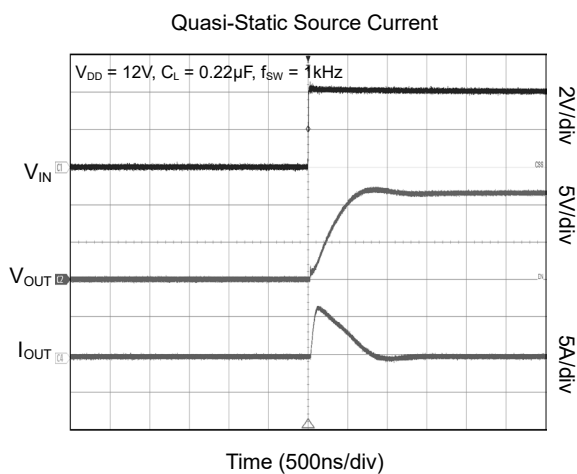
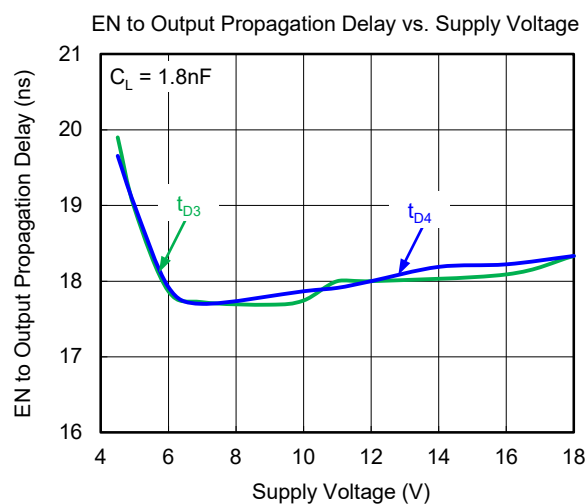
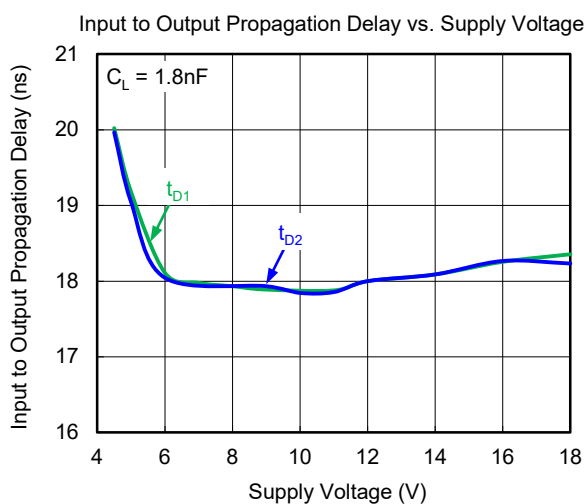
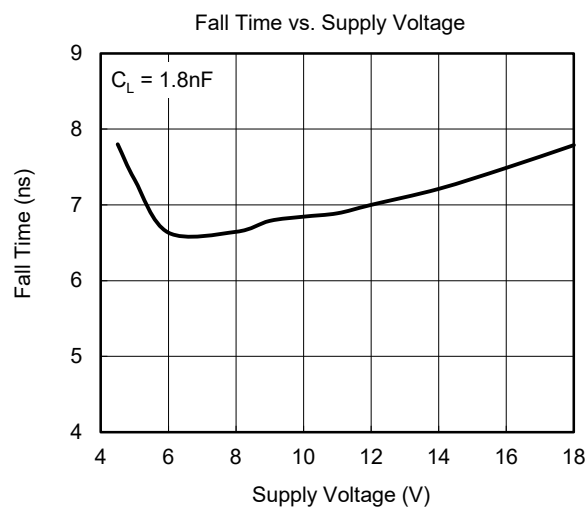
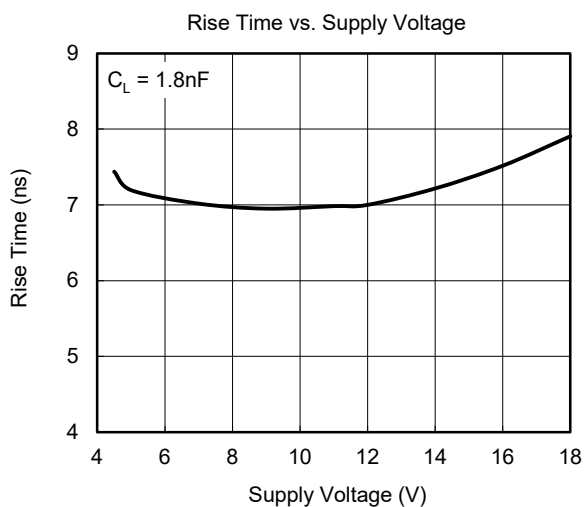
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J = +25^\circ\text{C}$, $V_{DD} = 12\text{V}$, $C_{IN} = 4.7\mu\text{F}$, unless otherwise noted.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J = +25^\circ\text{C}$, $V_{DD} = 12\text{V}$, $C_{IN} = 4.7\mu\text{F}$, unless otherwise noted.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At $T_J = +25^\circ\text{C}$, $V_{DD} = 12\text{V}$, $C_{IN} = 4.7\mu\text{F}$, unless otherwise noted.

TIMING DIAGRAMS

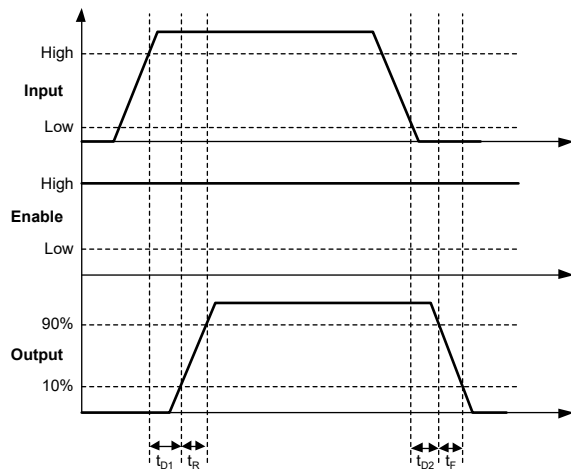
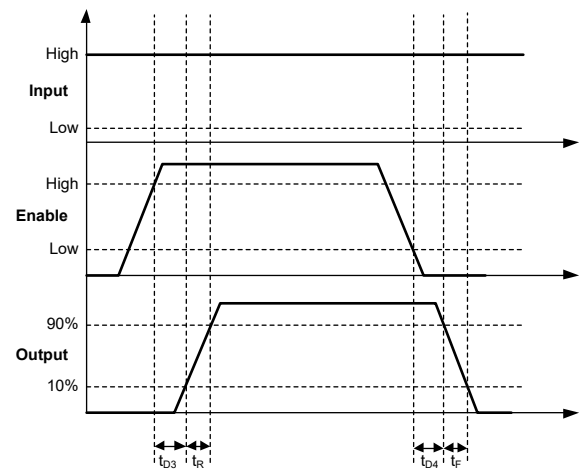


Figure 2. Non-Inverting Input Driver Operation

Figure 3. Enable Function
(For Non-Inverting Input Driver Operation)

FUNCTIONAL BLOCK DIAGRAM

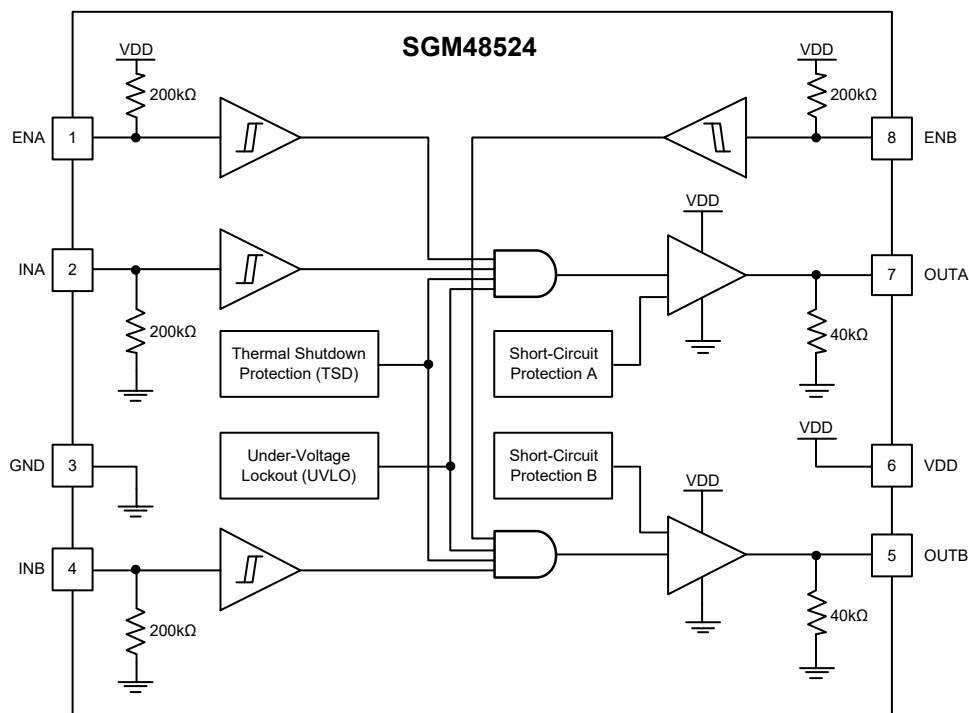


Figure 4. Functional Block Diagram

DETAILED DESCRIPTION

As a dual-channel, low-side, high-speed gate driver, the SGM48524 is among the top level devices in the market featuring 5A source/sink current capability and industry best-in-class switching characteristics. It has several other prominent features as listed in Table 1 assuring that they are reliable and efficient gate driving solutions for power switches in high frequency applications.

VDD and Under-Voltage Lockout

The internal under-voltage lockout (UVLO) protection keeps the outputs in low state when the VDD supply voltage is insufficient for proper operation of the chip. If V_{DD} is rising but its level is still below UVLO threshold, the outputs are held low, ignoring the state of the inputs. The UVLO rising threshold level is 4.15V (TYP) and has a 250mV (TYP) hysteresis band to prevent output from chattering when V_{DD} is low and prone to droops, large superimposed noise or other fluctuations.

Because VDD pin is the supply source for the device internal circuits, it is recommended to use two V_{DD} surface mount bypass capacitors to prevent noise problems due to high speed switching. A small 100nF ceramic capacitor must be soldered between the VDD

and GND pins as close as possible. In addition, a larger low ESR capacitor (at least 4.7μF) must be placed in parallel and close to the same pins for delivery of the high peak driving currents with sharp rise time. The low impedance characteristic provided by these capacitors allows high frequency and high current driving of the outputs. Avoid using vias for connecting bypass capacitors to the device pins.

Protection and Ringing Suppression

The SGM48524 is a reliable and high-speed gate driver for power switches with a comprehensive set of protection features such as thermal shutdown protection, under-voltage lockout and short-circuit protection. The outputs are forced low immediately if any of the above mentioned conditions occurs, except short-circuit protection. When short-circuit protection occurs, the outputs enter into high impedance, and the driver will be re-enabled after the protection period (13ms, TYP) expires.

The SGM48524 offers a unique output stage design. It can effectively suppress the output voltage ringing and the overshoot/undershoot on the outputs.

Table 1. Features and Benefits of the SGM48524

| Features | Benefits |
|---|--|
| Best-in-class propagation delay (18ns, TYP). | Very low delay and distortion in pulse transmission. |
| Excellent delay matching between channels (1ns, TYP). | Allow paralleling of the channel outputs for double current driving capability. It is especially useful for driving paralleled power switches. |
| Wide supply operating range (V _{DD} from 4.5V to 18V). | Design Flexibility. |
| Wide operating temperature range (-40°C to +125°C). | Wider system operating temperature range and smaller cooling system. |
| UVLO protection on VDD. | Driver outputs are actively held low in UVLO condition to ensure controlled and glitch-free driving during power-up and power-down. |
| Outputs are actively held low when inputs (INx) are floating. | This safety feature prevents unexpected gate pulses during abnormal situations such as the conditions tested in the safety certification. |
| Outputs are enabled when enable inputs (ENx) are floating. | This feature provides pin-to-pin compatibility with other similar products in those designs where pin 1 and 8 are floating. |
| Wide hysteresis CMOS/TTL compatible input and enable thresholds. | Improved noise immunity while compatible with digital logic. |
| Input/enable pin voltage levels are not restricted by V _{DD} . | Simplified system especially in the auxiliary bias supply architecture. |
| Ringing Suppression | Reduce turn-on/off overshoot/undershoot amplitude and period. |

REVISION HISTORY

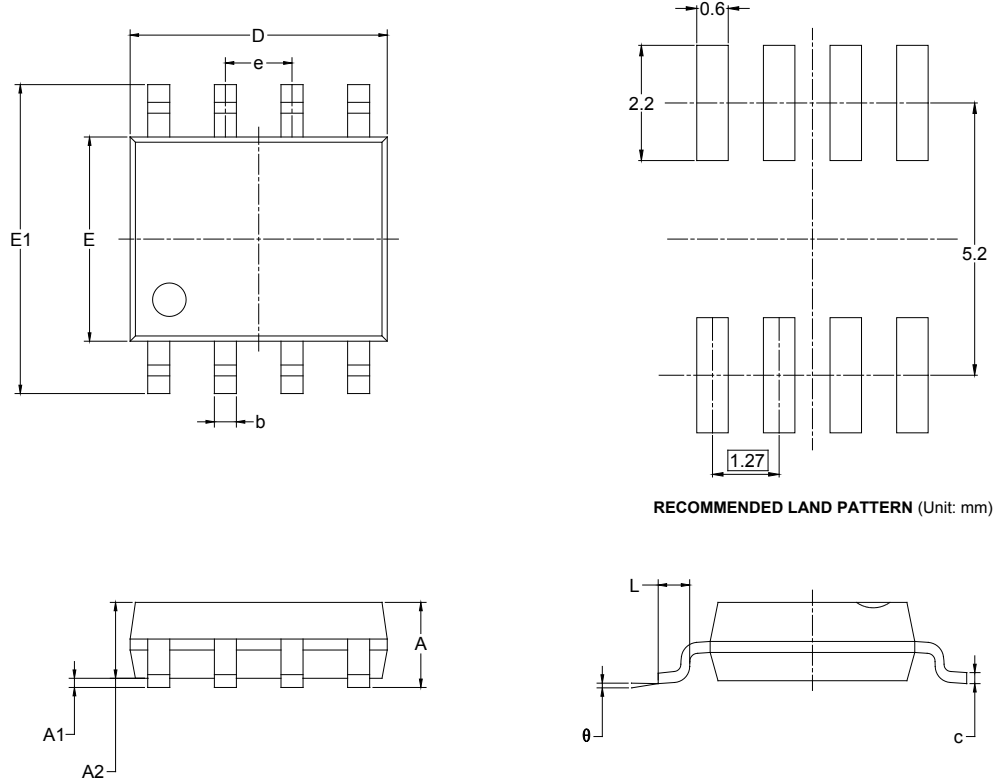
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (DECEMBER 2020) to REV.A

Changed from product preview to production data.....All

PACKAGE OUTLINE DIMENSIONS

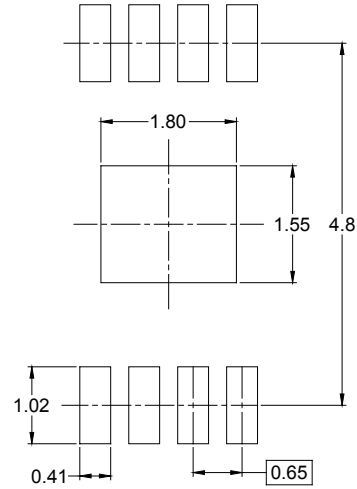
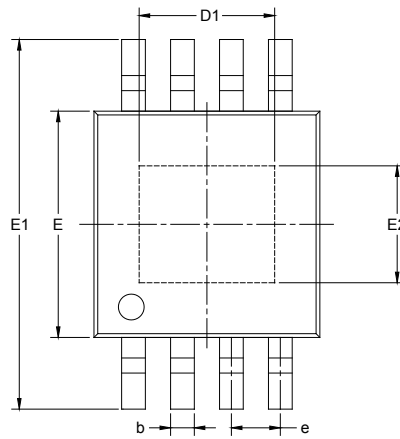
SOIC-8



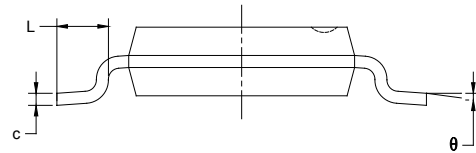
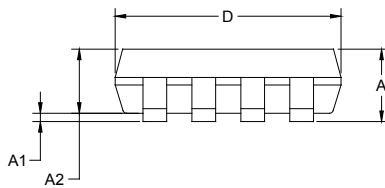
| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|------------------------------|-------|-------------------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.27 BSC | | 0.050 BSC | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

PACKAGE OUTLINE DIMENSIONS

MSOP-8 (Exposed Pad)



RECOMMENDED LAND PATTERN (Unit: mm)

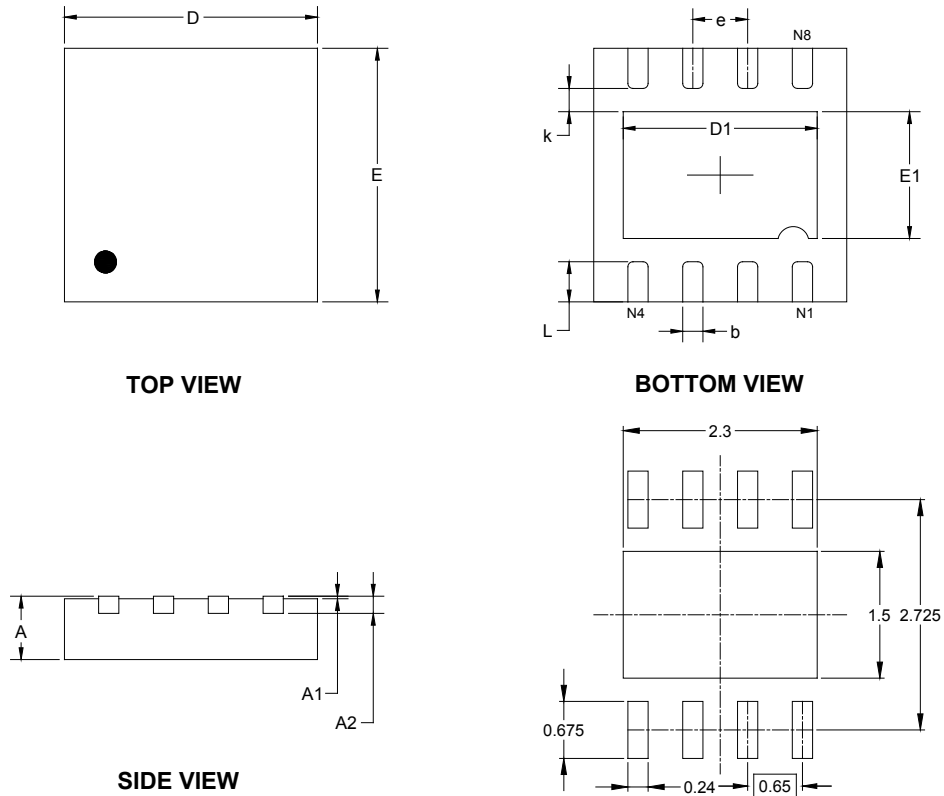


| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|------------------------------|-------|-------------------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.820 | 1.100 | 0.032 | 0.043 |
| A1 | 0.020 | 0.150 | 0.001 | 0.006 |
| A2 | 0.750 | 0.950 | 0.030 | 0.037 |
| b | 0.250 | 0.380 | 0.010 | 0.015 |
| c | 0.090 | 0.230 | 0.004 | 0.009 |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D1 | 1.700 | 1.900 | 0.067 | 0.075 |
| e | 0.65 BSC | | 0.026 BSC | |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 4.750 | 5.050 | 0.187 | 0.199 |
| E2 | 1.450 | 1.650 | 0.057 | 0.065 |
| L | 0.400 | 0.800 | 0.016 | 0.031 |
| θ | 0° | 6° | 0° | 6° |

PACKAGE INFORMATION

PACKAGE OUTLINE DIMENSIONS

TDFN-3×3-8L



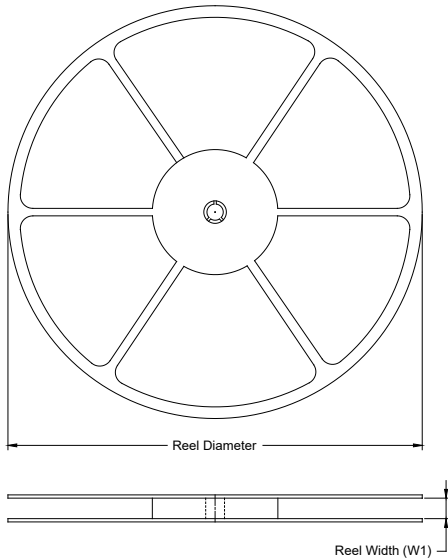
RECOMMENDED LAND PATTERN (Unit: mm)

| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|--------|------------------------------|-------|-------------------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.700 | 0.800 | 0.028 | 0.031 |
| A1 | 0.000 | 0.050 | 0.000 | 0.002 |
| A2 | 0.203 REF | | 0.008 REF | |
| D | 2.900 | 3.100 | 0.114 | 0.122 |
| D1 | 2.200 | 2.400 | 0.087 | 0.094 |
| E | 2.900 | 3.100 | 0.114 | 0.122 |
| E1 | 1.400 | 1.600 | 0.055 | 0.063 |
| k | 0.200 MIN | | 0.008 MIN | |
| b | 0.180 | 0.300 | 0.007 | 0.012 |
| e | 0.650 TYP | | 0.026 TYP | |
| L | 0.375 | 0.575 | 0.015 | 0.023 |

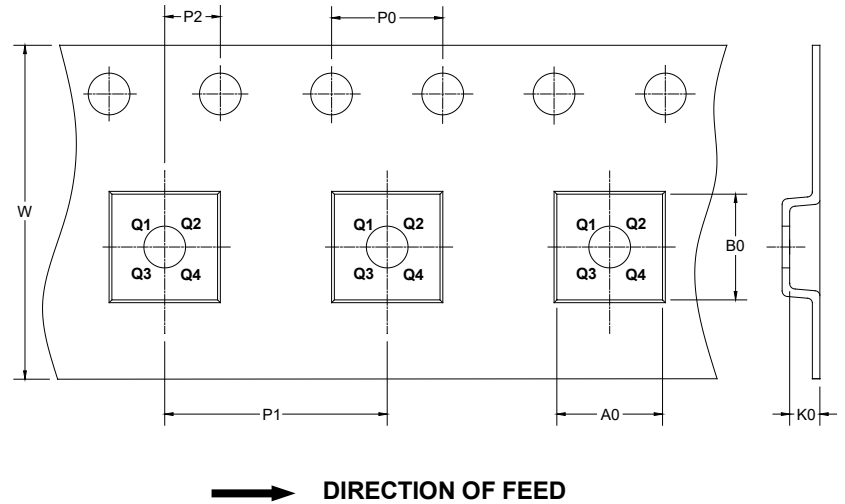
PACKAGE INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

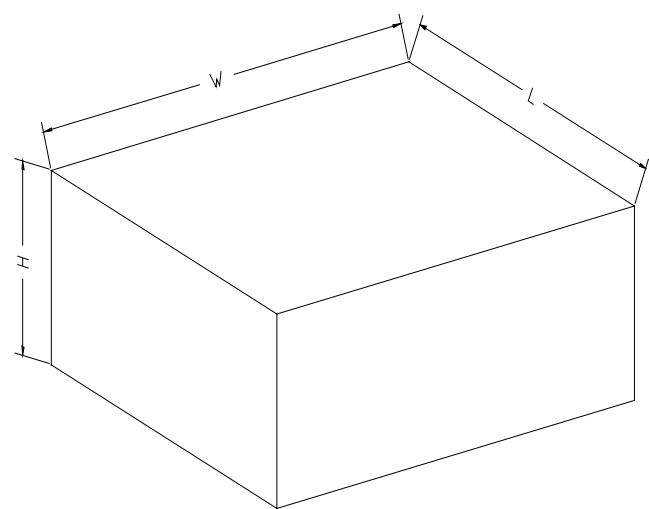
KEY PARAMETER LIST OF TAPE AND REEL

| Package Type | Reel Diameter | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P0 (mm) | P1 (mm) | P2 (mm) | W (mm) | Pin1 Quadrant |
|----------------------|---------------|--------------------|---------|---------|---------|---------|---------|---------|--------|---------------|
| SOIC-8 | 13" | 12.4 | 6.40 | 5.40 | 2.10 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |
| MSOP-8 (Exposed Pad) | 13" | 12.4 | 5.20 | 3.30 | 1.50 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |
| TDFN-3×3-8L | 13" | 12.4 | 3.35 | 3.35 | 1.13 | 4.0 | 8.0 | 2.0 | 12.0 | Q1 |

DD0001

PACKAGE INFORMATION

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

| Reel Type | Length (mm) | Width (mm) | Height (mm) | Pizza/Carton |
|-----------|-------------|------------|-------------|--------------|
| 13" | 386 | 280 | 370 | 5 |

DD0002