

精度为 1% 的 TPS6282x 5.5V、1A/2A/3A 降压转换器系列

1 特性

- DCS-Control™拓扑
- 26/25mΩ 内部电源开关 (TPS62823)
- 输出电流高达 3A (TPS62823)
- 极低的静态电流: 4μA
- 典型开关频率为 2.2MHz
- 反馈电压精度为 1% (完整温度范围)
- 使能 (EN) 和电源正常 (PG) 引脚
- 可调输出电压范围为 0.6V 至 4V
- 100% 占空比模式
- 内部软启动电路
- 无缝省电模式转换
- 欠压闭锁
- 有源输出放电
- 逐周期电流限制
- 断续短路保护
- 过热保护
- 使用 TPS62822 并借助 WEBENCH® 电源设计器创建定制设计方案

2 应用

- 便携式/电池供电类设备中的 POL 电源
- 工厂和楼宇自动化
- 移动计算、网卡
- 固态驱动器
- 数据终端、销售终端
- 服务器、投影仪、打印机

3 说明

TPS6282x 是一款通用且易于使用的同步降压型直流/直流转换器，具有仅 4μA 的极低静态电流。此系列器件具有 2.4V 至 5.5V 的输入电压，可提供高达 3A 的输出电流 (TPS62823)。此产品基于 DCS-Control™拓扑，可实现快速瞬态响应。

由于具有内部基准，此产品可在 -40°C 至 125°C 的结温范围内以高达 1% 的反馈电压精度将输出电压调节到低至 0.6V。1A/2A/3A 可扩展引脚对引脚器件系列可实现 BOM 对 BOM 兼容，并可与 470nH 的小型电感器结合使用。

TPS6282x 可在超轻负载时自动进入省电模式，并能保持高效率。

该器件具有电源正常信号和内部软启动电路。它能够以 100% 模式运行。在故障保护方面，它加入了断续电流限制以及热关断功能。

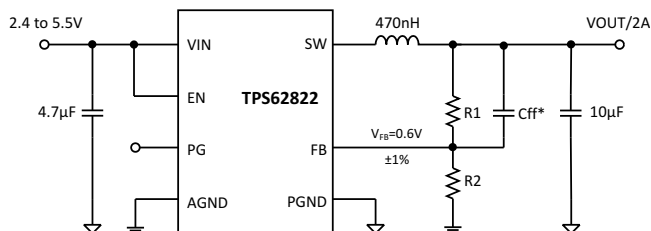
TPS6282x 采用 2 x 1.5mm QFN-8 封装。

器件信息⁽¹⁾

器件号	封装	封装尺寸 (标称值)
TPS62821DLC	QFN (8)	2.00mm x 1.50mm
TPS62822DLC		
TPS62823DLC		

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

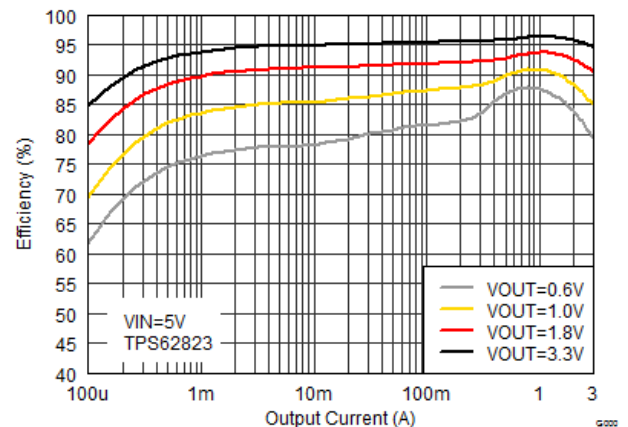
典型应用电路原理图



* optional

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效率与输出电流间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (February 2018) to Revision B	Page
• 已更改 将 TPS62822 和 TPS62823 的状态改为生产数据器件。	22

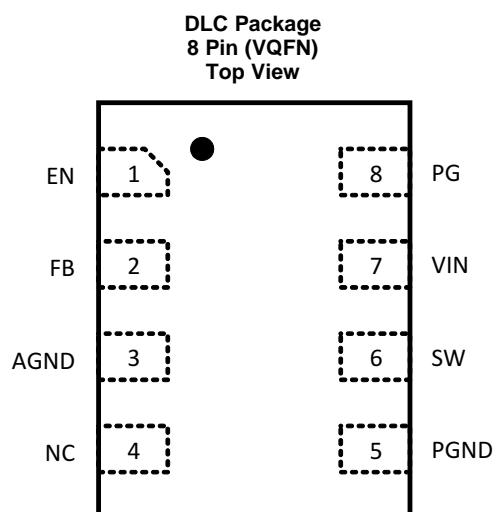
Changes from Original (November 2017) to Revision A	Page
• 已更改 将 TPS62821 的状态改为生产数据器件。	22

5 Device Comparison Table

Part Number	Output Current	Output Voltage ⁽¹⁾
TPS62821DLC	1 A	Adjustable
TPS62822DLC	2 A	Adjustable
TPS62823DLC	3 A	Adjustable

(1) For fixed output voltage versions please contact your TI sales representative.

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable input (High=Enabled, Low=Disabled). Do not leave floating.
FB	2	I	Output voltage feedback. Connect resistive voltage divider to this pin.
AGND	3		Signal ground. Internally connected to the PGND pin. Can be left floating.
NC	4		Internally not connected. Can be connected to VOUT, GND or left floating.
PGND	5	Power	Power ground
SW	6	Power	Switch node, connected to the internal MOSFET switches.
VIN	7	Power	Supply voltage
PG	8	O	Power good output. If unused, leave floating or connect to GND.

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

		MIN	MAX	UNIT
Pin Voltage Range	VIN, FB, EN, PG, NC	-0.3	6	V
	SW (DC)	-0.3	VIN + 0.3	
	SW (DC, in current limit)	-1.0		
	SW (AC), less than 10ns ⁽²⁾	-2.5		
Power Good Sink Current			1	mA
Operating Junction Temperature Range, TJ		-40	150	°C
Storage temperature, Tstg		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) While switching.

7.2 ESD Ratings

		VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply Voltage Range, V _{IN}		2.4		5.5	V
Output Voltage Range, V _{OUT}		0.6		4	V
Maximum Output Current, I _{OUT}	TPS62821			1	A
	TPS62822			2	
	TPS62823			3	
Operating Junction Temperature, T _J		-40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS6282x		UNIT
		DLC (VQFN) 8 PINS		
		JEDEC PCB	TPS6282xEVM-005	
R _{θJA}	Junction-to-ambient thermal resistance	114.1	69.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	90.2	n/a ⁽²⁾	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.4	n/a ⁽²⁾	°C/W
ψ _{JT}	Junction-to-top characterization parameter	6.6	4.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	43.7	44.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Not applicable to an EVM.

7.5 Electrical Characteristics

over operating junction temperature range ($T_J = -40^{\circ}\text{C}$ to 125°C) and $V_{IN} = 2.4\text{V}$ to 5.5V . Typical values at $V_{IN} = 5\text{V}$ and $T_J = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V _{IN}	Input Voltage range		2.4		5.5	V
I _Q	Operating Quiescent Current	EN=High, I _{OUT} =0A, device not switching		4	10	μA
I _{SD}	Shutdown Current	EN=Low, T _J = -40°C to 85°C		0.05	0.5	μA
V _{UVLO}	Undervoltage Threshold	Falling Input Voltage	2.1	2.2	2.3	V
	Undervoltage Hysteresis			160		mV
T _{SD}	Thermal Shutdown Threshold	Rising Junction Temperature		150		°C
	Thermal Shutdown Hysteresis			20		
CONTROL (EN, PG)						
V _H	High-Level Threshold Voltage (EN)		1.0			V
V _L	Low-Level Threshold Voltage (EN)				0.4	V
I _{LKG}	Input Leakage Current (EN, PG)	EN = High, V _{PG} = 5V		10	100	nA
t _{SS}	Soft-Start Time	Time from EN=High to 95% of V _{OUT} nominal		1.25		ms
V _{PGTL}	Power Good Lower Threshold Voltage	Rising (V _{FB} vs regulation target)	94%	96%	98%	
		Falling (V _{FB} vs regulation target)	90%	92%	94%	
V _{PGTH}	Power Good Upper Threshold Voltage	Rising (V _{FB} vs regulation target)	108%	110%	112%	
		Falling (V _{FB} vs regulation target)	103%	105%	107%	
V _{PGL}	Power Good Logic Low Level Output Voltage	I _{PG} = -1mA			0.4	V
t _{PGD}	Power Good delay	rising		100		μs
		falling		20		
POWER SWITCH						
F _{SW}	Switching Frequency	PWM Mode Operation		2.2		MHz
R _{DS(on)}	High-Side FET ON-Resistance	TPS62821		35		mΩ
		TPS62822		35		
		TPS62823		26		
	Low-Side FET ON-Resistance	TPS62821,2,3		25		
I _{LIM}	High-Side FET Current Limit	TPS62821	1.7	2.1	2.4	A
		TPS62822	2.7	3.3	3.7	
		TPS62823	3.7	4.3	5.0	
OUTPUT						
I _{LKG_FB}	Input Leakage Current (FB)	EN=High, V _{FB} =0.6V		10	50	nA
V _{FB}	Feedback Voltage Accuracy	PWM Mode	594	600	606	mV
I _{DIS}	Output Discharge Current	EN=Low, V _{SW} = 0.4V	75	400		mA
	DC Load Regulation	PWM Mode Operation		0.2		%/A
	DC Line Regulation	PWM Mode Operation		0.05		%/V

.0

7.6 Typical Characteristics

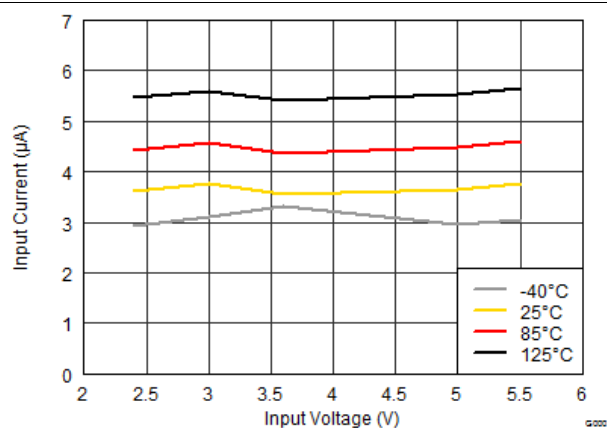


图 1. Quiescent Current

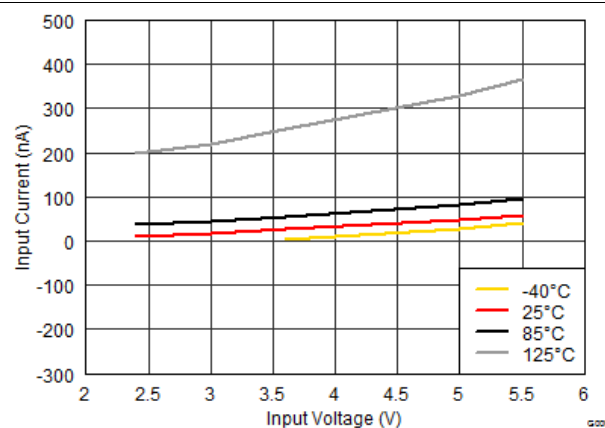


图 2. Shutdown Current

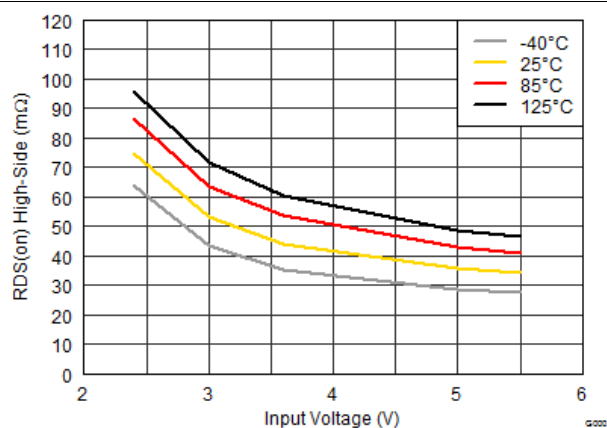


图 3. High-Side Switch Resistance (TPS62821/2)

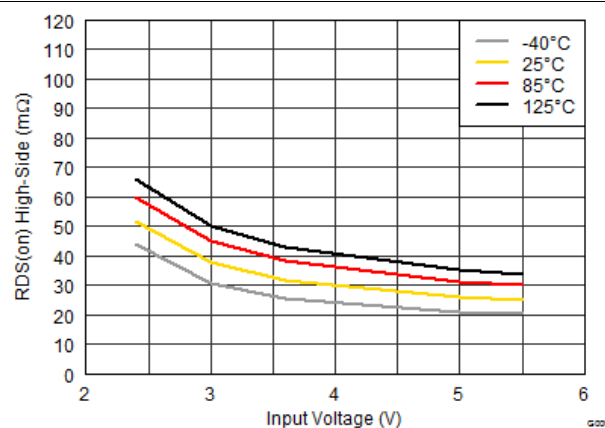


图 4. High-Side Switch Resistance (TPS62823)

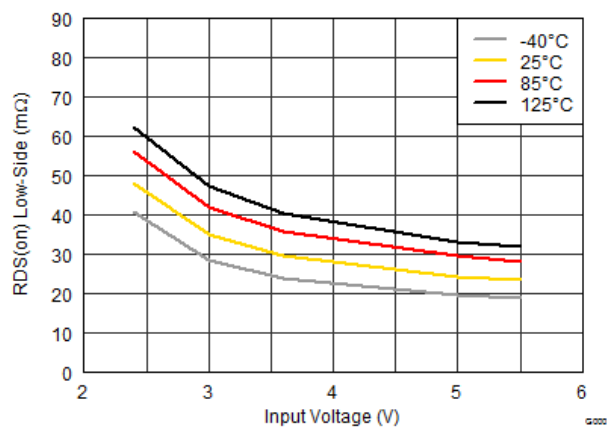


图 5. Low-Side Switch Resistance (TPS62821/2/3)

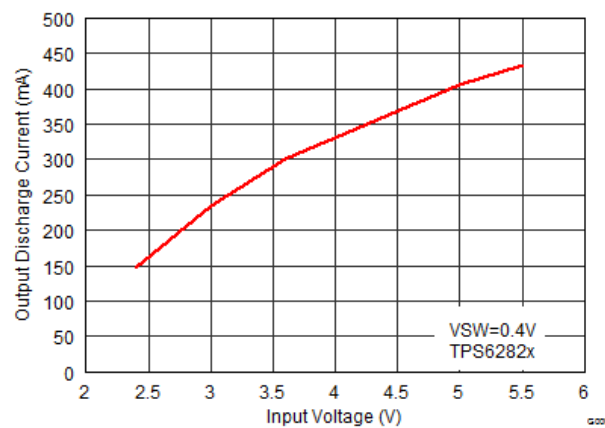


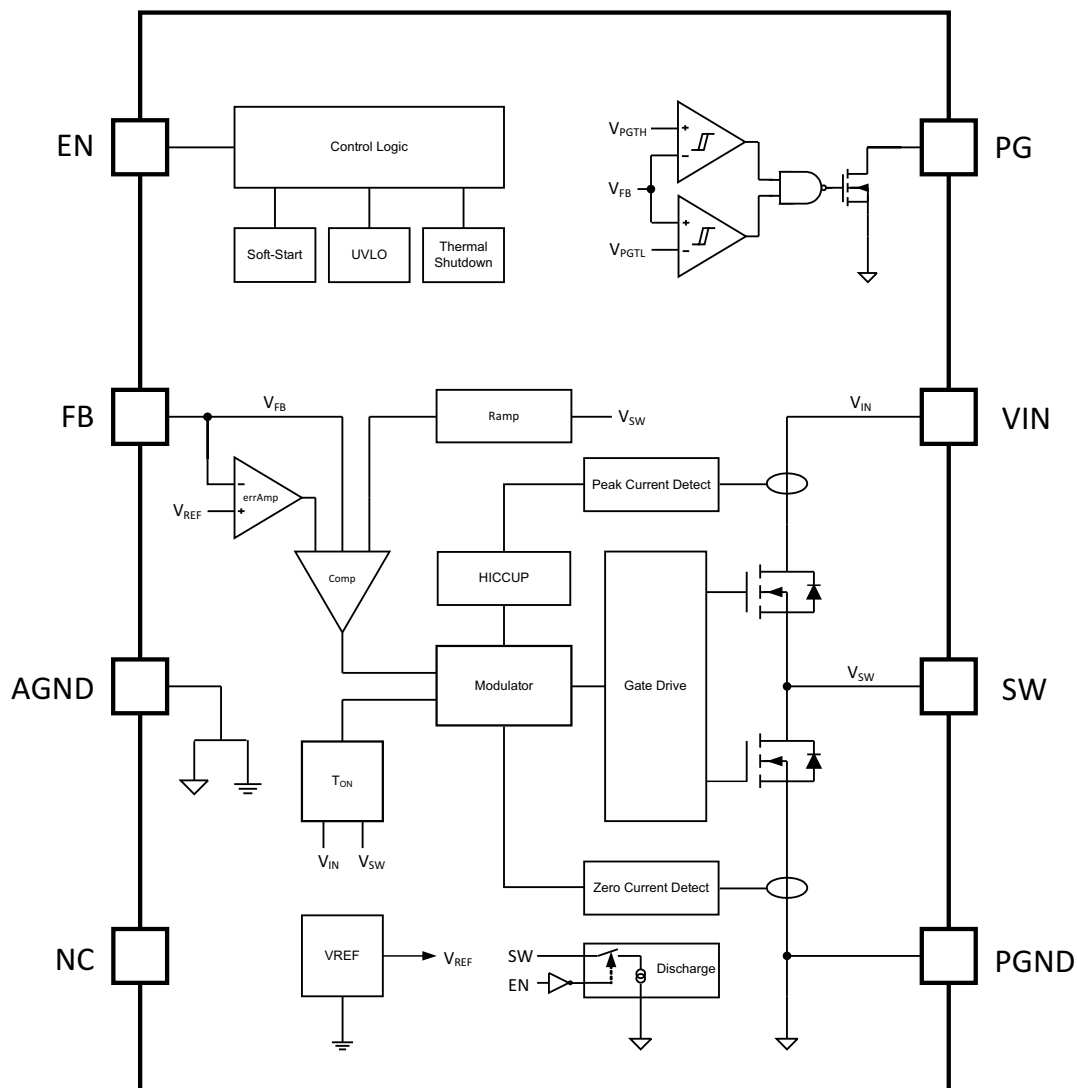
图 6. Active Output Discharge Current (EN=Low)

8 Detailed Description

8.1 Overview

The TPS6282x are synchronous step-down converters based on the DCS-Control™ topology with an adaptive constant on-time control and a stabilized switching frequency. It operates in PWM (pulse width modulation) mode for medium to heavy loads and in PSM (power save mode) at light load conditions, keeping the output voltage ripple small. The nominal switching frequency is about 2.2MHz with a small and controlled variation over the input voltage range. As the load current decreases, the converter enters PSM, reducing the switching frequency to keep efficiency high over the entire load current range. Since combining both PWM and PSM within a single building block, the transition between modes is seamless and without effect on the output voltage. The devices offer both excellent dc voltage and fast load transient regulation, combined with a very low output voltage ripple.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Enable / Shutdown and Output Discharge

The device starts operation, when Enable (EN) is set High. The input threshold levels are typically 0.9V for rising and 0.7V for falling signals. Do not leave EN floating. Shutdown is forced if EN is pulled Low with a shutdown current of typically 50nA. During shutdown, the internal power MOSFETs as well as the entire control circuitry are turned off and the output voltage is actively discharged through the SW pin by a current sink. Therefore, V_{IN} must remain present for the discharge to function.

8.3.2 Soft-Start

About 250 μ s after EN goes High, the internal soft-start circuitry controls the output voltage during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time of about 1ms. It also prevents unwanted voltage drops from high-impedance power sources or batteries. TPS6282x can start into a pre-biased output.

8.3.3 Power Good (PG)

The TPS6282x has a built in power good (PG) function. The PG pin goes high impedance, when the output voltage has reached its nominal value. Otherwise, including when disabled, in UVLO or in thermal shutdown, PG is Low (see [表 1](#)). The PG function is formed with a window comparator, which has an upper and lower voltage threshold (see [Electrical Characteristics](#)). The PG pin is an open drain output that requires a pull-up resistor and can sink up to 1mA. If not used, the PG pin can be left floating or connected to GND.

表 1. Power Good Pin Logic

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	$V_{FB} \geq V_{PGTL}$ and $V_{FB} \leq V_{PGTH}$	√	
	$V_{FB} \leq V_{PGTL}$ or $V_{FB} \geq V_{PGTH}$		√
Shutdown (EN=Low)			√
UVLO	$0.7\text{ V} < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 0.7\text{ V}$	√	

At startup, PG transitions from low to floating about 100 μ s after the output voltage has reached regulation. Once in operation, PG has a deglitch delay of about 20 μ s before going low. When the output voltage returns to regulation, the same 100 μ s delay occurs.

8.3.4 Undervoltage Lockout (UVLO)

The undervoltage lockout (UVLO) function prevents misoperation of the device, if the input voltage drops below the UVLO threshold. It is set to about 2.2V with a hysteresis of typically 160mV.

8.3.5 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 150°C (typ.), the device goes in thermal shutdown with a hysteresis of typically 20°C. Once the T_J has decreased enough, the device resumes normal operation.

8.4 Device Functional Modes

8.4.1 Pulse Width Modulation (PWM) Operation

At load currents larger than half the inductor ripple current, the device operates in pulse width modulation in continuous conduction mode (CCM).

The PWM operation is based on an adaptive constant on-time control with stabilized switching frequency. To achieve a stable switching frequency in a steady state condition, the on-time is calculated as:

Device Functional Modes (接下页)

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \cdot 450ns \quad (1)$$

With that, the typical switching frequency is about 2.2MHz.

8.4.2 Power Save Mode (PSM) Operation

To maintain high efficiency at light loads, the device enters power save mode (PSM) at the boundary to discontinuous conduction mode (DCM). This happens when the output current becomes smaller than half of the inductor's ripple current. The device operates now with a fixed on-time and the switching frequency further decreases proportional to the load current. It can be calculated as:

$$f_{PSM} = \frac{2 \cdot I_{OUT}}{T_{ON}^2 \cdot \frac{V_{IN}}{V_{OUT}} \left[\frac{V_{IN} - V_{OUT}}{L} \right]} \quad (2)$$

In PSM, the output voltage rises slightly above the nominal target, which can be minimized using larger output capacitance. At duty cycles larger than 90%, the device may not enter PSM. The device maintains output regulation in PWM mode.

8.4.3 Minimum Duty Cycle and 100% Mode Operation

There is no limitation for small duty cycles, since even at very low duty cycles the switching frequency is reduced as needed to always ensure a proper regulation.

If the output voltage level comes close to the input voltage, the device enters 100% mode. While the high-side switch is constantly turned on, the low-side switch is switched off. The difference between V_{IN} and V_{OUT} is determined by the voltage drop across the high-side FET and the dc resistance of the inductor. The minimum V_{IN} that is needed to maintain a specific V_{OUT} value is estimated as:

$$V_{IN(min)} = V_{OUT} + I_{OUT} (R_{DS(on)} + R_{DC(L)}) \quad (3)$$

8.4.4 Current Limit and Short Circuit Protection

The peak switch current of TPS6282x is internally limited, cycle by cycle, to a maximum dc value as specified in [Electrical Characteristics](#). This prevents the device from drawing excessive current in case of externally caused over current or short circuit condition. Due to an internal propagation delay of about 60ns, the actual ac peak current can exceed the static current limit during that time.

If the current limit threshold is reached, the device delivers its maximum output current. Detecting this condition for 32 switching cycles (about 13μs), the device turns off the high-side MOSFET for about 100μs which allows the inductor current to decrease through the low-side MOSFET's body diode and then restarts again with a soft start cycle. As long as the overload condition is present, the device hiccups that way, limiting the output power.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6282x is a switched mode step-down converter, able to convert a 2.4-V to 5.5-V input voltage into a lower 0.6-V to 4-V output voltage, providing up to 3A continuous output current (TPS62823). It needs a very low amount of external components. Apart from the inductor and the output and input capacitors, additional parts are only needed to set the output voltage and to enable the Power Good (PG) feature.

9.2 Typical Application

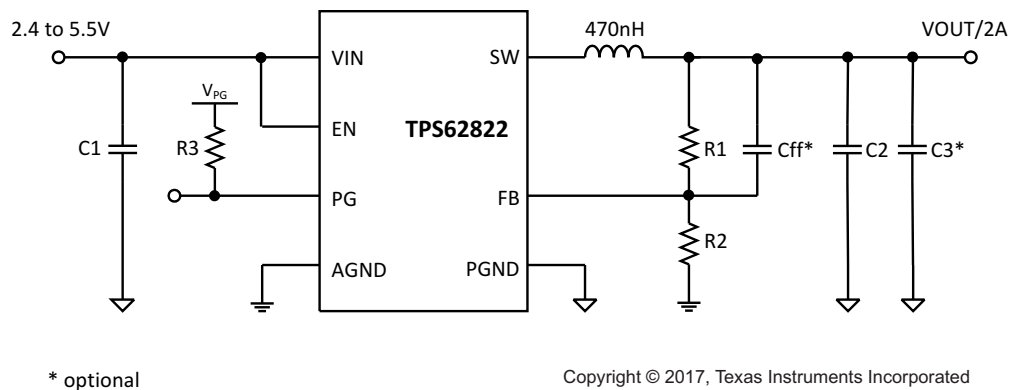


图 7. A typical 2.4 to 5.5-V, 2-A Power Supply

9.2.1 Design Requirements

The following design guideline provides a range for the component selection to operate within the recommended operating conditions. 表 2 shows the components selection that was used for the measurements shown in the [Application Curves](#).

表 2. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
IC	5.5-V, step-down converter	TPS6282xDLC, Texas Instruments
L1	470 nH $\pm 20\%$, 7.6m Ω DCR, 6.6A I_{SAT}	XFL4015-471MEB, Coilcraft
C1	4.7 μ F $\pm 20\%$, 6.3V, ceramic, 0603, X7R	JMK107BB7475MA-T, Taiyo Yuden
C2, C3	10 μ F $\pm 20\%$, 10V, ceramic, 0603, X7R	GRM188Z71A106MA73D, MuRata
Cff	120pF $\pm 5\%$, 50V, 0603	GRM1885C1H121JA01D, MuRata
R1, R2	Depending on VOUT, chip, 0603	Standard
R3	100-k Ω , chip, 0603, 0.1W, 1%	Standard

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click [here](#) to create a custom design using the TPS62822 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Setting the Adjustable Output Voltage

While the device regulates the feedback voltage to 0.6V, the output voltage is specified from 0.6 to 4V. A resistive divider (from VOUT to FB to AGND) sets the actual output voltage of the TPS6282x. [公式 4](#) and [公式 5](#) calculate the values of the resistors. I_{FB} is recommended to be in the range of 5μA, but can differ if needed.

$$R_2 = \frac{0.6V}{I_{FB}} \quad (4)$$

$$R_1 = \frac{V_{OUT}}{I_{FB}} - R_2 \quad (5)$$

[表 3](#) shows standard resistor values for typical output voltages.

表 3. Feedback Resistor Values for Typical Output Voltages

VOUT (V)	R1 (kΩ)	R2 (kΩ)
1.0	100	150
1.2	100	100
1.8	200	100
2.5	475	150
3.3	732	162

9.2.2.3 Output Filter Selection

The TPS6282x is internally compensated and optimized for a range of output filter component values, which is specified in [表 4](#). Using these values simplifies the output filter component selection. Checked cells represent combinations that are proven for stability by simulation and lab test. Further combinations are possible, but should be checked for each individual application.

表 4. Recommended LC Output Filter Combinations⁽¹⁾

	4.7 μ F	10 μ F	22 μ F	47 μ F	100 μ F	150 μ F
0.33 μ H						
0.47 μ H		✓	✓ ⁽²⁾	✓	✓ ⁽³⁾	
1.0 μ H		✓	✓	✓ ⁽³⁾	✓ ⁽³⁾	
1.5 μ H						

(1) The values in the table are the nominal values of inductors and ceramic capacitors. The effective capacitance can vary depending on package size, voltage rating and dielectric material (typical variations are from +20% to -50%).

(2) This combination is recommended as the standard value for most of all applications.

(3) C_{ff} is recommended for large C_{OUT} values.

9.2.2.4 Inductor Selection

The TPS6282x is designed to work with inductors of 470nH nominal and can be used with 1 μ H inductors as well. The inductor has to be selected for adequate saturation current and a low dc resistance (DCR). The minimum inductor current rating, that is needed under static load conditions is calculated using 公式 6 and 公式 7.

$$I_{peak(max)} = I_{L(min)} = I_{OUT(max)} + \frac{\Delta I_{L(max)}}{2} \quad (6)$$

$$\Delta I_{L(max)} = V_{OUT} \left(\frac{1 - \frac{V_{OUT}}{V_{IN}}}{L_{(min)} \cdot f_{SW}} \right) \quad (7)$$

This calculation gives the minimum saturation current of the inductor needed and an additional margin is recommended to cover dynamic overshoot due to startup or load transients. Inductors are available in different dimensions. Choosing the smallest size might result in less efficiency due to larger DCR and ac losses. The following inductors have been tested with the TPS6282x:

表 5. List of Recommended Inductors

TYPE	Nominal INDUCTANCE ⁽¹⁾	Saturation Current and DC Resistance		Dimensions [mm]	Manufacturer ⁽²⁾
		max. I_{SAT} [A] ⁽³⁾	max. R_{DC} [m Ω]		
HTEN20161T-R47MDR	0.47	4.8	32	2.0 x 1.6 x 1.0	Cyntec
HTEH20121T-R47MSR	0.47	4.6	25	2.0 x 1.2 x 1.0	Cyntec
DFE201610E - R47M	0.47	4.8	32	2.0 x 1.6 x 1.0	muRata
DFE201210S - R47M	0.47	4.8	32	2.0 x 1.2 x 1.0	muRata
TFM201610ALM-R47MTAA	0.47	5.1	34	2.0 x 1.6 x 1.0	TDK
TFM201610ALC-R47MTAA	0.47	5.2	25	2.0 x 1.6 x 1.0	TDK
XFL4015-471ME	0.47	6.6	8.36	4.0 x 4.0 x 1.6	Coilcraft

(1) Inductance Tolerance $\pm 20\%$

(2) See [Third-party Products](#) disclaimer.

(3) $\Delta L/L \approx 30\%$

9.2.2.5 Output Capacitor Selection

The output voltage range of TPS6282x is 0.6V to 4V. While stability is a first criteria for the output filter selection (L and C_{OUT}), the output capacitor value also determines transient response behavior and ripple of V_{OUT}. The recommended typical value for the output capacitor is 2x10μF (or 1x 22μF) and can be small ceramic capacitors with low equivalent series resistance (ESR). For lower V_{OUT} (V_{OUT} ≤ 2V) and where only moderate load transients are present, 10μF can be sufficient. In either case a minimum effective output capacitance of 5μF should be present.

To keep low resistance and to get a narrow capacitance variation with temperature, it is recommended to use X7R or X5R dielectric. Using an even higher value has advantages like smaller voltage ripple and tighter output voltage accuracy in PSM.

9.2.2.6 Input Capacitor Selection

For typical application, an input capacitor of 4.7μF is sufficient and recommended. A larger value reduces input current ripple further. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A low ESR ceramic capacitor is recommended for best filtering and should be placed between VIN and PGND as close as possible to those pins. In either case a minimum effective input capacitance of 3μF should be present.

9.2.2.7 Feed-forward Capacitor Selection

To improve regulation speed, TPS6282x preferably operates with a feed-forward capacitor, connected between V_{OUT} and FB. The appropriate value is calculated using 公式 8.

$$C_{ff} = \frac{12\mu s}{R_2} \quad (8)$$

Therewith, for typical values of feedback resistors (R₂=100kΩ), the feed-forward capacitance is 120pF.

图 44 and 图 45 show the results of a frequency domain analysis for both use cases, with and without a feed-forward capacitor. The larger unity gain frequency, caused by the feed forward capacitor, results in a significant improvement of the transient response.

9.2.3 Application Curves

$V_{IN}=5V$, $V_{OUT}=1.8V$, $T_A=25^{\circ}C$, BOM = 表 2, (unless otherwise noted)

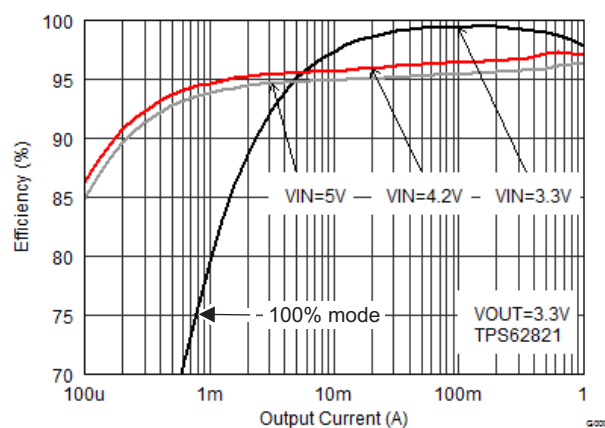


图 8. Efficiency TPS62821 at VOUT=3.3V

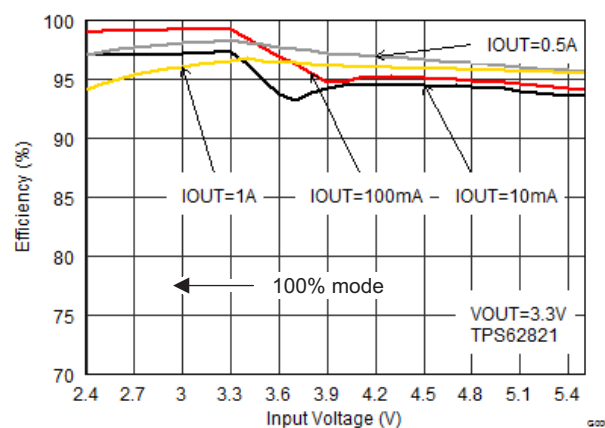


图 9. Efficiency TPS62821 at VOUT=3.3V

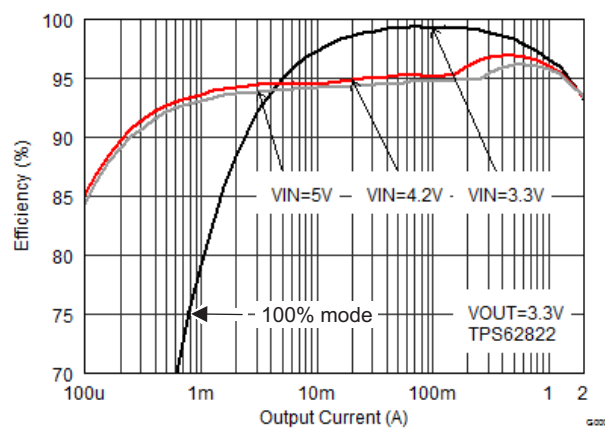


图 10. Efficiency TPS62822 at VOUT=3.3V

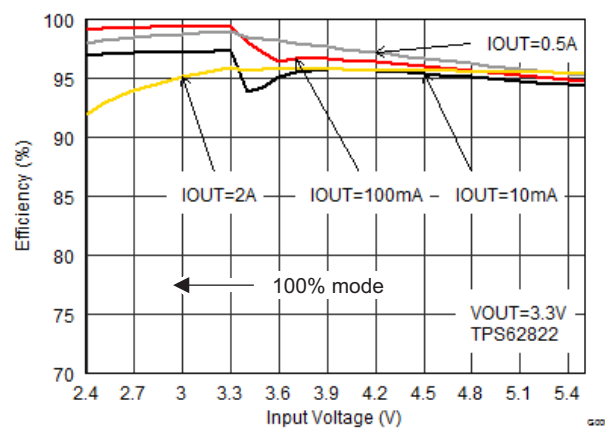


图 11. Efficiency TPS62822 at VOUT=3.3V

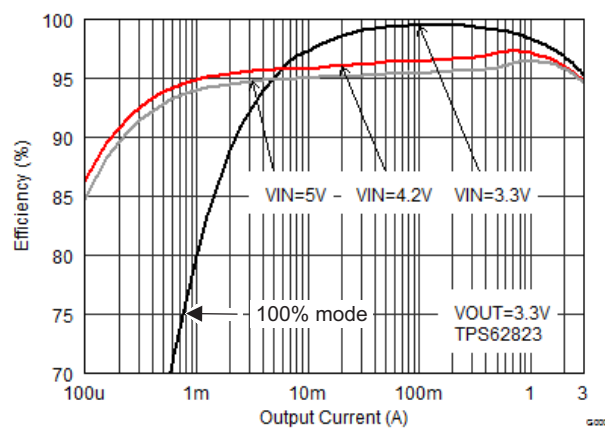


图 12. Efficiency TPS62823 at VOUT=3.3V

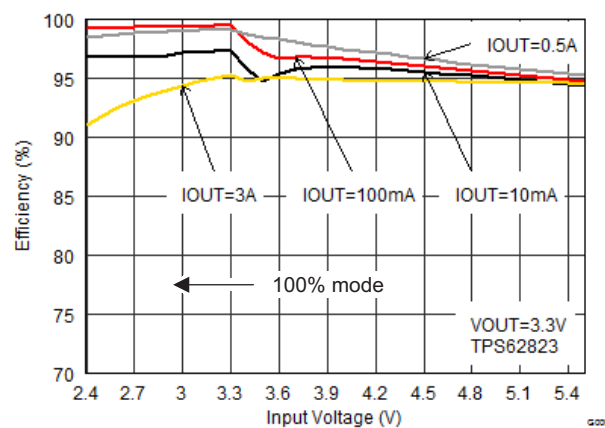


图 13. Efficiency TPS62823 at VOUT=3.3V

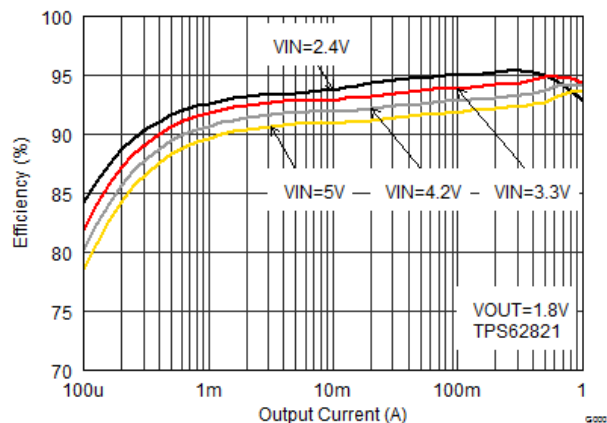


图 14. Efficiency TPS62821 at VOUT=1.8V

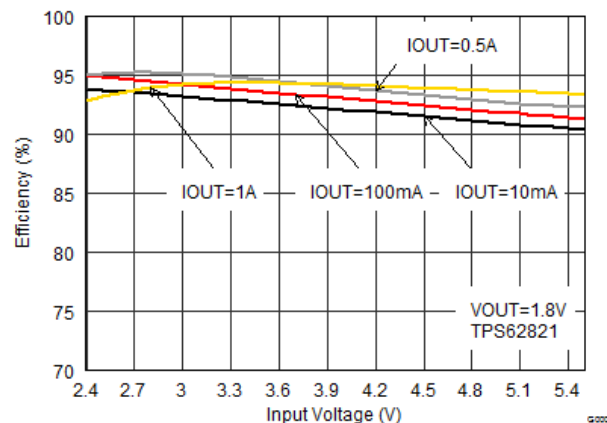


图 15. Efficiency TPS62821 at VOUT=1.8V

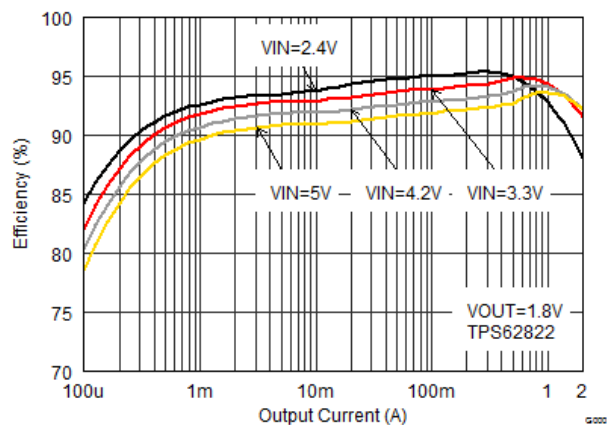


图 16. Efficiency TPS62822 at VOUT=1.8V

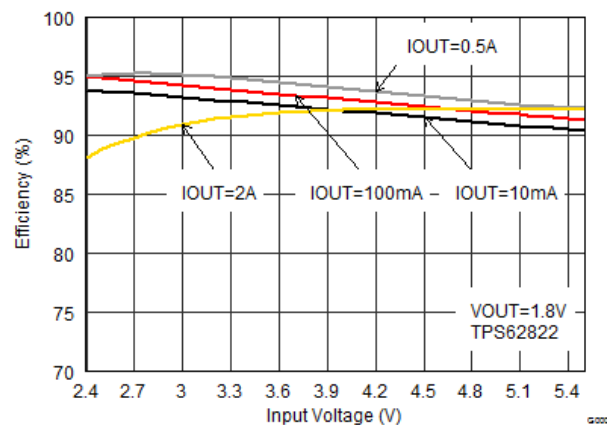


图 17. Efficiency TPS62822 at VOUT=1.8V

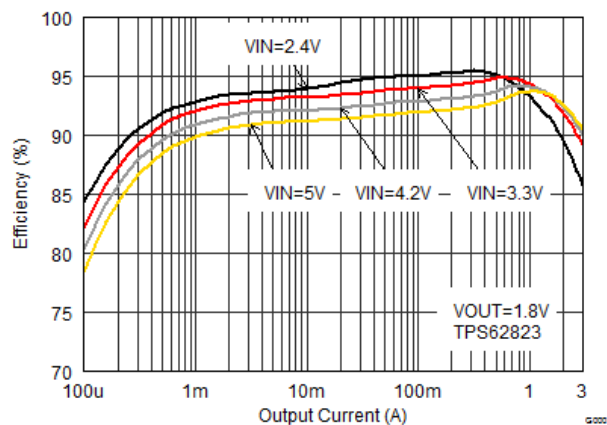


图 18. Efficiency TPS62823 at VOUT=1.8V

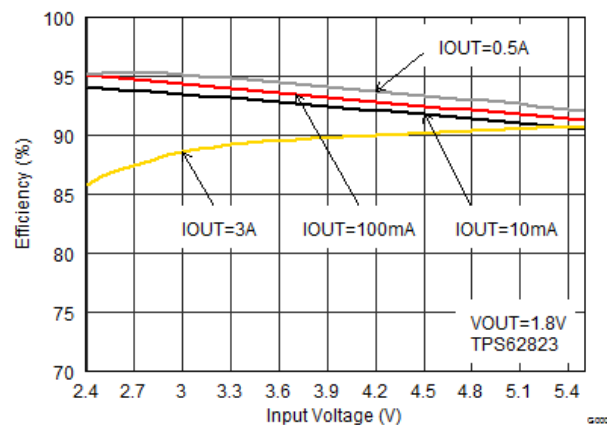


图 19. Efficiency TPS62823 at VOUT=1.8V

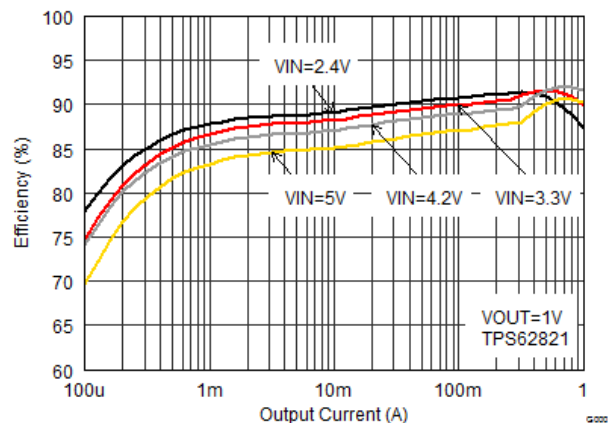


图 20. Efficiency TPS62821 at VOUT=1V

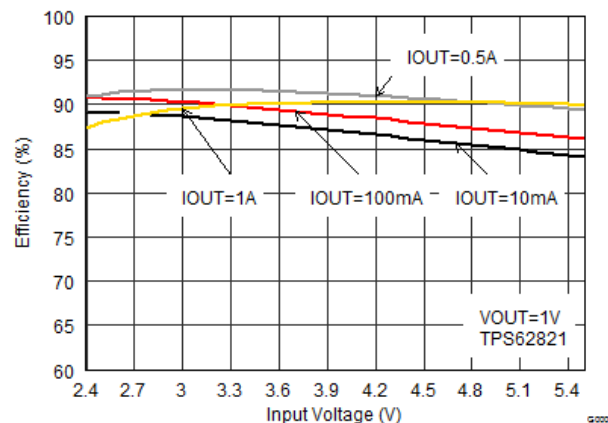


图 21. Efficiency TPS62821 at VOUT=1V

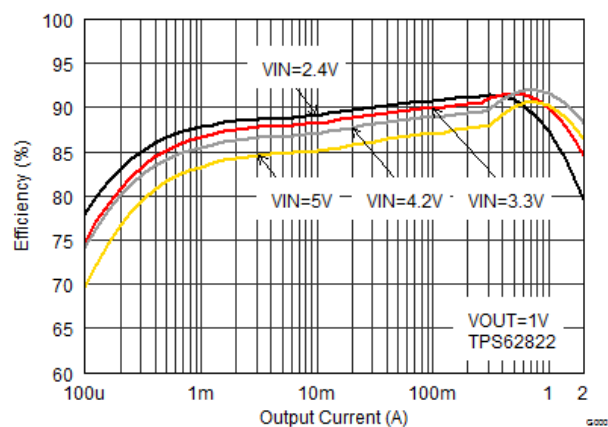


图 22. Efficiency TPS62822 at VOUT=1V

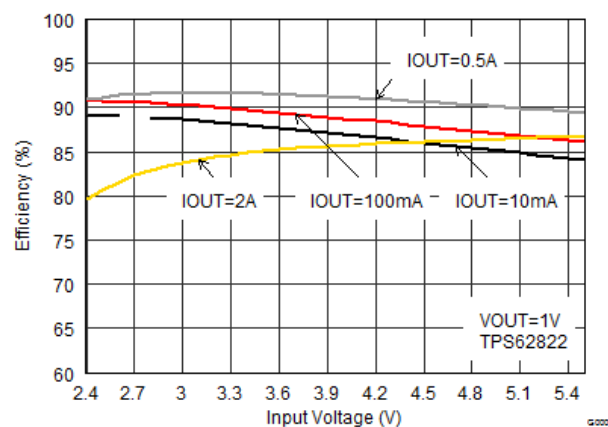


图 23. Efficiency TPS62822 at VOUT=1V

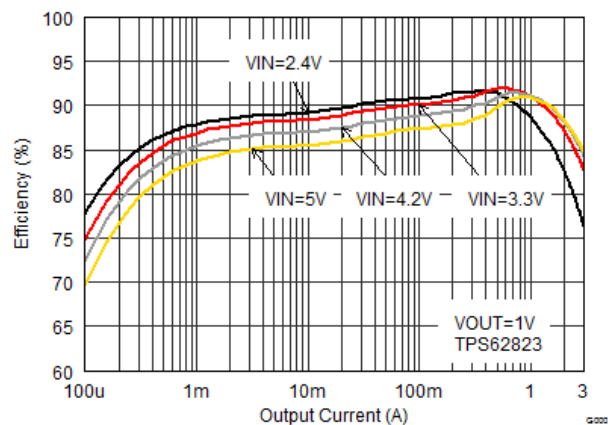


图 24. Efficiency TPS62823 at VOUT=1V

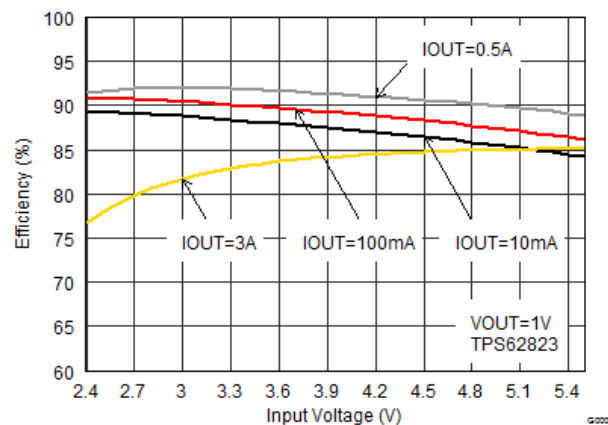


图 25. Efficiency TPS62823 at VOUT=1V

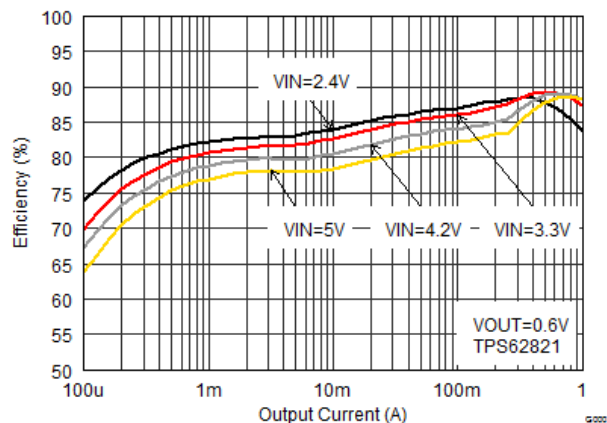


图 26. Efficiency TPS62821 at VOUT=0.6V

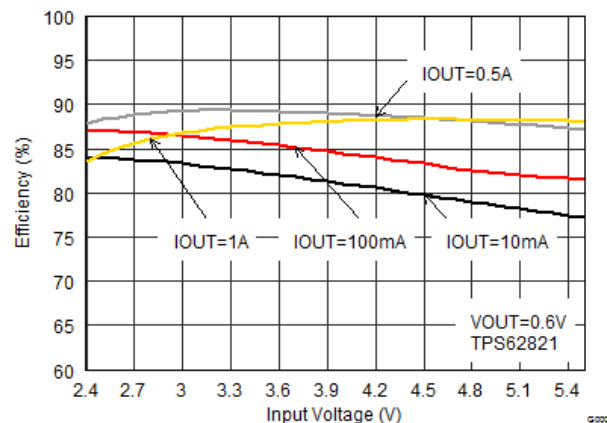


图 27. Efficiency TPS62821 at VOUT=0.6V

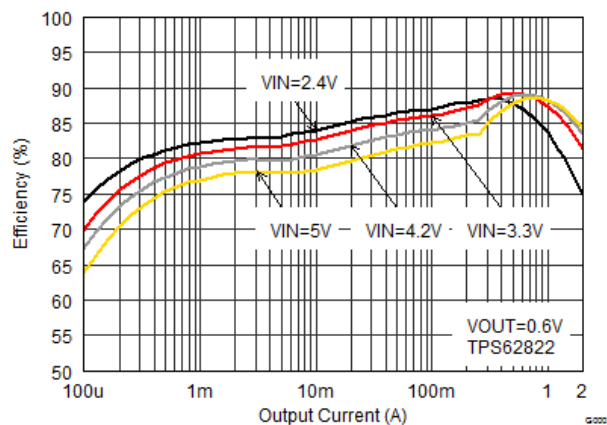


图 28. Efficiency TPS62822 at VOUT=0.6V

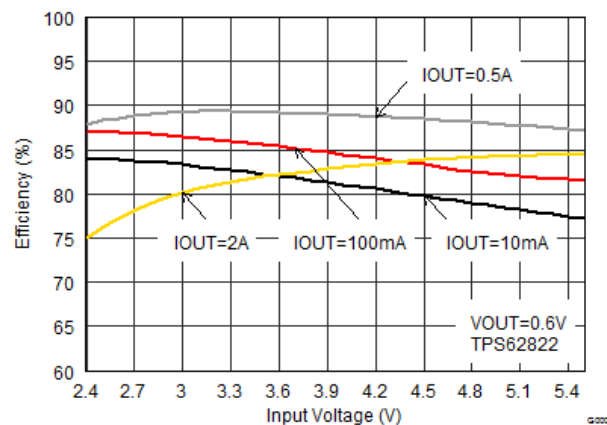


图 29. Efficiency TPS62822 at VOUT=0.6V

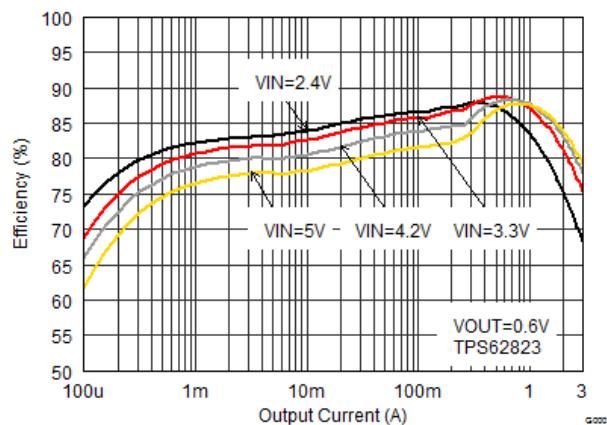


图 30. Efficiency TPS62823 at VOUT=0.6V

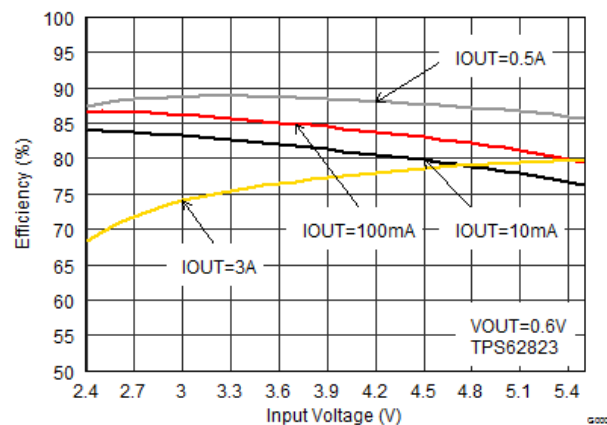


图 31. Efficiency TPS62823 at VOUT=0.6V

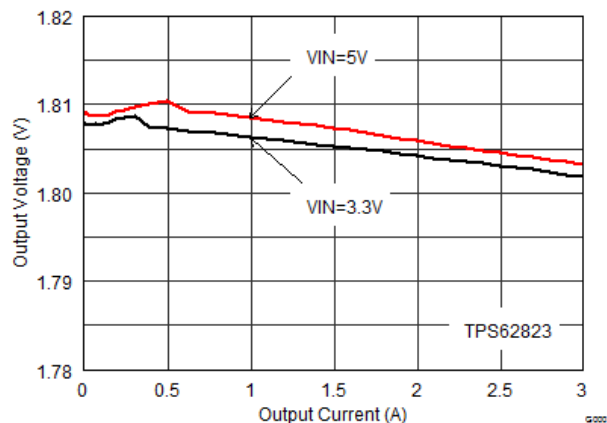


图 32. Output Voltage Accuracy (Load Regulation)

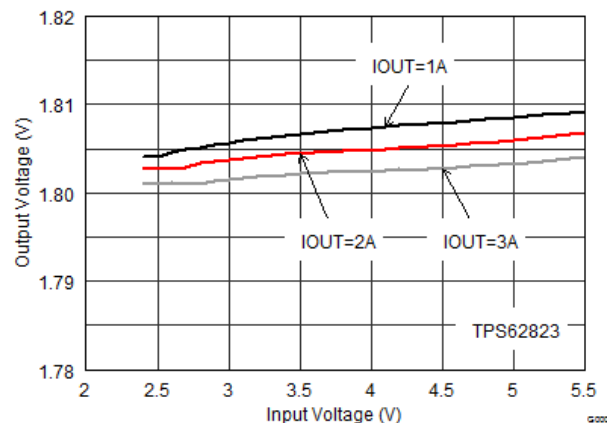


图 33. Output Voltage Accuracy (Line Regulation)

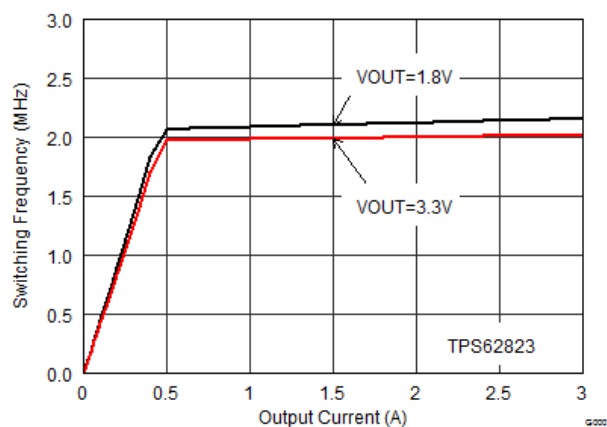


图 34. Switching Frequency vs Output Current

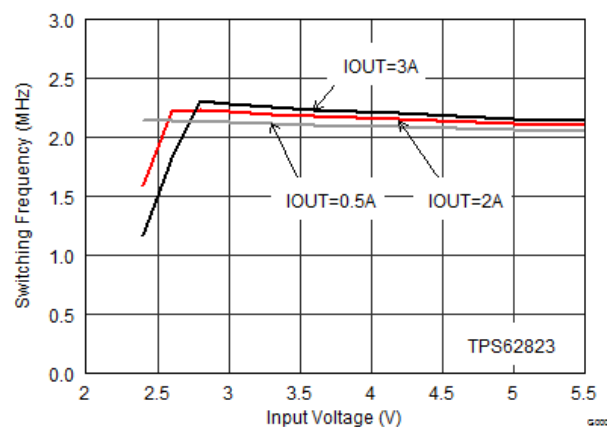


图 35. Switching Frequency vs Input Voltage

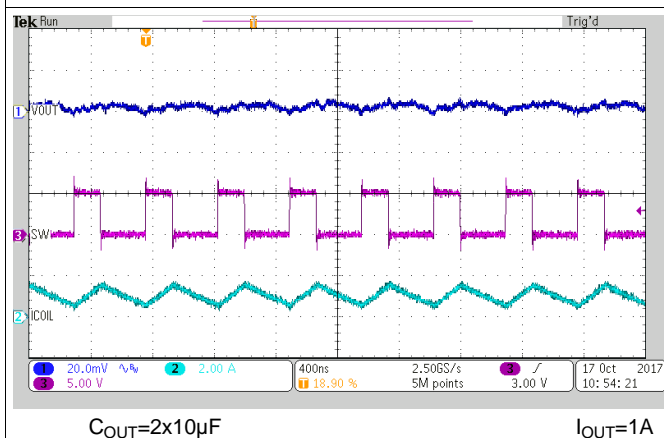


图 36. Typical Operation PWM

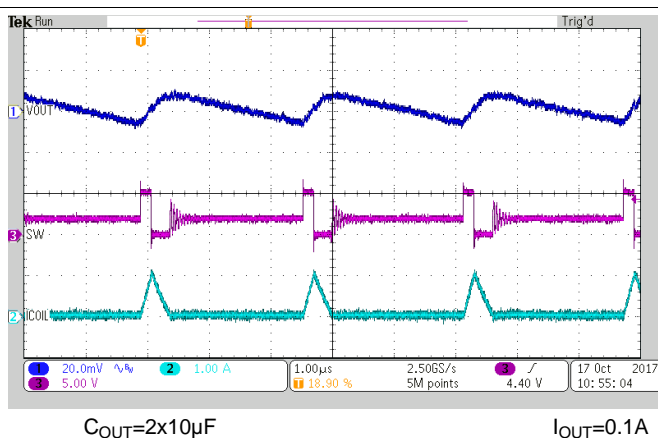
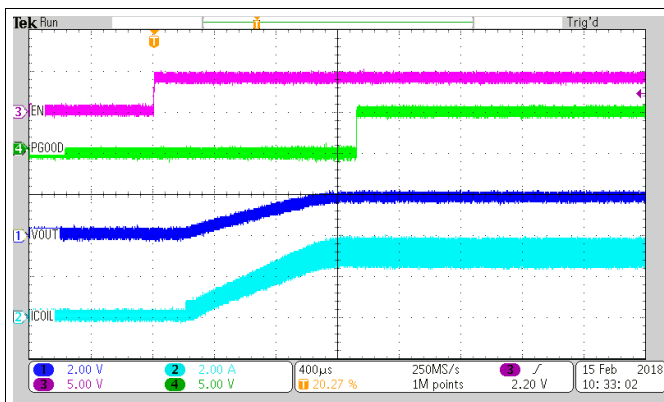
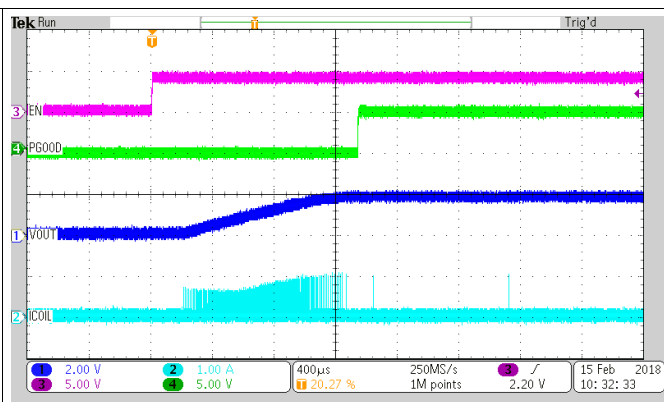


图 37. Typical Operation PSM



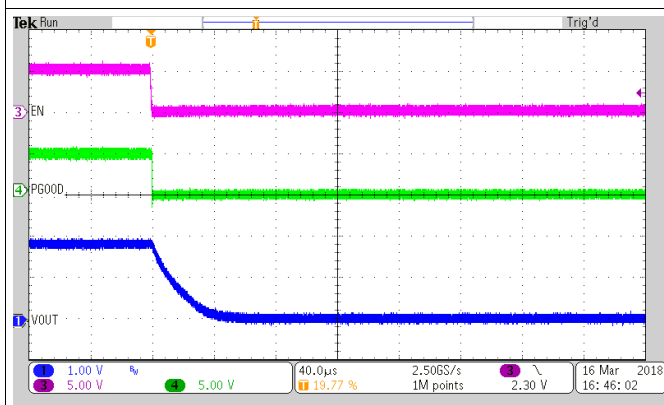
$C_{OUT}=2 \times 10 \mu F$

图 38. Startup into 0.6-Ohm (TPS62823)



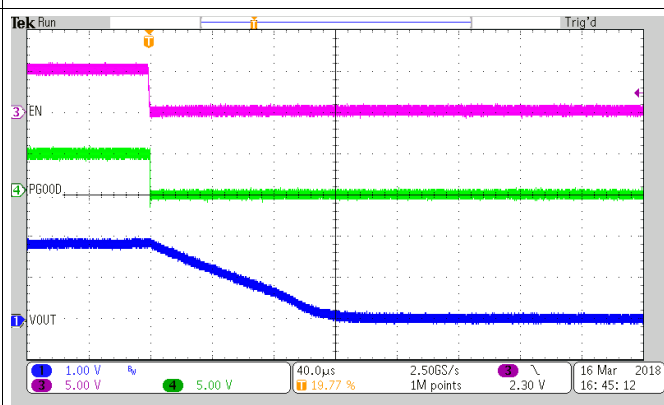
$C_{OUT}=2 \times 10 \mu F$

图 39. Startup at No Load



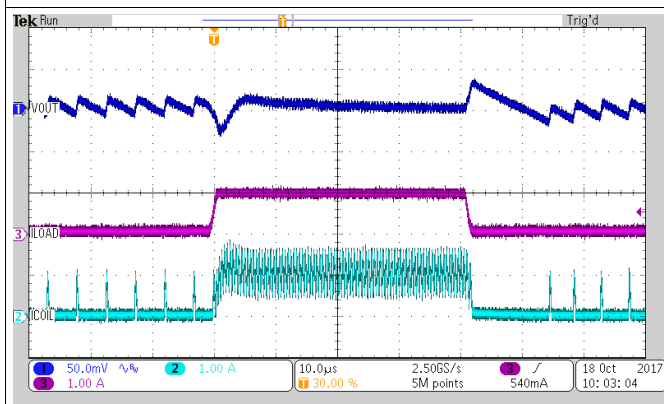
$C_{OUT}=2 \times 10 \mu F$

图 40. Active Output Discharge at load 1.8-Ohm



$C_{OUT}=2 \times 10 \mu F$

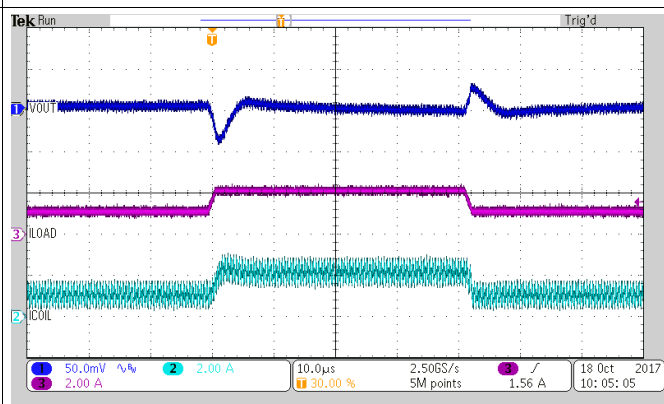
图 41. Active Output Discharge at No Load



$C_{OUT}=2 \times 10 \mu F$

$C_{ff}=120 pF$

图 42. Load Transient Response, 50mA to 1A, TPS62822



$C_{OUT}=2 \times 10 \mu F$

$C_{ff}=120 pF$

图 43. Load Transient Response, 1A to 2A, TPS62822

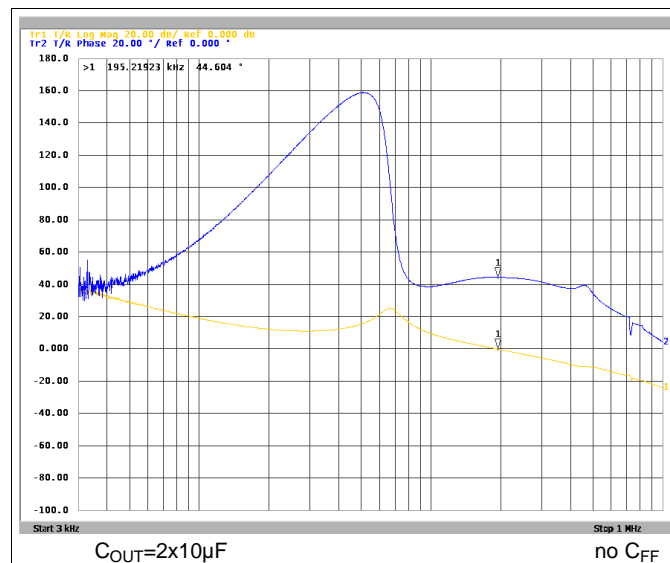


图 44. Frequency Response (TPS62823), IOUT=3A

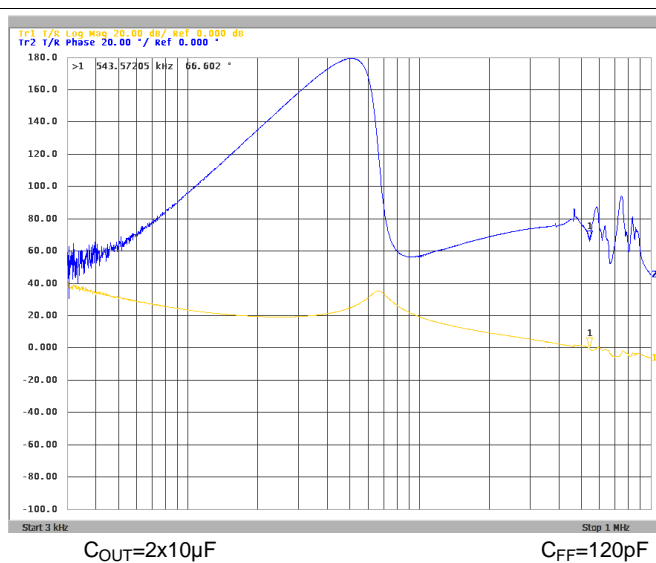


图 45. Frequency Response (TPS62823), IOUT=3A

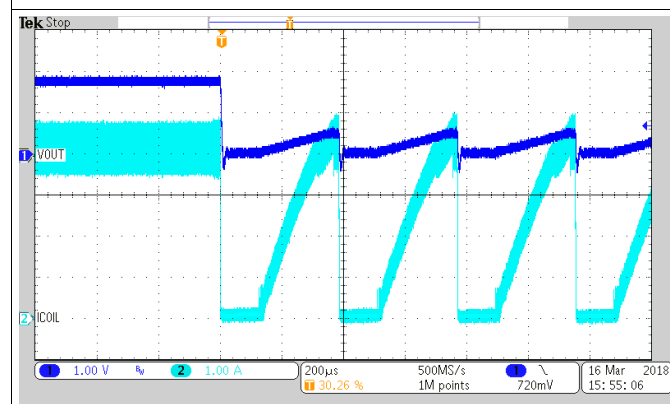


图 46. Overload Response of TPS62823

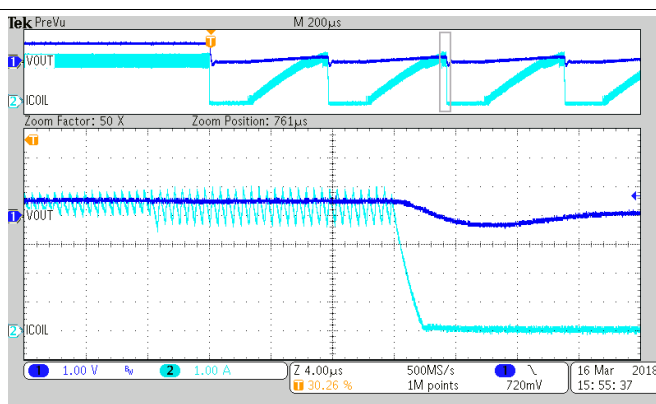


图 47. Overload Response of TPS62823 (Hiccup cycle)

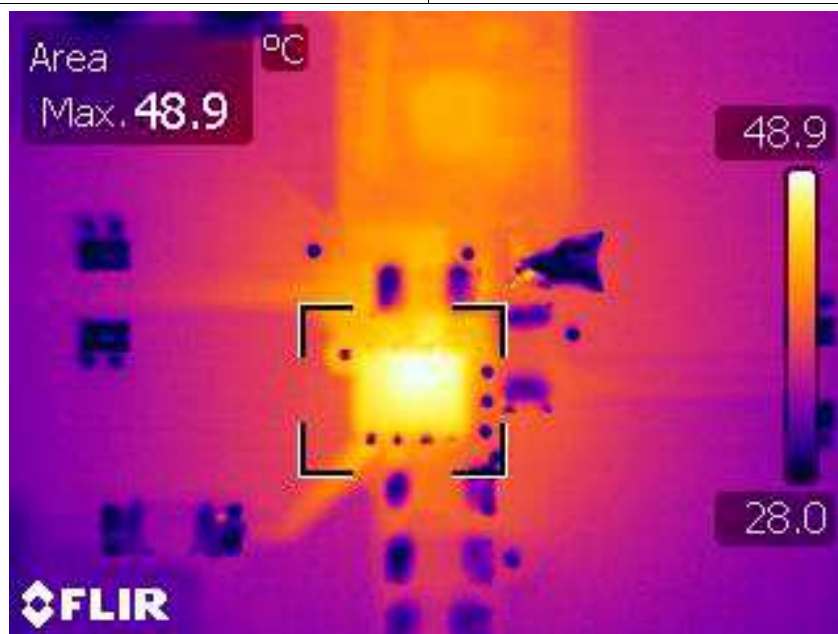


图 48. Device Temperature Rise on TPS62823 EVM at IOUT=3A

10 Power Supply Recommendations

The TPS6282x is designed to operate from a 2.4-V to 5.5-V input voltage supply. The input power supply's output current needs to be rated according to the output voltage and the output current of the power rail application.

11 Layout

11.1 Layout Guidelines

The recommended PCB layout for the TPS6282x is shown below. It ensures best electrical and optimized thermal performance considering the following important topics:

- The input capacitor(s) must be placed as close as possible to the VIN and PGND pins of the device. This provides low resistive and inductive paths for the high di/dt input current.
- The SW node connection from the IC to the inductor conducts alternating high currents. It should be kept short.
- The V_{OUT} regulation loop is closed with COUT and its ground connection. To avoid load regulation and EMI noise, the loop should be kept short.
- The FB node is sensitive to dv/dt signals. Therefore the resistive divider should be placed close to the FB and AGND pins.

For more detailed information about the actual EVM solution, see the [EVM users guide](#).

11.2 Layout Example

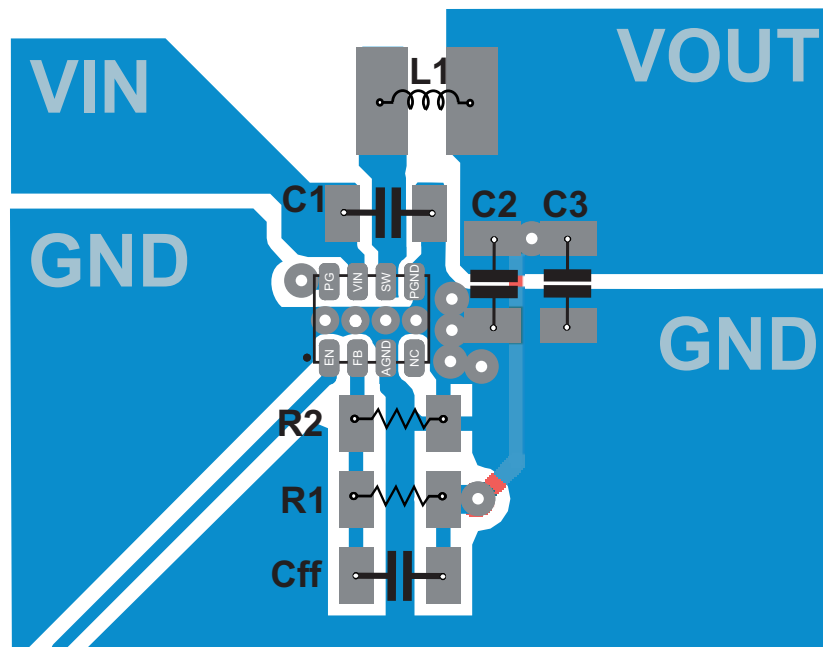


图 49. TPS6282x Board Layout

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62821DLCR	ACTIVE	VSON-HR	DLC	8	3000	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1	Samples
TPS62821DLCT	ACTIVE	VSON-HR	DLC	8	250	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1	Samples
TPS62822DLCR	ACTIVE	VSON-HR	DLC	8	3000	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	-40 to 125	A2	Samples
TPS62822DLCT	ACTIVE	VSON-HR	DLC	8	250	RoHS & Green	Call TI NIPDAU	Level-1-260C-UNLIM	-40 to 125	A2	Samples
TPS62823DLCR	ACTIVE	VSON-HR	DLC	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A3	Samples
TPS62823DLCT	ACTIVE	VSON-HR	DLC	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A3	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

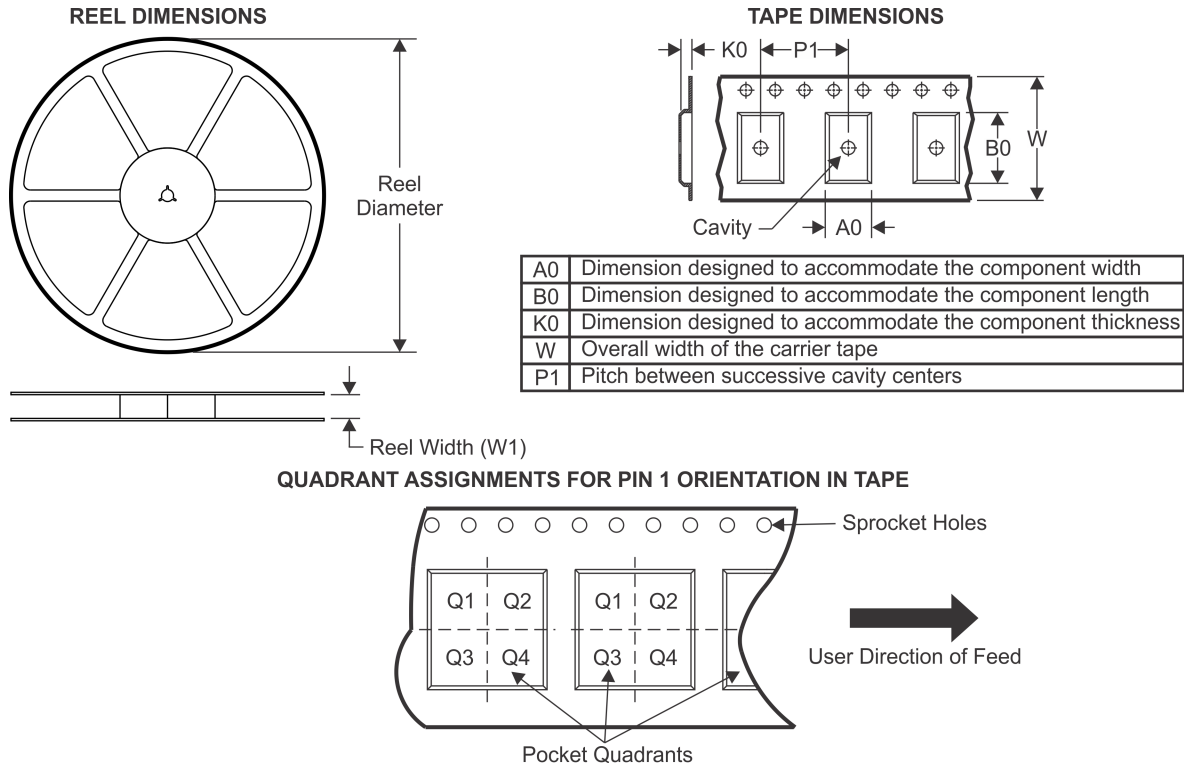
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

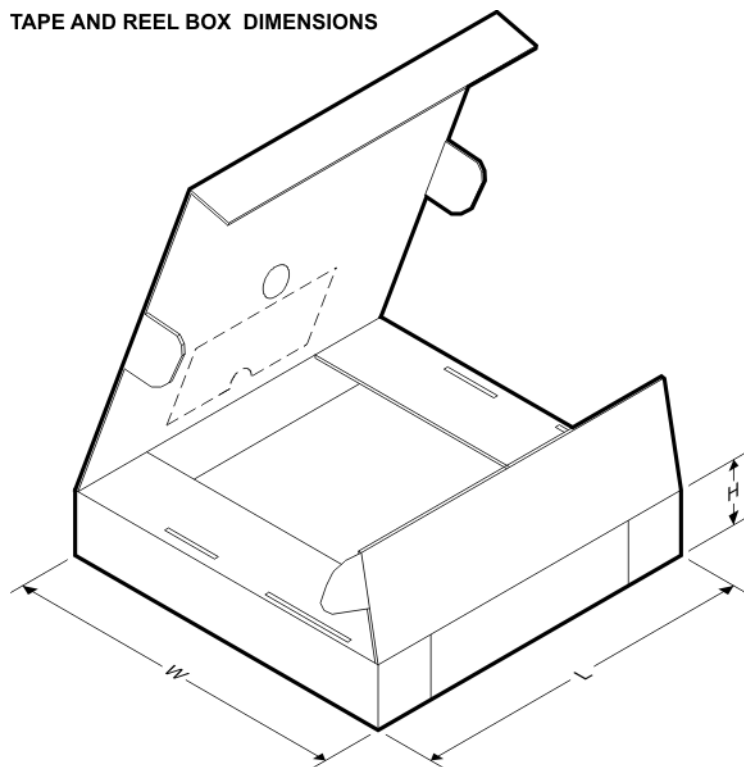
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62821DLCR	VSON-HR	DLC	8	3000	180.0	8.4	1.8	2.25	1.15	4.0	8.0	Q1
TPS62821DLCT	VSON-HR	DLC	8	250	180.0	8.4	1.8	2.25	1.15	4.0	8.0	Q1
TPS62822DLCR	VSON-HR	DLC	8	3000	180.0	8.4	1.8	2.25	1.15	4.0	8.0	Q1
TPS62822DLCT	VSON-HR	DLC	8	250	180.0	8.4	1.8	2.25	1.15	4.0	8.0	Q1
TPS62823DLCR	VSON-HR	DLC	8	3000	180.0	8.4	1.8	2.25	1.15	4.0	8.0	Q1
TPS62823DLCT	VSON-HR	DLC	8	250	180.0	8.4	1.8	2.25	1.15	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62821DLCR	VSON-HR	DLC	8	3000	182.0	182.0	20.0
TPS62821DLCT	VSON-HR	DLC	8	250	182.0	182.0	20.0
TPS62822DLCR	VSON-HR	DLC	8	3000	182.0	182.0	20.0
TPS62822DLCT	VSON-HR	DLC	8	250	182.0	182.0	20.0
TPS62823DLCR	VSON-HR	DLC	8	3000	182.0	182.0	20.0
TPS62823DLCT	VSON-HR	DLC	8	250	182.0	182.0	20.0

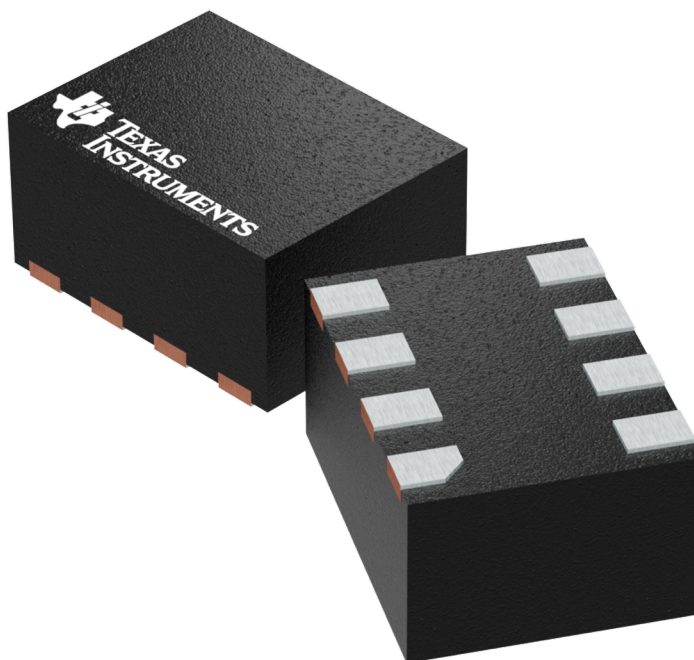
DLC 8

2.0 x 1.5 mm, 0.5 mm pitch

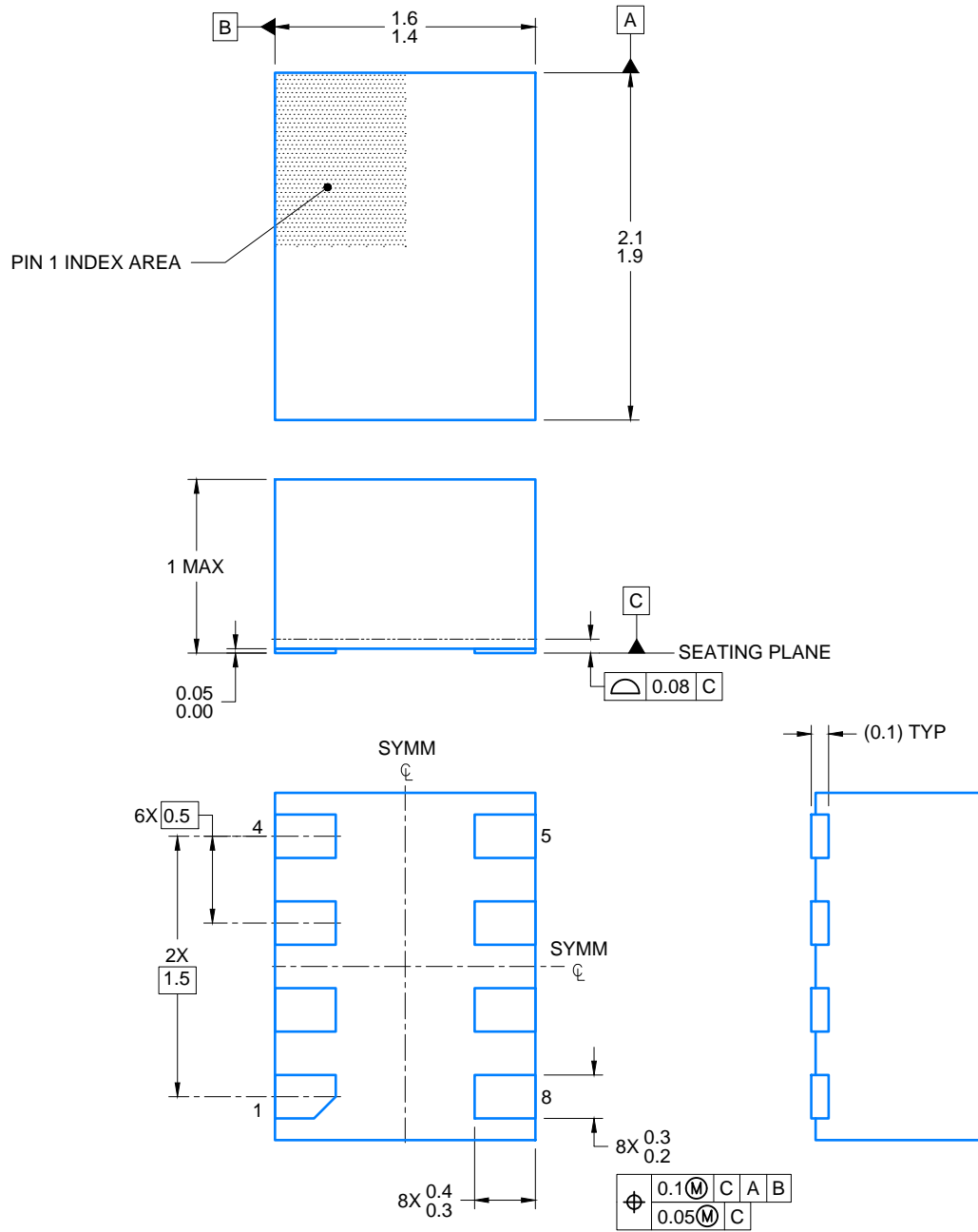
GENERIC PACKAGE VIEW

VSON-HR - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



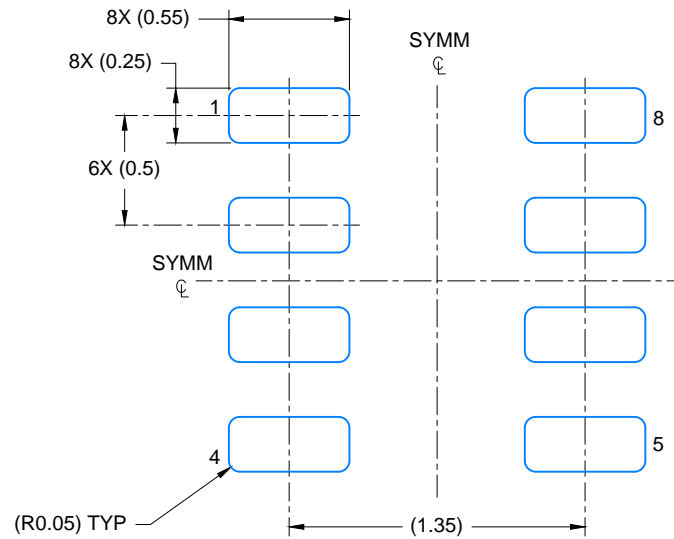
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



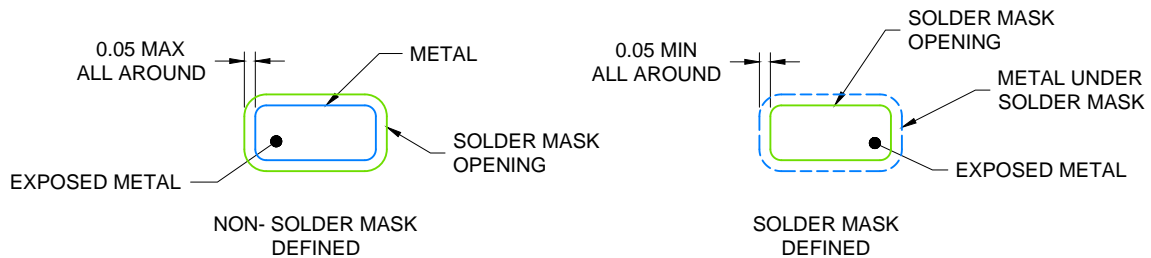
4223754/A 06/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

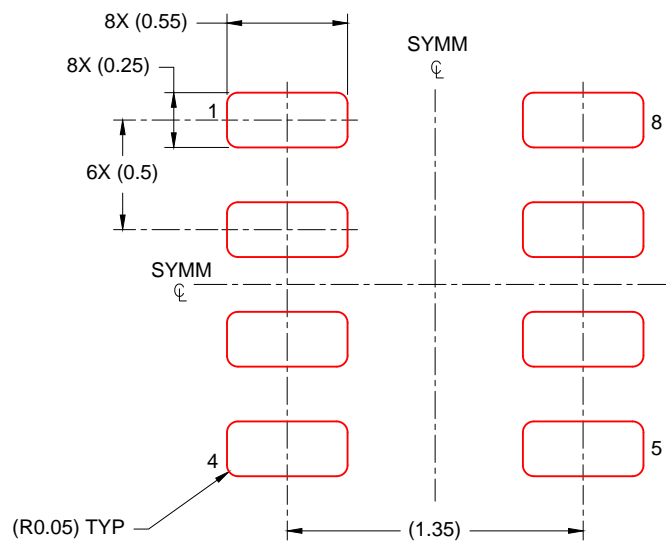


SOLDER MASK DETAILS

4223754/A 06/2017

NOTES: (continued)

- For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slue271) .



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4223754/A 06/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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