SGM820
Precision Voltage Supervisor with Integrated Watchdog Timer

GENERAL DESCRIPTION

The SGM820 combines a precision voltage supervisor with a programmable watchdog timer. The SGM820 is suitable for monitoring common rail voltages of 1.8V, 2.5V, 3V, 3.3V and 5V. The SGM820 comparator achieves a high accuracy (-40℃ to +125℃) for the under-voltage threshold and also includes accurate hysteresis, making the device ideal for use with tight tolerance systems. The supervisor nRESET delay features a high accuracy, high-precision delay timing.

The SGM820 includes a programmable watchdog timer for a wide variety of applications. The dedicated watchdog output (nWDO) enables increased resolution to help determine the nature of fault conditions. The watchdog timeouts can be programmed either by an external capacitor, or by factory-programmed default delay settings. The watchdog can be disabled via logic pins to avoid undesired watchdog timeouts during the development process.

The SGM820 is available in Green TDFN-3×3-8L and TDFN-2×2-8L packages. It operates over an ambient temperature range of -40℃ to +125℃.

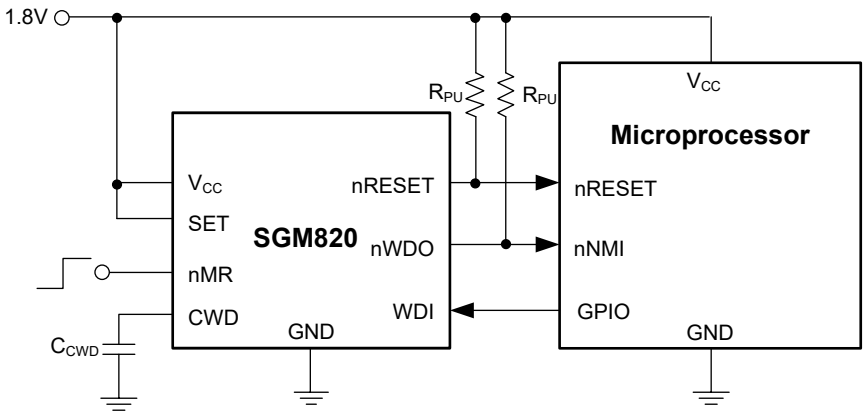
FEATURES

- **High Accuracy Voltage Threshold (< 1%)**
- **Precision Under-Voltage Monitoring:**
  - **Supports Common Rails of 1.8V, 2.5V, 3V, 3.3V and 5V**
  - **0.5% Typical Hysteresis**
- **Factory-Programmed Precision Watchdog and Reset Timers:**
  - **±15% Accurate WDT and RST Delays**
- **User-Programmable Watchdog Timeout**
- **Input Voltage Range: 1.6V to 6.5V**
- **Low Supply Current: 1.2μA (TYP)**
- **Open-Drain Outputs**
- **Watchdog Disable Feature**
- **Manual Reset Input (nMR)**
- **-40℃ to +125℃ Operating Temperature Range**
- **Available in Green TDFN-3×3-8L and TDFN-2×2-8L Packages**

APPLICATIONS

Safety-Critical Applications
Telematics Control Units
FPGAs and ASICs
Microcontrollers and DSPs

TYPICAL APPLICATION



PACKAGE/ORDERING INFORMATION

MODEL	UNDER-VOLTAGE THRESHOLD (V)	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM820A-4.8	4.800	TDFN-3×3-8L	SGM820A-4.8XTDB8G/TR	SGM MKBDB XXXXX	Tape and Reel, 4000
	4.800	TDFN-2×2-8L	SGM820A-4.8XTDE8G/TR	MJ1 XXXX	Tape and Reel, 3000
SGM820B-4.8	4.800	TDFN-3×3-8L	SGM820B-4.8XTDB8G/TR	SGM ML5DB XXXXX	Tape and Reel, 4000
	4.800	TDFN-2×2-8L	SGM820B-4.8XTDE8G/TR	MJB XXXX	Tape and Reel, 3000
SGM820A-4.6	4.650	TDFN-3×3-8L	SGM820A-4.6XTDB8G/TR	SGM MKADB XXXXX	Tape and Reel, 4000
	4.650	TDFN-2×2-8L	SGM820A-4.6XTDE8G/TR	MJ0 XXXX	Tape and Reel, 3000
SGM820B-4.6	4.650	TDFN-3×3-8L	SGM820B-4.6XTDB8G/TR	SGM ML4DB XXXXX	Tape and Reel, 4000
	4.650	TDFN-2×2-8L	SGM820B-4.6XTDE8G/TR	MJA XXXX	Tape and Reel, 3000
SGM820A-3.1	3.168	TDFN-3×3-8L	SGM820A-3.1XTDB8G/TR	SGM MK9DB XXXXX	Tape and Reel, 4000
	3.168	TDFN-2×2-8L	SGM820A-3.1XTDE8G/TR	MIF XXXX	Tape and Reel, 3000
SGM820B-3.1	3.168	TDFN-3×3-8L	SGM820B-3.1XTDB8G/TR	SGM ML3DB XXXXX	Tape and Reel, 4000
	3.168	TDFN-2×2-8L	SGM820B-3.1XTDE8G/TR	MJ9 XXXX	Tape and Reel, 3000
SGM820A-3.0	3.069	TDFN-3×3-8L	SGM820A-3.0XTDB8G/TR	SGM MK8DB XXXXX	Tape and Reel, 4000
	3.069	TDFN-2×2-8L	SGM820A-3.0XTDE8G/TR	MIE XXXX	Tape and Reel, 3000
SGM820B-3.0	3.069	TDFN-3×3-8L	SGM820B-3.0XTDB8G/TR	SGM ML2DB XXXXX	Tape and Reel, 4000
	3.069	TDFN-2×2-8L	SGM820B-3.0XTDE8G/TR	MJ8 XXXX	Tape and Reel, 3000
SGM820A-2.8	2.880	TDFN-3×3-8L	SGM820A-2.8XTDB8G/TR	SGM MK7DB XXXXX	Tape and Reel, 4000
	2.880	TDFN-2×2-8L	SGM820A-2.8XTDE8G/TR	MID XXXX	Tape and Reel, 3000
SGM820B-2.8	2.880	TDFN-3×3-8L	SGM820B-2.8XTDB8G/TR	SGM ML1DB XXXXX	Tape and Reel, 4000
	2.880	TDFN-2×2-8L	SGM820B-2.8XTDE8G/TR	MJ7 XXXX	Tape and Reel, 3000

PACKAGE/ORDERING INFORMATION (continued)

MODEL	UNDER-VOLTAGE THRESHOLD (V)	PACKAGE DESCRIPTION	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM820A-2.7	2.790	TDFN-3×3-8L	SGM820A-2.7XTDB8G/TR	SGM MK6DB XXXXX	Tape and Reel, 4000
	2.790	TDFN-2×2-8L	SGM820A-2.7XTDE8G/TR	MIC XXXX	Tape and Reel, 3000
SGM820B-2.7	2.790	TDFN-3×3-8L	SGM820B-2.7XTDB8G/TR	SGM ML0DB XXXXX	Tape and Reel, 4000
	2.790	TDFN-2×2-8L	SGM820B-2.7XTDE8G/TR	MJ6 XXXX	Tape and Reel, 3000
SGM820A-2.4	2.400	TDFN-3×3-8L	SGM820A-2.4XTDB8G/TR	SGM MK5DB XXXXX	Tape and Reel, 4000
	2.400	TDFN-2×2-8L	SGM820A-2.4XTDE8G/TR	MIB XXXX	Tape and Reel, 3000
SGM820B-2.4	2.400	TDFN-3×3-8L	SGM820B-2.4XTDB8G/TR	SGM MKFDB XXXXX	Tape and Reel, 4000
	2.400	TDFN-2×2-8L	SGM820B-2.4XTDE8G/TR	MJ5 XXXX	Tape and Reel, 3000
SGM820A-2.3	2.325	TDFN-3×3-8L	SGM820A-2.3XTDB8G/TR	SGM MK4DB XXXXX	Tape and Reel, 4000
	2.325	TDFN-2×2-8L	SGM820A-2.3XTDE8G/TR	MI9 XXXX	Tape and Reel, 3000
SGM820B-2.3	2.325	TDFN-3×3-8L	SGM820B-2.3XTDB8G/TR	SGM MKEDB XXXXX	Tape and Reel, 4000
	2.325	TDFN-2×2-8L	SGM820B-2.3XTDE8G/TR	MJ4 XXXX	Tape and Reel, 3000
SGM820A-1.7	1.728	TDFN-3×3-8L	SGM820A-1.7XTDB8G/TR	SGM MK2DB XXXXX	Tape and Reel, 4000
	1.728	TDFN-2×2-8L	SGM820A-1.7XTDE8G/TR	MI7 XXXX	Tape and Reel, 3000
SGM820B-1.7	1.728	TDFN-3×3-8L	SGM820B-1.7XTDB8G/TR	SGM MKDDB XXXXX	Tape and Reel, 4000
	1.728	TDFN-2×2-8L	SGM820B-1.7XTDE8G/TR	MJ3 XXXX	Tape and Reel, 3000
SGM820A-1.6	1.674	TDFN-3×3-8L	SGM820A-1.6XTDB8G/TR	SGM MK1DB XXXXX	Tape and Reel, 4000
	1.674	TDFN-2×2-8L	SGM820A-1.6XTDE8G/TR	MI6 XXXX	Tape and Reel, 3000
SGM820B-1.6	1.674	TDFN-3×3-8L	SGM820B-1.6XTDB8G/TR	SGM MKCDB XXXXX	Tape and Reel, 4000
	1.674	TDFN-2×2-8L	SGM820B-1.6XTDE8G/TR	MJ2 XXXX	Tape and Reel, 3000

NOTE:

SGM820A-X provide standard user-programming watchdog timeout: $t_{WD\_standard}$ (ms) = 3.33 × C_{CWD} (nF) + 0.28 (ms)

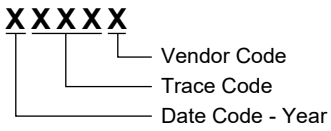
SGM820B-X provide extended user-programming watchdog timeout: $t_{WD\_extended}$ (ms) = 78.3 × C_{CWD} (nF) + 51 (ms)

PACKAGE/ORDERING INFORMATION (continued)

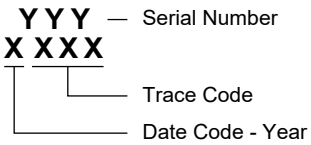
MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XXXX = Date Code and Trace Code.

TDFN-3×3-8L



TDFN-2×2-8L



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range, V_{CC} ..... -0.3V to 7V
Output Voltage Range
nRESET, nWDO .....-0.3V to 7V
Voltage Ranges
SET, WDI, nMR.....-0.3V to 7V
CWD.....-0.3V to V_{CC} + 0.3V
Output Pin Current
nRESET, nWDO ..... ±20mA
Input Current (All Pins) ..... ±20mA
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
ESD Susceptibility
Lead Temperature (Soldering, 10s).....+260℃
HBM.....4000V
CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Supply Pin Voltage, V_{CC}.....1.6V to 6.5V

Watchdog Timing Capacitor, C_{CWD}.....0.1nF to 1000nF (1) (2)
Pull-Up Resistor to V_{CC}, CWD.....9kΩ to 11kΩ

Pull-Up Resistor, nRESET and nWDO, R_{PU}.....1kΩ to 100kΩ
nRESET Pin Current, I_{nRESET} 10mA
Watchdog Output Current, I_{nWDO} 10mA
Junction Temperature Range.....-40℃ to +125℃
Ambient Temperature Range.....-40℃ to +125℃

NOTES:
1. Using standard timing with a C_{CWD} capacitor from 0.1nF to 1000nF gives a t_{WD_TYP} from 0.613ms to 3.33s correspondingly.

2. Using extended timing with a C_{CWD} capacitor from 0.1nF to 1000nF gives a t_{WD_TYP} from 58.83ms to 78.35s correspondingly.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

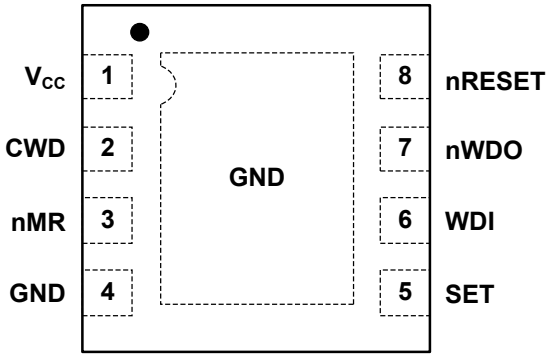
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATIONS

(TOP VIEW)



TDFN-3×3-8L/TDFN-2×2-8L

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
1	V_{CC}	I	Supply Voltage Pin. For noisy systems, connecting a 0.1μF bypass capacitor is recommended.
2	CWD	I	Programmable Watchdog Timeout Input. The watchdog timeout is set by connecting a capacitor between this pin and ground. Connecting via a 10kΩ resistor to V_{CC} or leaving unconnected further enables the selection of the preset watchdog timeouts; see the CWD functionality section. The SGM820 determines the watchdog timeout using either Equation 1 or Equation 2 with standard or extended timing, respectively.
3	nMR	I	Manual Reset Pin. A logical low on this pin issues an nRESET. This pin is internally pulled up to V_{CC}. nRESET remains low for a fixed reset delay time (t_{RST}) after nMR is deasserted (high).
4	GND	G	Ground Pin.
5	SET	I	Logic Input. Grounding the SET pin disables the watchdog timer. SET and CWD pins select the watchdog timeouts; see the SET section.
6	WDI	I	Watchdog Input. A falling edge must occur at WDI before the timeout (t_{WD}) expires. When the watchdog is not in use, the SET pin can be used to disable the watchdog. WDI is ignored when nRESET or nWDO is low (asserted) and when the watchdog is disabled. If the watchdog is disabled, WDI pin cannot be left unconnected and must be driven to either V_{CC} or GND.
7	nWDO	O	Watchdog Output. Connect nWDO pin with a 1kΩ to 100kΩ resistor to the correct pull-up voltage rail (V_{PU}). nWDO goes low (asserts) when a watchdog timeout occurs. nWDO only asserts when nRESET is high. When a watchdog timeout occurs, nWDO goes low (asserts) for the set nRESET timeout delay (t_{RST}). When nRESET goes low, nWDO is in a high-impedance state.
8	nRESET	O	Reset Output. Connect nRESET pin with a 1kΩ to 100kΩ resistor to the correct pull-up voltage rail (V_{PU}). nRESET goes low (asserts) when V_{CC} goes below the under-voltage threshold (V_{ITN}). When V_{CC} is within the normal operating range, the nRESET timeout-counter starts. At completion, nRESET goes high (deasserts). During start-up, the state of nRESET is undefined below the specified power-on-reset (POR) voltage (V_{POR}). Above POR, nRESET goes low and remains low until the monitored voltage is within the correct operating range (above V_{ITN} + V_{HYS}) and the nRESET timeout is complete.
Exposed Pad	GND	G	Ground Pin. Connect the thermal pad to a large-area ground plane. The exposed pad is internally connected to GND.

NOTE: I: Input, O: Output, G: Ground.

ELECTRICAL CHARACTERISTICS

(V_{ITN} + V_{HYS} ≤ V_{CC} ≤ 6.5V, Full = -40℃ to +125℃, the open-drain pull-up resistors are 10kΩ for each output, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
General Characteristics							
Power Supply Voltage	V_{CC} (1) (2)		Full	1.6		6.5	V
Supply Current	I_{CC}		Full		1.2	3.3	μA
Reset Function							
Power-On Reset Voltage	V_{POR} (1)	I_{nRESET} = 15μA, $V_{OL(MAX)}$ = 0.25V	Full			0.8	V
Under-Voltage Threshold	V_{ITN}	SGM820A/B-4.8, V_{CC} falling	Full	4.757	4.800	4.843	V
		SGM820A/B-4.6, V_{CC} falling	Full	4.608	4.650	4.692	
		SGM820A/B-3.1, V_{CC} falling	Full	3.139	3.168	3.197	
		SGM820A/B-3.0, V_{CC} falling	Full	3.041	3.069	3.097	
		SGM820A/B-2.8, V_{CC} falling	Full	2.854	2.880	2.906	
		SGM820A/B-2.7, V_{CC} falling	Full	2.765	2.790	2.815	
		SGM820A/B-2.4, V_{CC} falling	Full	2.377	2.400	2.423	
		SGM820A/B-2.3, V_{CC} falling	Full	2.303	2.325	2.347	
		SGM820A/B-1.7, V_{CC} falling	Full	1.711	1.728	1.745	
		SGM820A/B-1.6, V_{CC} falling	Full	1.658	1.674	1.690	
Hysteresis Voltage	V_{HYS}	V_{CC} rising	Full	0.15% × V_{ITN}	0.50% × V_{ITN}	0.85% × V_{ITN}	V
nMR Pin Internal Pull-Up Current	I_{nMR}	V_{nMR} = 0V	Full	520	620	720	nA
Watchdog Function							
CWD Pin Charging Current	I_{CWD}	CWD = 0.5V	Full	337	375	413	nA
CWD Pin Threshold Voltage	V_{CWD}		Full	1.180	1.210	1.245	V
nRESET, nWDO Output Low	V_{OL}	V_{CC} = 5V, I_{SINK} = 3mA	Full			0.4	V
nRESET, nWDO Output Leakage Current, Open-Drain	I_D	V_{CC} = V_{ITN} + V_{HYS}, V_{nRESET} = V_{nWDO} = 6.5V	Full			1	μA
Low-Level Input Voltage of nMR	V_{IL_nMR}		Full			0.25	V
High-Level Input Voltage of nMR	V_{IH_nMR}		Full	0.8			V
Low-Level Input Voltage of SET	V_{IL_SET}		Full			0.25	V
High-Level Input Voltage of SET	V_{IH_SET}		Full	0.8			V
Low-Level Input Voltage of WDI	V_{IL_WDI}		Full			0.3 × V_{CC}	V
High-Level Input Voltage of WDI	V_{IH_WDI}		Full	0.8 × V_{CC}			V

NOTES:

1. When V_{CC} falls below V_{POR}, nRESET and nWDO are undefined.
2. During power-on, V_{CC} must be a minimum 1.6V for at least 400μs before nRESET correlates with V_{CC}.

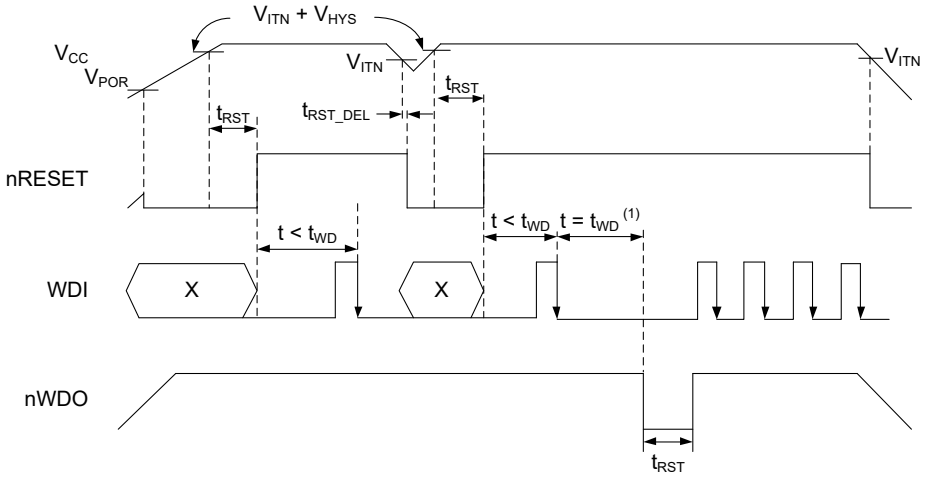
TIMING REQUIREMENTS

(At T_A = +25℃, V_{ITN} + V_{HYS} ≤ V_{CC} ≤ 6.5V, Full = -40℃ to +125℃, the open-drain pull-up resistors are 10kΩ for each output, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	TEMP	MIN	TYP	MAX	UNITS
General							
CWD Pin Evaluation Period	t_{INIT}		+25℃		390		μs
Minimum nMR Pin Pulse Duration			+25℃		1		μs
Reset Function							
nRESET Timeout Period	t_{RST}		Full	170	200	230	ms
V_{CC} to nRESET Delay	t_{RST_DEL}	V_{CC} = (V_{ITN} + V_{HYS}) × (1 + 2.5%) to V_{ITN} × (1 - 2.5%)	+25℃		90		μs
nMR to nRESET Delay	t_{MR_DEL}		+25℃		700		ns
Watchdog Function							
Watchdog Timeout (1)	t_{WD}	CWD = NC, SET = 0 (2)	Watchdog disabled				
		CWD = NC, SET = 1 (2)	Full	1360	1600	1840	ms
		CWD = 10kΩ to V_{CC}, SET = 0 (2)	Watchdog disabled				
		CWD = 10kΩ to V_{CC}, SET = 1 (2)	Full	170	200	230	ms
Set-Up Time Required for Device to Respond to Changes on WDI after Being Enabled	t_{WD_SETUP}		+25℃		140		μs
Minimum WDI, nMR Pin Pulse Duration			+25℃		50		ns
WDI to nWDO Delay	t_{WD_DEL}		+25℃		100		ns

NOTES:
1. The fixed watchdog timing covers both standard version SGM820A-X and extended version SGM820B-X.
2. SET = 0 means V_{SET} < V_{IL_SET}; SET = 1 means V_{SET} > V_{IH_SET}.

TIMING DIAGRAM



NOTE:
1. See Figure 2 for WDI timing requirements.

Figure 1. Timing Diagram

TIMING DIAGRAM (continued)

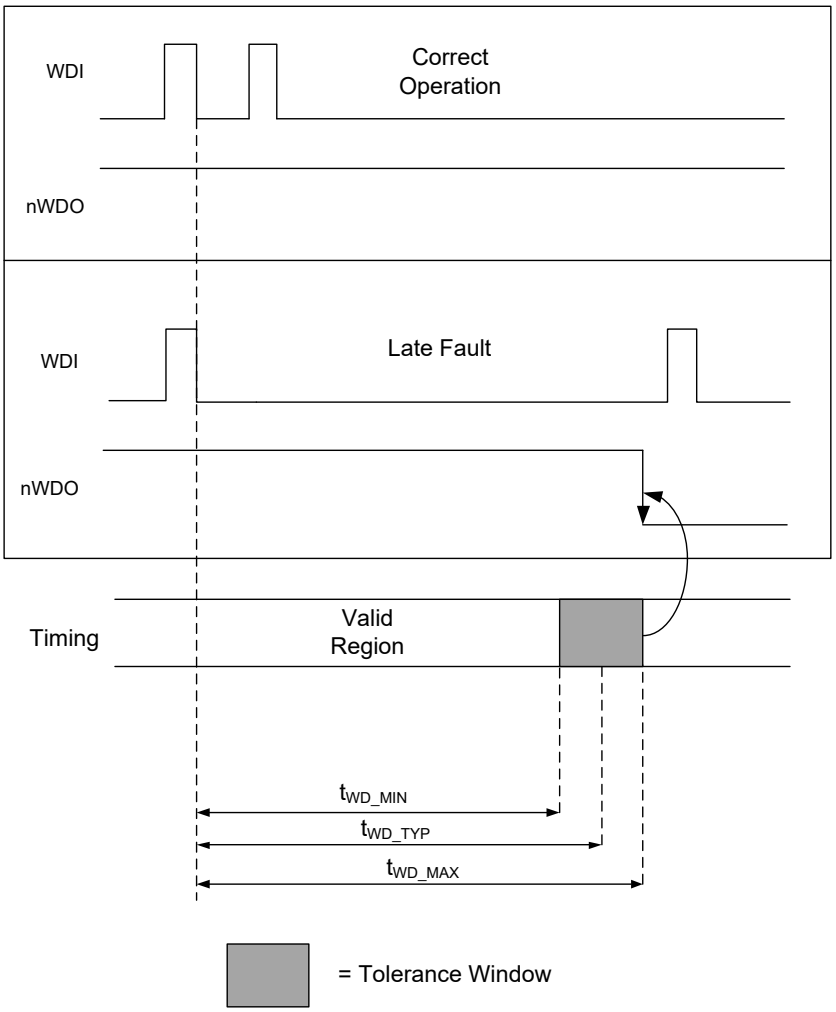
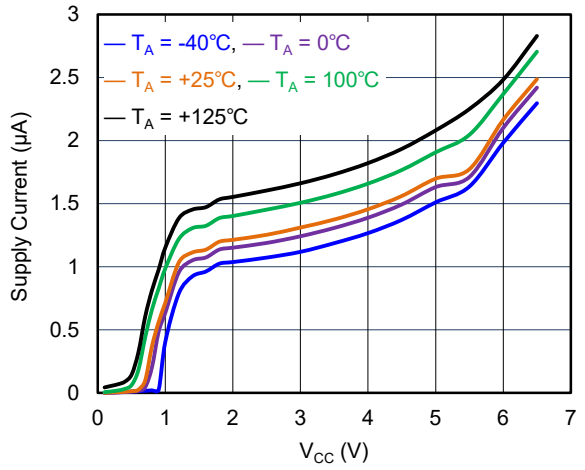


Figure 2. Watchdog Timing Diagram

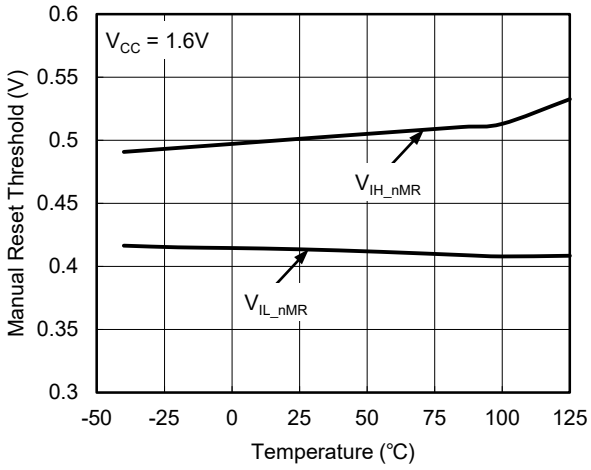
TYPICAL PERFORMANCE CHARACTERISTICS

At T_A = +25℃, 1.6V ≤ V_{CC} ≤ 6.5V, unless otherwise noted.

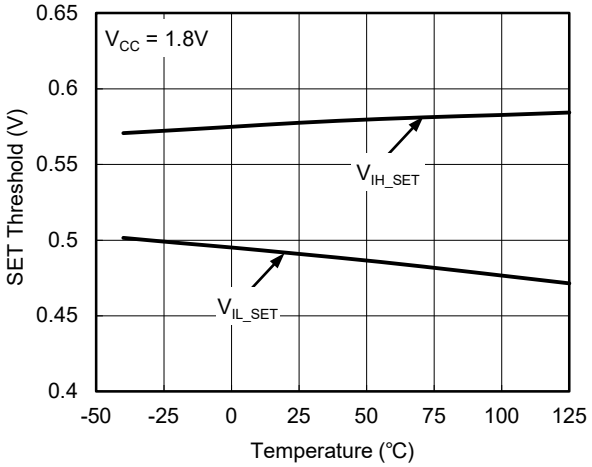
Supply Current vs. Supply Voltage



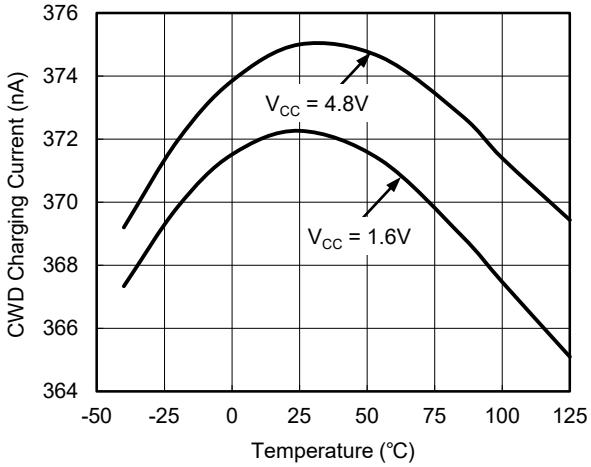
nMR Threshold vs. Temperature



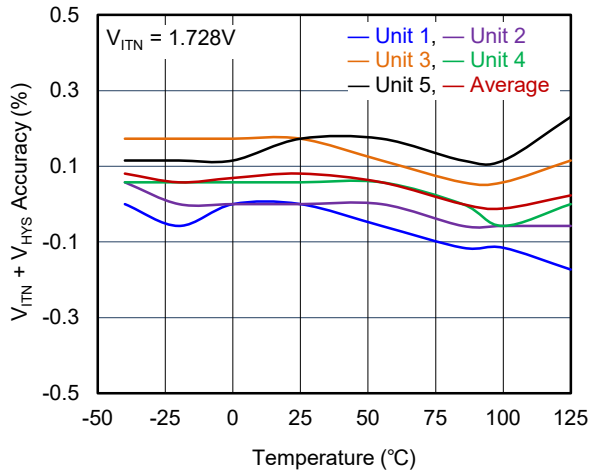
SET Threshold vs. Temperature



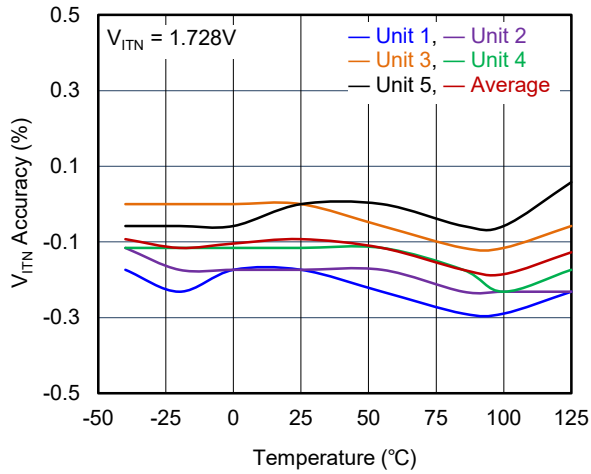
CWD Charging Current vs. Temperature



V_{ITN} + V_{HYS} Accuracy vs. Temperature



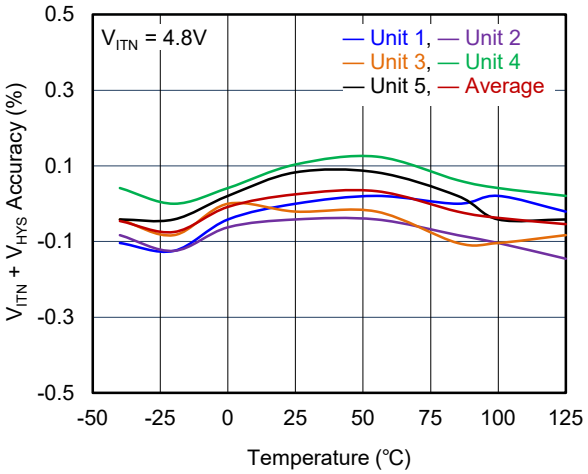
V_{ITN} Accuracy vs. Temperature



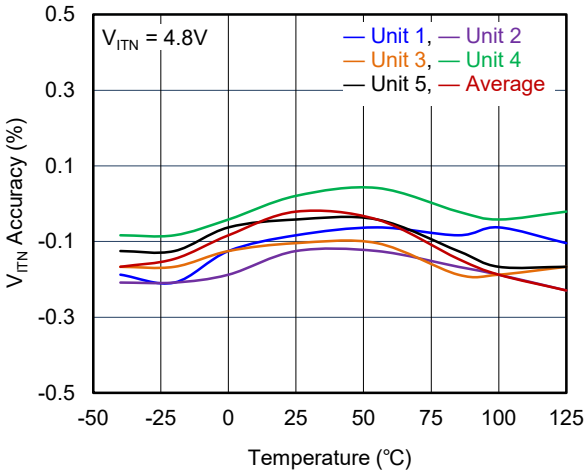
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, 1.6V ≤ V_{CC} ≤ 6.5V, unless otherwise noted.

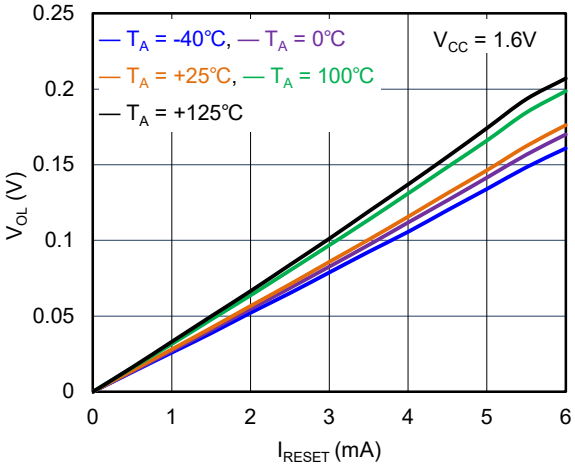
V_{ITN} + V_{HYS} Accuracy vs. Temperature



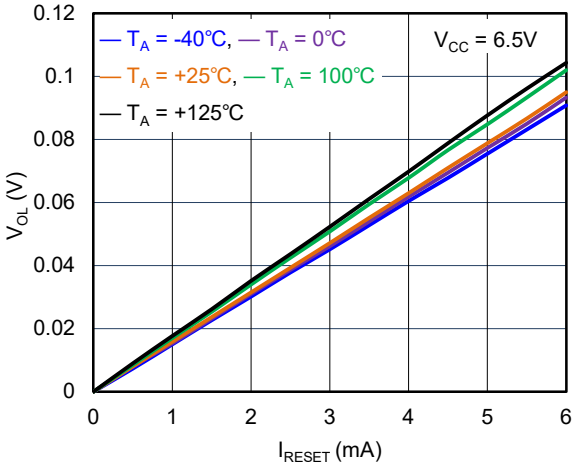
V_{ITN} Accuracy vs. Temperature



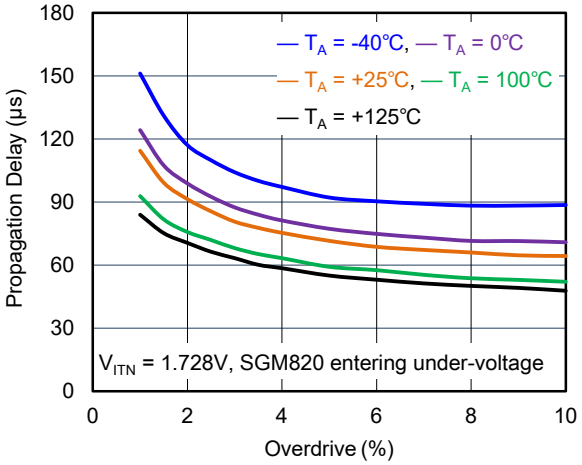
Low-Level nRESET Voltage vs. nRESET Current



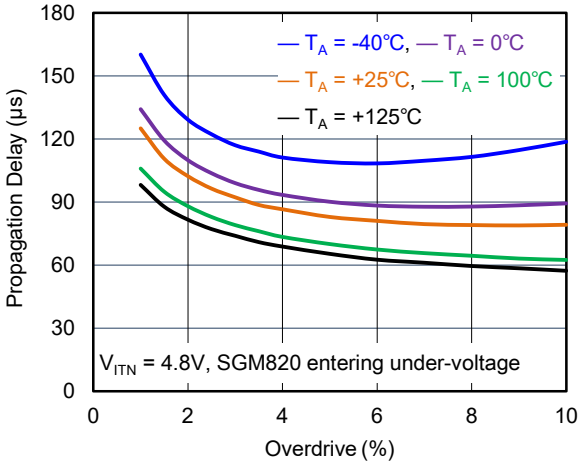
Low-Level nRESET Voltage vs. nRESET Current



Propagation Delay vs. Overdrive



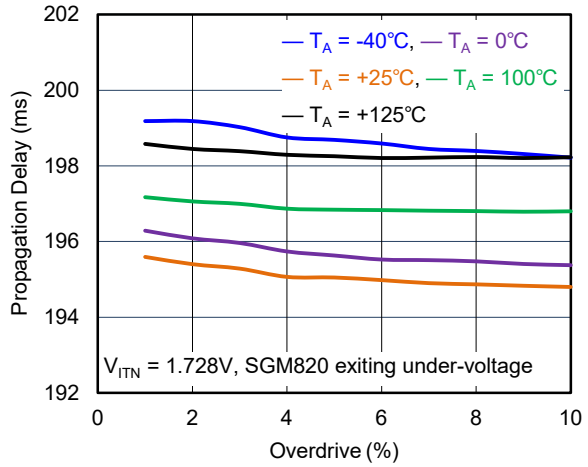
Propagation Delay vs. Overdrive



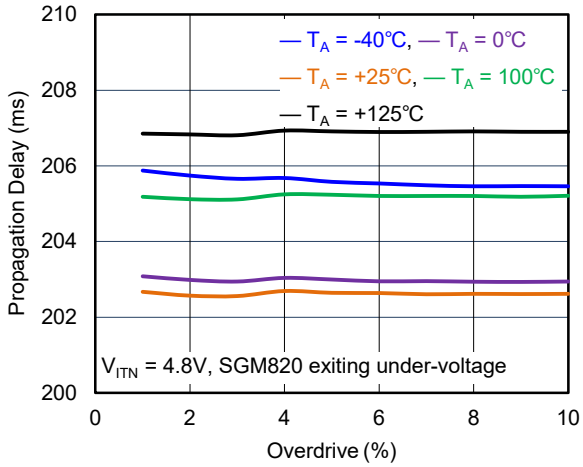
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, 1.6V ≤ V_{CC} ≤ 6.5V, unless otherwise noted.

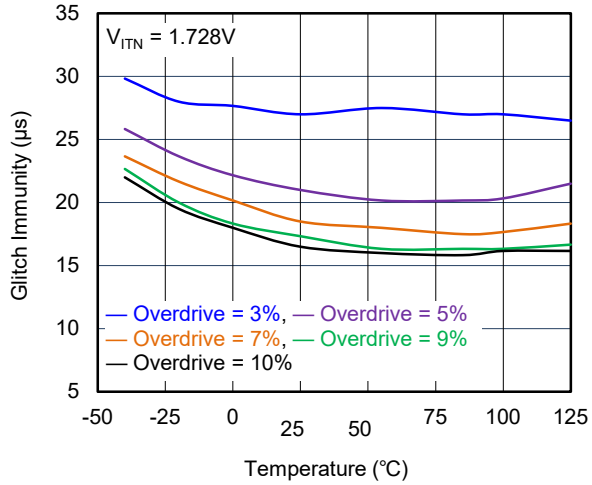
Propagation Delay (t_{RST}) vs. Overdrive



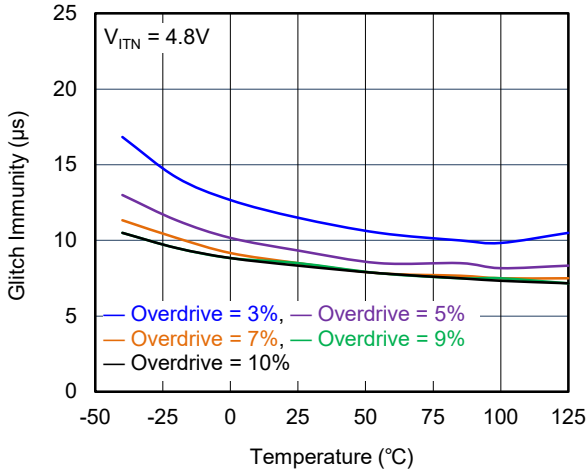
Propagation Delay (t_{RST}) vs. Overdrive



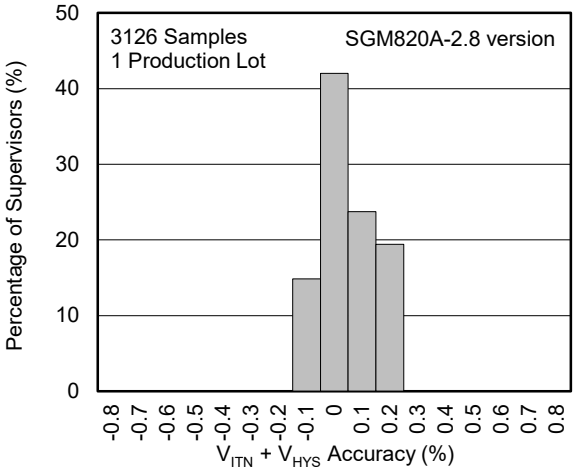
High-to-Low Glitch Immunity vs. Temperature



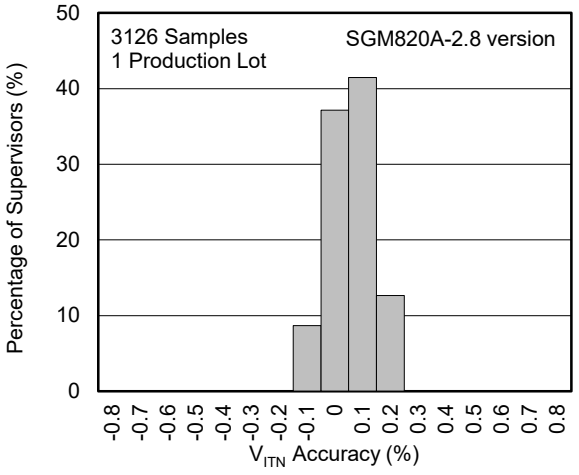
High-to-Low Glitch Immunity vs. Temperature



V_{ITN} + V_{HYS} Accuracy Histogram

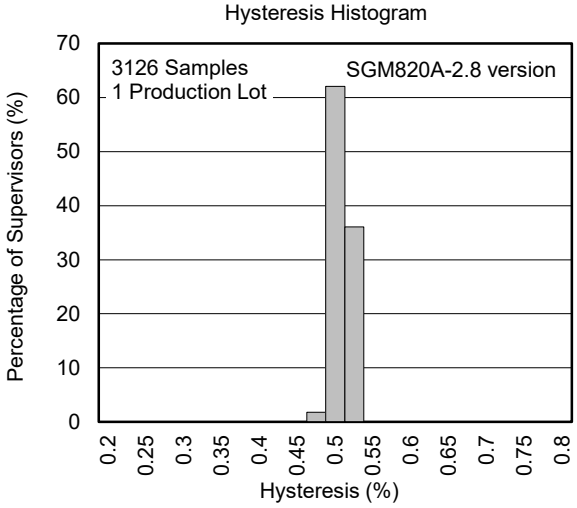


V_{ITN} Accuracy Histogram



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

At T_A = +25℃, 1.6V ≤ V_{CC} ≤ 6.5V, unless otherwise noted.



FUNCTIONAL BLOCK DIAGRAM

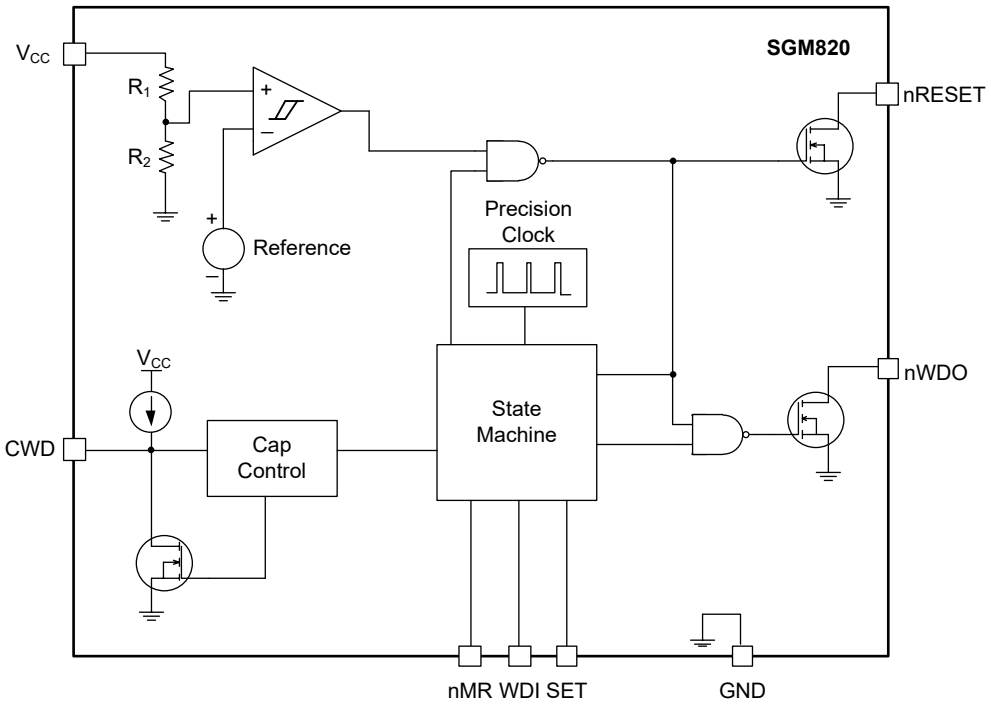


Figure 3. SGM820 Block Diagram

DETAILED DESCRIPTION

Overview

The SGM820 is a high accuracy voltage supervisor with an integrated watchdog timer. This device includes a precision under-voltage supervisor with a threshold that achieves high accuracy over the specified temperature range of -40℃ to +125℃. In addition, the SGM820 includes accurate hysteresis on the threshold, making the device ideal for use with tight tolerance systems where voltage supervisors must ensure an nRESET before the minimum supply tolerance of the microprocessor or system-on-a-chip (SoC) is reached. There are two options for the watchdog timing: standard timing and extended timing. To get standard timing use the SGM820A versions. For extended timing use the SGM820B versions.

nRESET

Connect nRESET to V_{PU} through a 1kΩ to 100kΩ pull-up resistor. nRESET remains high (deasserted) when V_{CC} is greater than the negative threshold voltage (V_{ITN}). If V_{CC} falls below the negative threshold voltage (V_{ITN}), then nRESET is asserted, driving the nRESET pin to low-impedance state. When V_{CC} rises above V_{ITN} + V_{HYS}, a delay circuit is enabled that holds nRESET low for a specified reset delay period (t_{RST}). When the reset delay has elapsed, the nRESET pin goes to a high-impedance state and uses a pull-up resistor to hold nRESET high. The pull-up resistor must be connected to the proper voltage rail to allow other devices to be connected at the correct interface voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The pull-up resistor value is determined by output logic low voltage (V_{OL}), capacitive loading, leakage current (I_D), and the current through the nRESET pin (I_{nRESET}).

Manual Reset (nMR)

The manual reset input (nMR) allows a processor or other logic circuits to initiate a reset. A logic low on nMR causes nRESET to assert. After nMR returns to a logic high and V_{CC} is above V_{ITN} + V_{HYS}, nRESET is deasserted after the reset delay time (t_{RST}). If nMR is not controlled externally, then nMR can either be connected to V_{CC} or left floating because the nMR pin is internally pulled up.

DETAILED DESCRIPTION (continued)

UV Fault Detection

The SGM820 features under-voltage detection for common rails between 1.8V and 5V. The voltage is monitored on the input rail of the device. If V_{CC} drops below V_{ITN}, then nRESET is asserted (low). When V_{CC} is above V_{ITN} + V_{HYS}, nRESET deasserts after t_{RST}, as shown in Figure 4. The internal comparator has built-in hysteresis that provides some noise immunity and ensures stable operation. Although not required in most cases, for noisy applications, good analog design practice is to place a 1nF to 100nF bypass capacitor close to the V_{CC} pin to reduce sensitivity to transient voltages on the monitored signal.

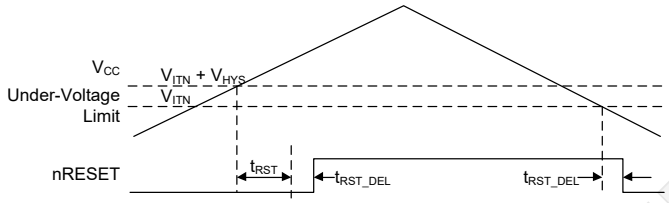


Figure 4. Under-Voltage Detection

Watchdog Mode

This section provides information for the watchdog mode of operation.

CWD

The CWD pin provides the user the functionality of both high precision, factory-programmed watchdog timing options and user-programmable watchdog timing. The SGM820 features three options for setting the watchdog timer: connecting a capacitor to the CWD pin, connecting a pull-up resistor to V_{CC}, and leaving the CWD pin unconnected. The configuration of the CWD pin is evaluated by the device every time V_{CC} enters the valid region (V_{ITN} + V_{HYS} < V_{CC}). The pin evaluation is controlled by an internal state machine that determines which option is connected to the CWD pin. The sequence of events typically takes 390μs (t_{INIT}) to determine if the CWD pin is left unconnected, pulled up through a resistor, or connected to a capacitor. If the CWD pin is being pulled up to V_{CC}, a 10kΩ resistor is required.

Watchdog Input (WDI)

The WDI pin is the watchdog timer input that controls the nWDO output. The WDI input is triggered by the falling edge of the input signal. To ensure proper functionality of the watchdog timer, always issue the WDI pulse before t_{WD_MIN}. If the pulse is issued in this region, then nWDO remains deasserted. Otherwise, the device asserts nWDO, putting the nWDO pin into a low-impedance state.

The watchdog input (WDI) is a digital pin. In order to ensure there is no increase in I_{CC}, drive the WDI pin to either V_{CC} or GND at all times. Putting the pin to an intermediate voltage can cause an increase in supply current (I_{CC}) because of the architecture of the digital logic gates. When nRESET is asserted, the watchdog is disabled and all signals input to WDI are ignored. When nRESET is no longer asserted, the device resumes normal operation and no longer ignores the signal on WDI. If the watchdog is disabled, drive the WDI pin to either V_{CC} or GND. Figure 5 shows the valid region for a WDI pulse to be issued to prevent nWDO from being triggered and pulled low.

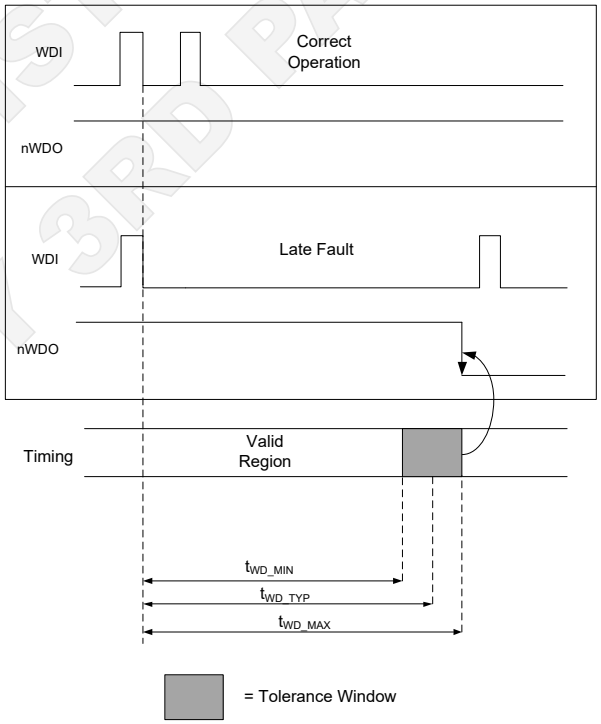


Figure 5. Watchdog Timing Diagram

DETAILED DESCRIPTION (continued)

Watchdog Output (nWDO)

The SGM820 features a watchdog timer with an independent watchdog output (nWDO). The independent watchdog output provides the flexibility to flag a fault in the watchdog timing without performing an entire system reset. When nRESET is not asserted (high), the nWDO signal maintains normal operation, and nWDO signal will maintain low for t_{RST} if asserted. When the nRESET signal is asserted (low), the nWDO pin goes to a high-impedance state. When the nRESET signal is deasserted again, the watchdog timer resumes normal operation.

SET

The SET pin can enable and disable the watchdog timer. If SET is set to GND, the watchdog timer is disabled and WDI is ignored. If the watchdog timer is disabled, drive the WDI pin to either GND or V_{CC} to ensure that there is no increase in I_{CC}. When SET is logic high, the watchdog operates normally. The SET pin can be changed dynamically; however, if the watchdog is going from disabled to enabled there is a 140μs (TYP) set-up time where the watchdog does not respond to changes on WDI, as shown in Figure 6.

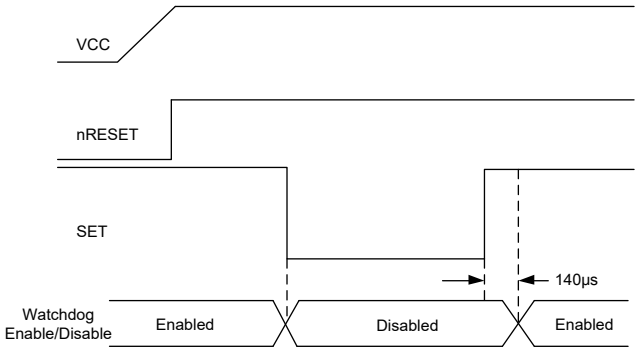


Figure 6. Enabling and Disabling the Watchdog

Device Functional Modes

Table 1 summarizes the functional modes of the SGM820.

Table 1. Device Functional Modes

V_{CC}	WDI	nWDO	nRESET
$V_{CC} < V_{POR}$	---	---	Undefined
$V_{POR} \le V_{CC} < V_{CC\_MIN}$	Ignored	High	Low
$V_{CC\_MIN} \le V_{CC} \le V_{ITN} + V_{HYS}$ (1)	Ignored	High	Low
$V_{CC} > V_{ITN}$ (2)	$t_{PULSE} < t_{WD\_MIN}$ (3)	High	High
$V_{CC} > V_{ITN}$ (2)	$t_{PULSE} > t_{WD\_MIN}$ (3)	Low	High

NOTES:
1. Only valid before V_{CC} has gone above $V_{ITN} + V_{HYS}$.
2. Only valid after V_{CC} has gone above $V_{ITN} + V_{HYS}$.
3. Where t_{PULSE} is the time between the falling edges on WDI.

V_{CC} is below V_{POR} ($V_{CC} < V_{POR}$)

When V_{CC} is less than V_{POR}, nRESET is undefined and can be either high or low. The state of nRESET largely depends on the load that the nRESET pin is experiencing.

Above Power-On-Reset, But Less than V_{CC_MIN}

($V_{POR} \le V_{CC} < V_{CC\_MIN}$)

When the voltage on V_{CC} is less than V_{CC_MIN}, and greater than or equal to V_{POR}, the nRESET signal is asserted (low). When nRESET is asserted, the watchdog output nWDO is in a high-impedance state regardless of the WDI signal that is input to the device.

Normal Operation ($V_{CC} \ge V_{CC\_MIN}$)

When V_{CC} is greater than or equal to V_{CC_MIN}, the nRESET signal is determined by V_{CC}. When nRESET is asserted, nWDO goes to a high-impedance state. nWDO is then pulled high through the pull-up resistor.

APPLICATION INFORMATION (1)

The following sections describe in detail proper device implementation, depending on the final application requirements.

CWD Functionality

The SGM820 features three options for setting the watchdog timer: connecting a capacitor to the CWD pin, connecting a pull-up resistor to V_{CC}, and leaving the CWD pin unconnected. Figure 7 shows a schematic drawing of all three options. If this pin is connected to V_{CC} through a 10kΩ pull-up resistor or left unconnected (high-impedance), then the factory-programmed watchdog timeouts are enabled; see the factory-programmed timing options section. Otherwise, the watchdog timeout can be adjusted by placing a capacitor from the CWD pin to ground.

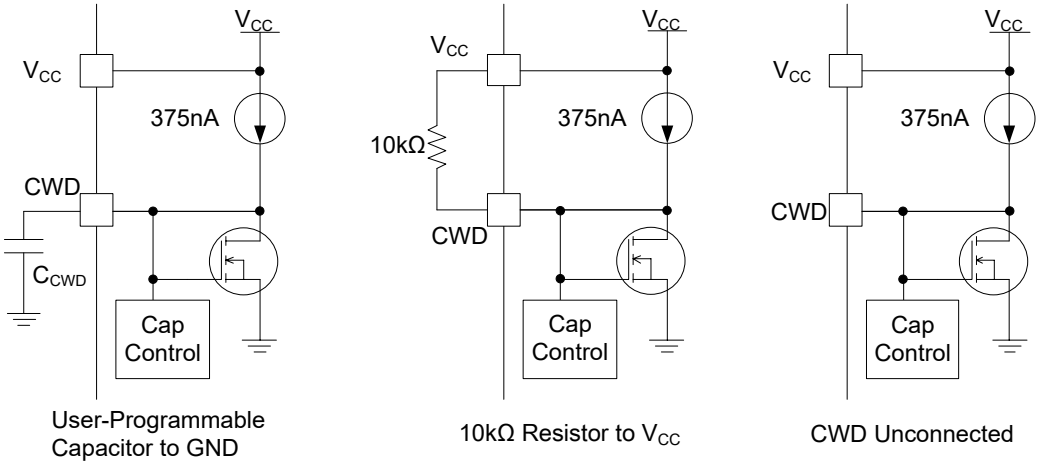


Figure 7. CWD Charging Circuit

Factory-Programmed Timing Options

If using the factory-programmed timing options (listed in Table 2), the CWD pin must either be unconnected or pulled up to V_{CC} through a 10kΩ pull-up resistor.

Table 2. Factory Programmed Watchdog Timing

Input		Standard and Extended Timing WDT (t_{WD})			UNITS
CWD	SET	MIN	TYP	MAX	
NC	0	Watchdog disabled			
NC	1	1360	1600	1840	ms
10kΩ to V_{CC}	0	Watchdog disabled			
10kΩ to V_{CC}	1	170	200	230	ms

Adjustable Capacitor Timing

Adjustable capacitor timing is achievable by connecting a capacitor to the CWD pin. If a capacitor is connected to CWD, then a 375nA, constant-current source charges C_{CWD} until V_{CWD} = 1.210V. The SGM820 determines the watchdog timeout with the formulas given in Equation 1 and Equation 2, where C_{CWD} is in nanofarads and t_{WD} is in milliseconds.

For standard versions SGM820A-X:

$$t_{WD\_standard}\,(ms) = 3.33 \times C_{CWD}\,(nF) + 0.28\,(ms) \quad (1)$$

For extended versions SGM820B-X:

$$t_{WD\_extended}\,(ms) = 78.3 \times C_{CWD}\,(nF) + 51\,(ms) \quad (2)$$

The SGM820 is designed and tested using C_{CWD} capacitors between 100pF and 1μF. Note that Equation 1 and Equation 2 are for ideal capacitors, and capacitor tolerances vary the actual device timing. For the most accurate timing, use ceramic capacitors with COG dielectric material. If a C_{CWD} capacitor is used, Equation 1 can be used to set t_{WD} for standard timing. Use Equation 2 to calculate t_{WD} for extended timing.

NOTE:

1. Information in the following applications sections is not part of the SGMICRO component specification, and SGMICRO does not warrant its accuracy or completeness. SGMICRO's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

APPLICATION INFORMATION (continued)

Overdrive Voltage

Forcing an nRESET is dependent on two conditions: the amplitude V_{CC} is beyond the trip point (ΔV_1 and ΔV_2), and the length of time that the voltage is beyond the trip point (t_1 and t_2). If the voltage is just under the trip point for a long period of time, nRESET asserts and the output is pulled low. However, if V_{CC} is just under the trip point for a few nanoseconds, nRESET does not assert and the output remains high. The length of time required for nRESET to assert can be changed by increasing the amount V_{CC} goes under the trip point. If V_{CC} is under the trip point by 10%, the amount of time required for the comparator to respond is much faster and causes nRESET to assert much quicker than when barely under the trip point voltage. Equation 3 shows how to calculate the percentage overdrive.

$$\text{Overdrive} = |(V_{CC}/V_{ITX} - 1) \times 100\%| \quad (3)$$

In Equation 3, V_{ITX} corresponds to the threshold trip point. If V_{CC} is exceeding the positive threshold, $V_{ITN} + V_{HYS}$ is used. V_{ITN} is used when V_{CC} is falling below the negative threshold. In Figure 8, t_1 and t_2 correspond to the amount of time that V_{CC} is over the threshold; the propagation delay versus overdrive for V_{ITN} and $V_{ITN} + V_{HYS}$ is illustrated, respectively.

The SGM820 is relatively immune to short positive and negative transients on V_{CC} because of the overdrive voltage curve.

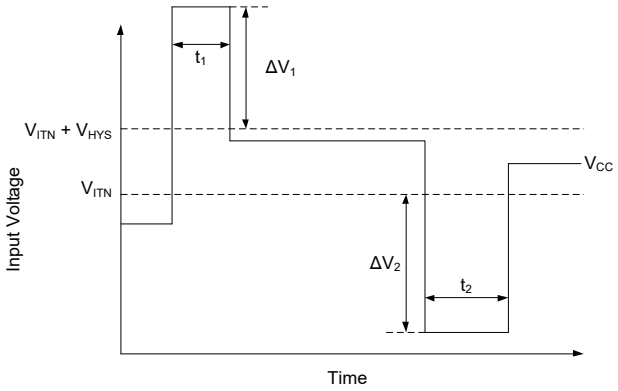


Figure 8. Overdrive Voltage

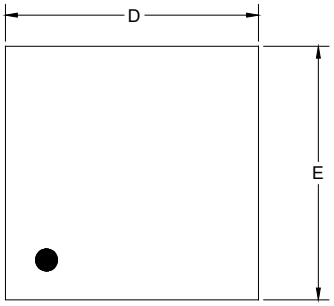
REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

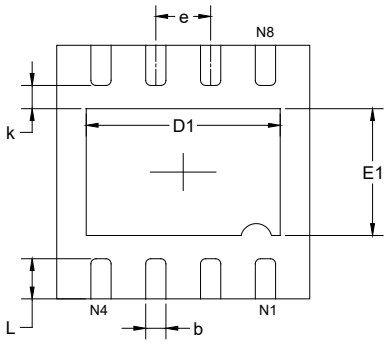
Changes from Original (JULY 2019) to REV.A	Page
Changed from product preview to production data	All

PACKAGE OUTLINE DIMENSIONS

TDFN-3×3-8L



TOP VIEW



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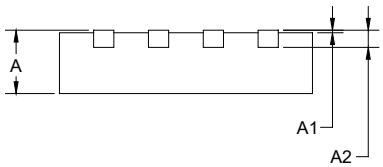
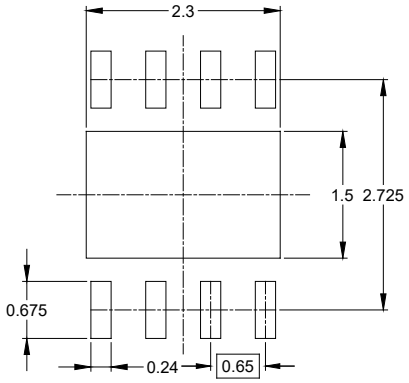


SIDE VIEW

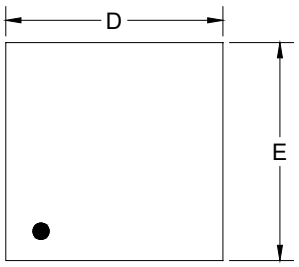


RECOMMENDED LAND PATTERN (Unit: mm)

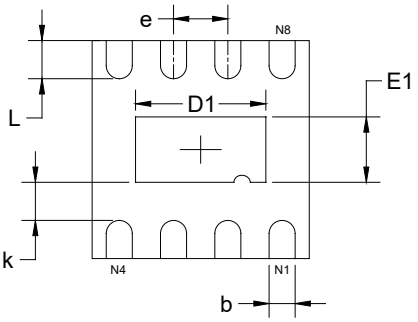
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.200	2.400	0.087	0.094
E	2.900	3.100	0.114	0.122
E1	1.400	1.600	0.055	0.063
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.650 TYP		0.026 TYP	
L	0.375	0.575	0.015	0.023

PACKAGE OUTLINE DIMENSIONS

TDFN-2×2-8L



TOP VIEW



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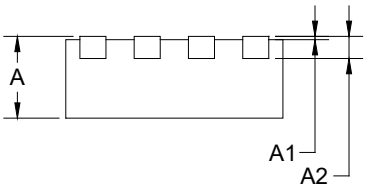
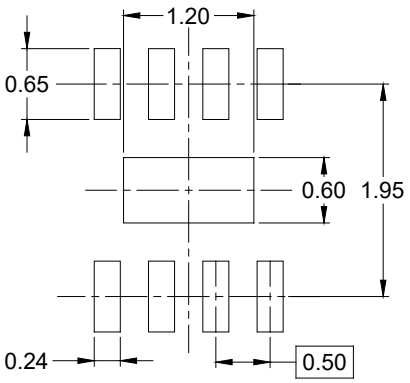


SIDE VIEW

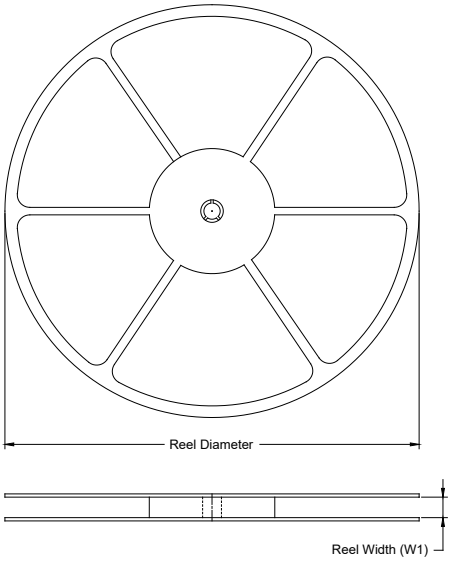


RECOMMENDED LAND PATTERN (Unit: mm)

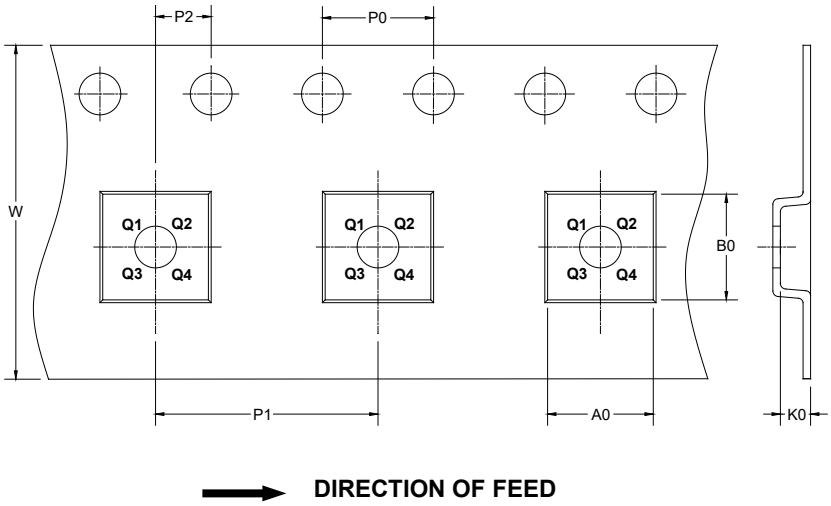
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	1.900	2.100	0.075	0.083
D1	1.100	1.300	0.043	0.051
E	1.900	2.100	0.075	0.083
E1	0.500	0.700	0.020	0.028
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.250	0.450	0.010	0.018

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



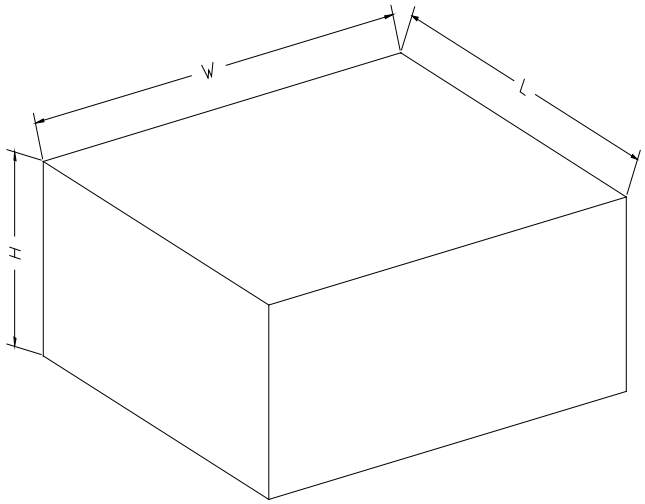
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
TDFN-3×3-8L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1
TDFN-2×2-8L	7″	9.5	2.30	2.30	1.10	4.0	4.0	2.0	8.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002