SGM42553
3A Triple 1/2-H-Bridge Driver

GENERAL DESCRIPTION

The SGM42553 provides three individually controllable half-H-bridge drivers. The device is intended to drive a three-phase brushless-DC motor, although it can also be used to drive solenoids or other loads. Each output driver channel consists of N-channel power MOSFETs configured in a 1/2-H-bridge configuration. Each 1/2-H-bridge driver has a dedicated ground terminal, which allows independent external current sensing.

An uncommitted comparator is integrated into the SGM42553, which allows for the construction of current-limit circuitry or other functions.

Internal protection functions are provided for under-voltage, charge pump faults, over-current, short-circuits, and over-temperature. Fault conditions are indicated by the nFAULT pin.

The SGM42553 is available in Green TQFN-6×6-36L and TSSOP-28 (Exposed Pad) packages.

FEATURES

- **Triple 1/2-H-Bridge Driver IC**
  - **3-Phase Brushless DC Motors**
  - **Solenoid and Brushed DC Motors**
- **High Current Drive Capability: 3A Peak**
- **Low MOSFET ON-Resistance**
- **Independent 1/2-H-Bridge Control**
- **Uncommitted Comparator Can Be Used for Current Limit or Other Functions**
- **Built-In 3.3V 10mA LDO Regulator**
- **8V to 60V Operating Supply Voltage Range**
- **Sleep Mode for Standby Operation**

APPLICATIONS

Camera Gimbals
HVAC Motors
Office Automation Machines
Factory Automation and Robotics

TYPICAL APPLICATION

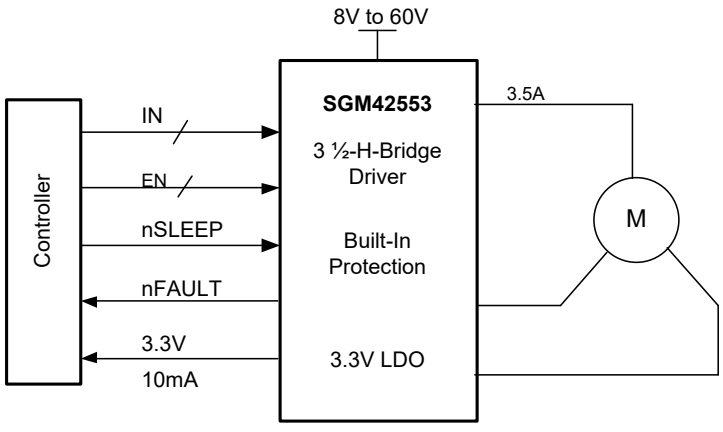


Figure 1. Simplified Schematic

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM42553	TSSOP-28 (Exposed Pad)				
	TQFN-6×6-36L				

MARKING INFORMATION

NOTE: X = Date Code. XX = Date Code. XXXXX = Date Code, Trace Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage, V_M ..... -0.3V to 65V
Power Supply Voltage Ramp Rate, V_M ..... 0V/μs to 2V/μs
Charge Pump Voltage, VCP, CPH..... -0.3V to V_M +12V
Charge Pump Negative Switching Pin, CPL ..... -0.3V to V_M
Internal Regulator Current Output, V3P3 ..... 0mA to 10mA
Internal Regulator Voltage, V3P3 ..... -0.3V to 3.8V
Control Pin Voltage, nRESET, nSLEEP, nFAULT, nCOMPO, ENx, INx..... -0.5V to 7V
Comparator Input-Voltage, COMPP, COMPN ..... -0.5V to 7V
Open-Drain Output Current, nFAULT, nCOMPO..... 0mA to 10mA
Continuous Phase Node Pin Voltage, OUTx ..... -0.7V to V_M +0.7V
Continuous 1/2-H-Bridge Source Voltage, PGNDx..... -600mV to 600mV
Peak Output Current, OUTx..... Internally limited
Junction Temperature.....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s).....+260℃
ESD

RECOMMENDED OPERATING CONDITIONS

Power Supply Voltage, V_M .....8V to 60V
Digital Pin Voltage, V_{IN}.....0V to 5.5V
Applied PWM signal on ENx, INx, f_{PWM}..... 0kHz to 250kHz
PGNDx Pin Voltage, V_{GNDX} ..... -500mV to 500mV
V3P3 Load Current, I_{V3P3} .....0mA to 10mA

NOTE: 1. V_{CLAMP} is used only to supply the clamp diodes. It is not a power supply input.

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

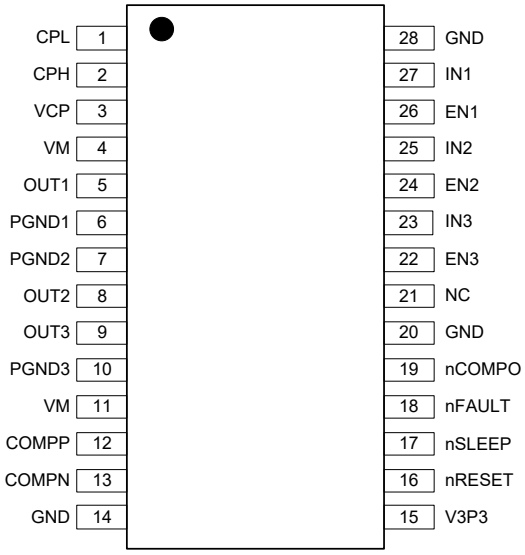
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

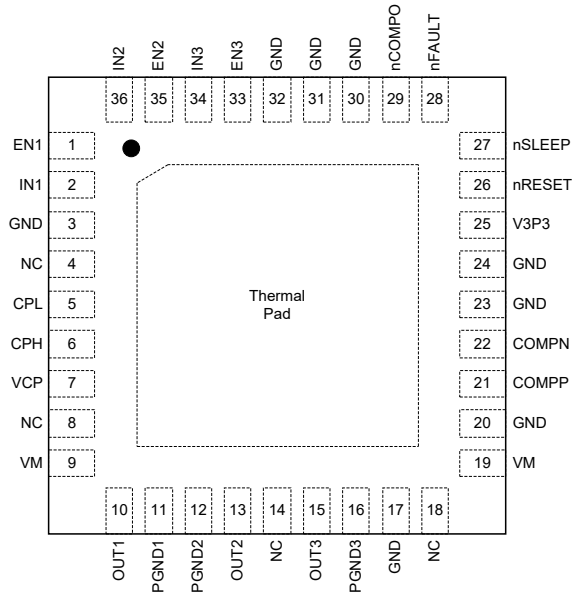
PIN CONFIGURATIONS

SGM42553 (TOP VIEW)



TSSOP-28 (Exposed Pad)

SGM42553 (TOP VIEW)



TQFN-6×6-36L

PIN DESCRIPTION

Pin			Type (1)	Description
Name	TSSOP-28 (Exposed Pad)	TQFN-6×6-36L		
COMPN	13	22	I	Comparator negative input. Uncommitted comparator input.
COMPP	12	21	I	Comparator positive input. Uncommitted comparator input.
CPL	1	5	PWR	Charge pump. Connect a VM rated, 0.01μF ceramic capacitor between CPH and CPL.
CPH	2	6	PWR	Charge pump. Connect a VM rated, 0.01μF ceramic capacitor between CPH and CPL.
EN1	26	1	I	Channel enable. Logic high enables the 1/2-H-bridge channel; internal pull-down.
EN2	24	35	I	Channel enable. Logic high enables the 1/2-H-bridge channel; internal pull-down.
EN3	22	33	I	Channel enable. Logic high enables the 1/2-H-bridge channel; internal pull-down.
GND	14, 20, 28	3, 17, 20, 23, 24, 30, 31, 32,	PWR	Device ground. Connect to system ground.
IN1	27	2	I	Channel input. Logic high pulls 1/2-H-bridge high, logic low pulls 1/2-H-bridge low; no effect when ENx is low; internal pull-down input.
IN2	25	36	I	Channel input. Logic high pulls 1/2-H-bridge high, logic low pulls 1/2-H-bridge low; no effect when ENx is low; internal pull-down input.
IN3	23	34	I	Channel input. Logic high pulls 1/2-H-bridge high, logic low pulls 1/2-H-bridge low; no effect when ENx is low; internal pull-down input.
NC	21	4, 8, 14, 18	NC	No internal connection. Recommended net given in block diagram (if any).
nCOMPO	19	29	OD	Comparator output. Uncommitted comparator output; open drain requires an external pull-up.
nFAULT	18	28	OD	Fault indication pin. Pulled logic-low with fault condition; open-drain output requires an external pull-up.
nRESET	16	26	I	Reset input. Active-low reset input initializes internal logic, clears faults, and disables the outputs, internal pull-down.

PIN DESCRIPTION (continued)

Pin			Type (1)	Description
Name	TSSOP-28 (Exposed Pad)	TQFN-6×6-36L		
nSLEEP	17	27	I	Sleep mode input. Logic high to enable device; logic low to enter low-power sleep mode; internal pull-down.
OUT1	5	10	O	Half-H-bridge output, connect to the load.
OUT2	8	13	O	Half-H-bridge output, connect to the load.
OUT3	9	15	O	Half-H-bridge output, connect to the load.
PGND1	6	11	PWR	Low-side FET source. Connect to GND or to low-side current-sense resistors.
PGND2	7	12	PWR	Low-side FET source. Connect to GND or to low-side current-sense resistors.
PGND3	10	16	PWR	Low-side FET source. Connect to GND or to low-side current-sense resistors.
V3P3	15	25	PWR	Internal regulator. Internal supply voltage; bypass to GND with a 6.3V, 0.47μF ceramic capacitor; up to 10mA external load.
VCP	3	7	PWR	Charge pump. Connect a 16V, 0.1μF ceramic capacitor to VM.
VM	4, 11	9, 19	PWR	Power supply. Connect to motor supply voltage; bypass to GND with two 0.1μF capacitors (for each pin) plus one bulk capacitor rated for VM.
Thermal pad			PWR	Must be connected to ground.

NOTE: I = input, O = output, OD = open-drain output, PWR = power, NC = no connect.

ELECTRICAL CHARACTERISTICS

(Typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supplies						
VM Operating Supply Current	I_{VM}	V_M = 24V, f_{PWM} < 50kHz		1	5	mA
VM Sleep-Mode Supply Current	I_{VMQ}	V_M = 24V		500	800	μA
Internal Regulator (V3P3)						
V3P3 Voltage	V_{3P3}	I_{OUT} = 0 to 10mA	3.1	3.3	3.52	V
Logic-Level Inputs (nSLEEP, ENx, INx)						
Input Low Voltage	V_{IL}			0.6	0.7	V
Input High Voltage	V_{IH}		2.2		5.25	V
Input Hysteresis	V_{HYS}		50		600	mV
Input Low Current	I_{IL}	V_{IN} = 0	-5		5	μA
Input High Current	I_{IH}	V_{IN} = 3.3V			100	μA
Pull-Down Resistance	R_{PD}			100		kΩ
Open-Drain Outputs (nFAULT and nCOMPO)						
Output Low Voltage	V_{OL}	I_O = 5mA			0.5	V
Output High Leakage Current	I_{OH}	V_O = 3.3V			1	μA
Comparator (COMPP, COMPN, nCOMPO)						
Input Common Mode Voltage Range	V_{CM}		0		5	V
Input Offset Voltage	V_{IO}		-7		7	mV
Input Bias Current	I_{IB}		-300		300	nA
Response Time	t_R	100mV step with 10mV overdrive			2	μs
H-Bridge FETs						
High-side FET On-Resistance	$R_{DS(on)}$	V_M = 24V, I_O = 1A, T_J = +25℃		0.2		Ω
		V_M = 24V, I_O = 1A, T_J = +85℃		0.25		
Low-side FET On-Resistance		V_M = 24V, I_O = 1A, T_J = +25℃		0.2		Ω
		V_M = 24V, I_O = 1A, T_J = +85℃		0.25		
Off-State Leakage Current	I_{OFF}		-2		2	μA
Protection Circuits						
VM Under-Voltage Lockout Voltage	V_{UVLO}	V_M rising		6.3	8	V
Over-Current Protection Trip Level	I_{OCP}		3.5	5		A
Over-Current Protection Deglitch Time	t_{OCP}			5		μs
Thermal Shutdown Temperature	T_{TSD}	Die temperature	150	160	180	℃
Thermal Shutdown Hysteresis	T_{HYS}	Die temperature		20		℃

TIMING REQUIREMENTS

(V_M = 24V, R_L = 20Ω, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t1	Delay time, ENx high to OUTx high	INx = 1	130		330	ns
t2	Delay time, ENx low to OUTx low	INx = 1	275		475	ns
t3	Delay time, ENx high to OUTx low	INx = 0	100		300	ns
t4	Delay time, ENx low to OUTx high	INx = 0	200		400	ns
t5	Delay time, INx high to OUTx high	ENx = 1	300		500	ns
t6	Delay time, INx low to OUTx low	ENx = 1	275		475	ns
t_r	Output rise time, resistive load to GND		30		150	ns
t_f	Output fall time, resistive load to GND		30		150	ns
t_{DEAD} (1)	Output dead time			90		ns

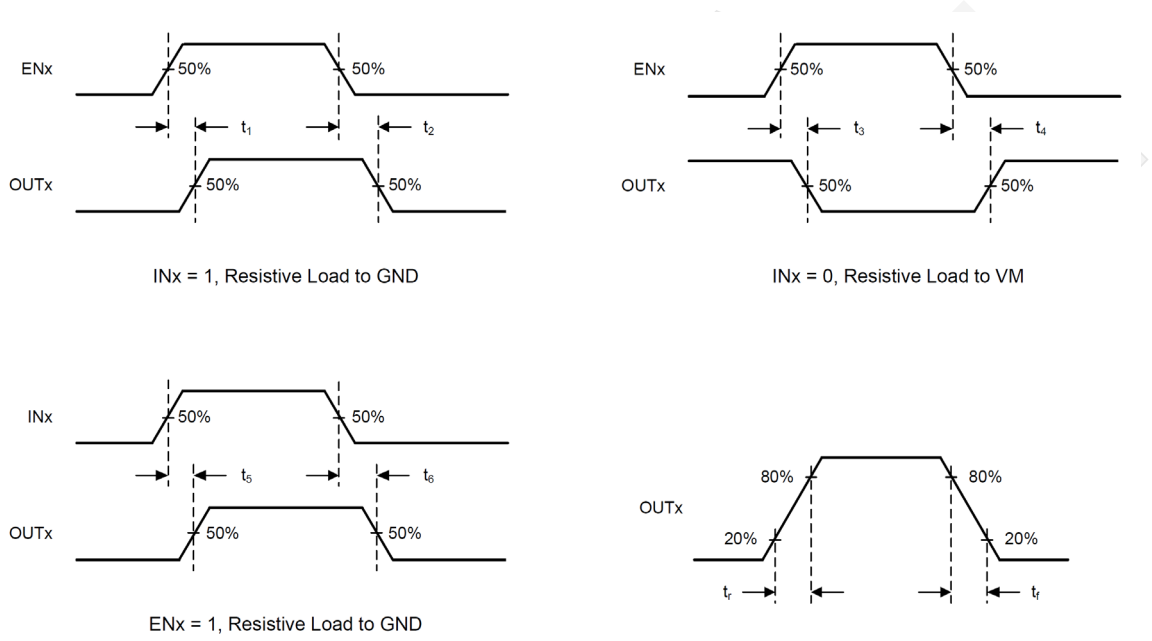


Figure 2. SGM42553 Switching Characteristics

TYPICAL APPLICATION CIRCUITS

The SGM42553 can be used to drive brushless-DC motors, brushed-DC motors, and solenoid loads. The following design procedure can be used to configure the SGM42553.

Three-Phase Brushless-DC Motor Control

In this application, the SGM42553 is used to drive a brushless-DC motor.

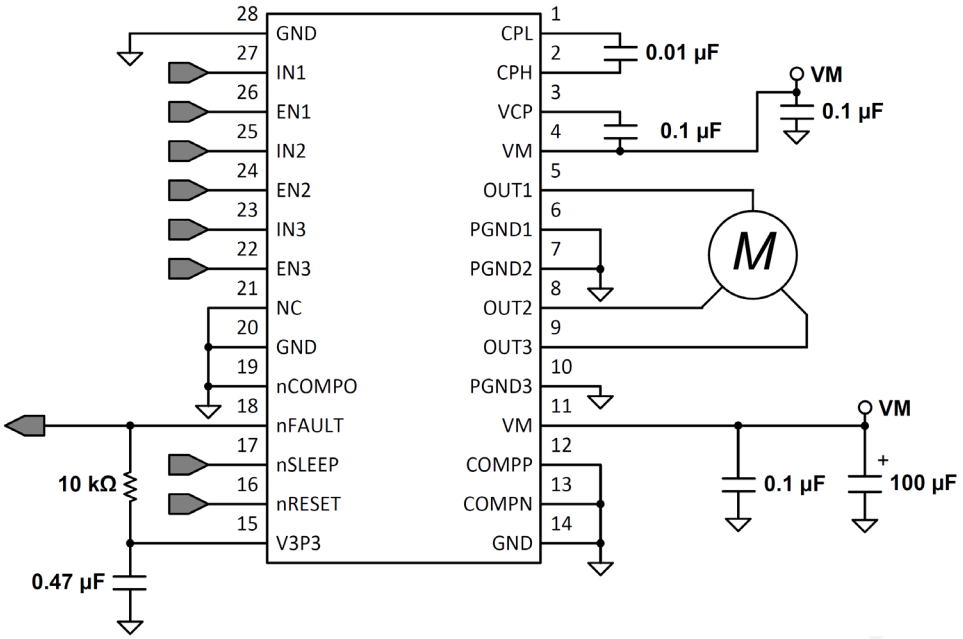


Figure 3. BLDC Driver Application Schematic

Design Requirements

Table 1 gives design input parameters for system design.

Table 1. Design Parameters

Design Parameter	Reference	Example Value
Typical Supply Voltage	V_M	18V
Maximum Voltage	VM_{MAX}	36V
Target rms Current	I_{RMS}	1.2A
Motor Winding Resistance	M_R	0.5Ω
Motor Winding Inductance	M_L	0.28mH
Motor Poles	M_P	16 poles
Motor Rated RPM	M_{RPM}	4000 RPM
PWM Frequency	f_{PWM}	25kHz

Motor Voltage

Brushless-DC motors are typically rated for a certain voltage (for example 12V and 24V). Operating a motor at a higher voltage corresponds to a lower drive current to obtain the same motor power. A higher operating voltage also corresponds to a higher obtainable rpm. SGM42553 allows for the use of higher operaing voltage because of a maximum V_M rating of 60V.

Operating at lower voltages generally allows for more accurate control of phase currents. The SGM42553 functions down to a supply of 8V.

TYPICAL APPLICATION CIRCUITS (continued)

Motor Commutation

The SGM42553 can drive both trapezoidal (120°) and sinusiodal (180°) commutation due to independent control of each of the three 1/2-H-bridges.

Both synchronous and asynchronous rectification are supported. Synchronous rectification is achieved by applying a pulse-width-modulated (PWM) input signal to the INx pins while driving. The user can also implement asynchronous rectification by applying the PWM signal to the ENx inputs.

Table 2. Trapezoidal (120°) Commutation States

State	OUT1 (Phase U)			OUT2 (Phase V)			OUT3 (Phase W)		
	IN1	EN1	OUT1	IN2	EN2	OUT2	IN3	EN3	OUT3
1	X	0	Z	1	1	H	0	1	L
2	1	1	H	X	0	Z	0	1	L
3	1	1	H	0	1	L	X	0	Z
4	X	0	Z	0	1	L	1	1	H
5	0	1	L	X	0	Z	1	1	H
6	0	1	L	1	1	H	X	0	Z
Brake	0	1	L	0	1	L	0	1	L
Coast	X	0	Z	X	0	Z	X	0	Z

Application Curve

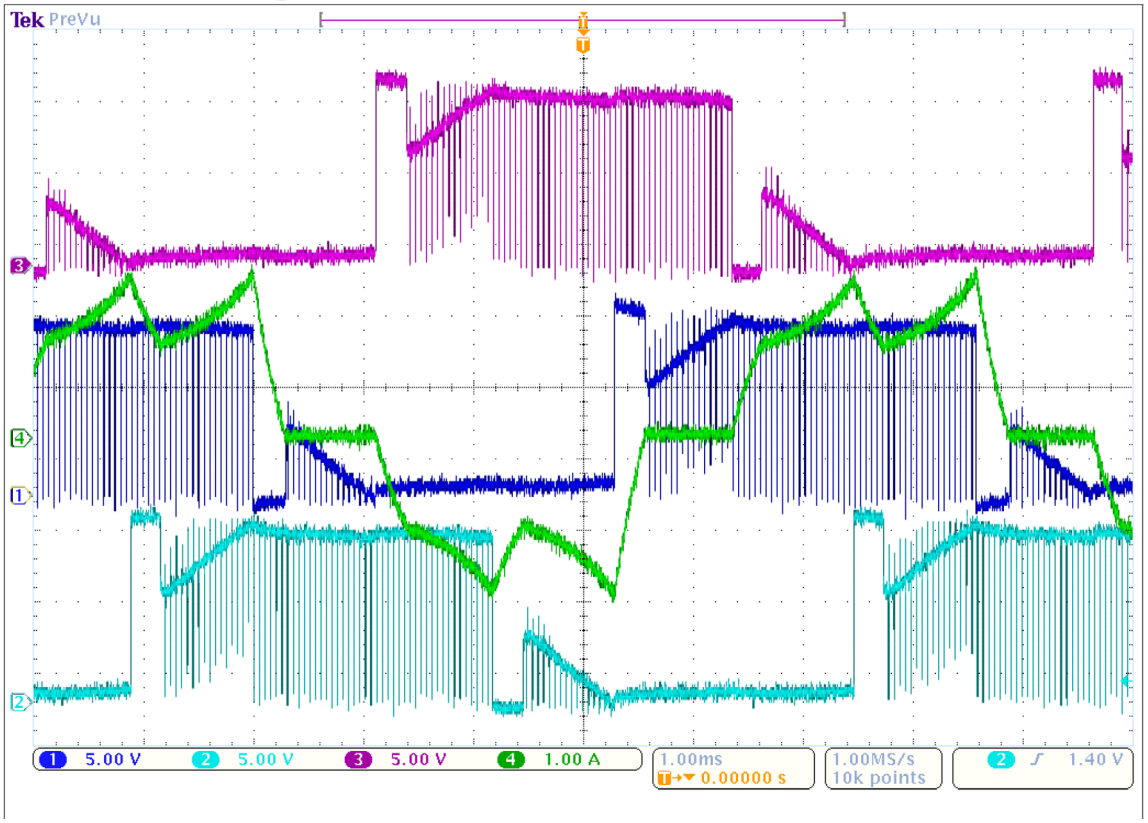


Figure 4. Driving a BLDC Motor

TYPICAL APPLICATION CIRCUITS (continued)

Three-Phase Brushless-DC Motor Control with Current Monitor

In this application, the SGM42553 is used to drive a brushless-DC motor and the uncommitted comparator is used to monitor the motor current.

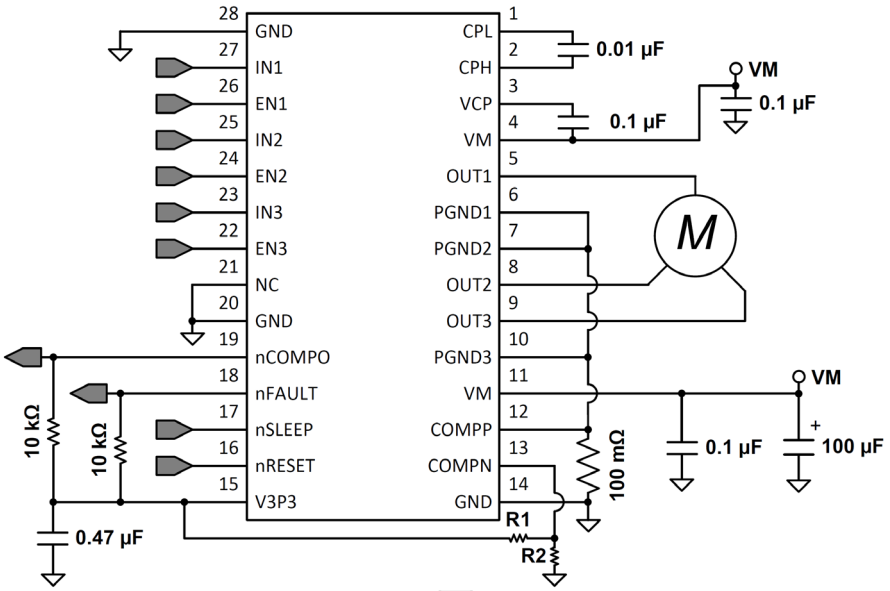


Figure 5. Uncommitted Comparator Used As a Current Monitor

Design Requirements

Table 3 gives design input parameters for system design.

Table 3. Design Parameters

Design Parameter	Reference	Example Value
Trip Current	I_{TRIP}	3A

Trip Current

The uncommitted comparator is configured such that the negative input COMPN is connected to the PGNDx pins. A sense resistor is placed from the PGNDx/COMPN pins to GND.

The voltage on the COMPP pin will set the current monitor trip threshold. In this case, the the nCOMPO pin will change state when COMPP and COMPN have the same potential.

$$I_{TRIP}(A)=\frac{COMPN(V)}{R_{SENSE}(\Omega)} \quad (1)$$

Example: If the desired trip current is 3A
Set R_{SENSE} = 200mΩ
COMPN would have to be 0.6V.
Create a resistor divider from V3P3 (3.3V) to set COMPN ≈ 0.6V.
Set R2 = 10kΩ, set R1 = 56kΩ

Sense Resistor

For optimal performance, the sense resistor must have the following characteristics:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{rms}^2 \times R$. For example, if the rms motor current is 1A and a 200mΩ sense resistor is used, the resistor will dissipate $1A^2 \times 0.2\Omega = 0.2W$. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. Measuring the actual sense-resistor temperature in a final system, along with the power MOSFETs, is always best because these are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, using multiple standard resistors in parallel, between the sense node and ground is a common practice. This configuration distributes the current and heat dissipation.

TYPICAL APPLICATION CIRCUITS (continued)

Brushed-DC and Solenoid Load

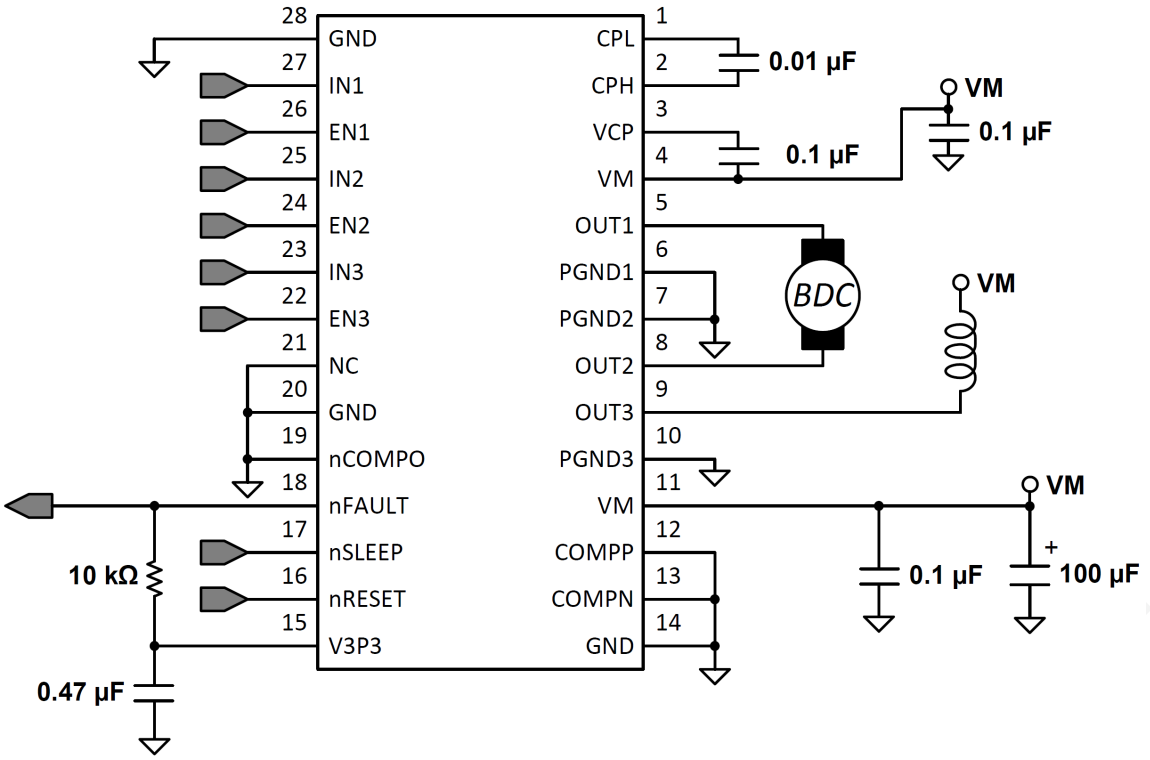


Figure 6. Brushed-DC and Solenoid Schematic

Design Requirements

Table 4 gives design input parameters for system design.

Table 4. Design Parameters

Design Parameter	Reference	Example Value
Brushed Motor rms Current	$I_{RMS, BDC}$	1.0A
Brushed Motor Peak Current	$I_{PEAK, BDC}$	2.0A
Solenoid rms Current	$I_{RMS, SOL}$	0.5A
Solenoid Peak Current	$I_{PEAK, SOL}$	1.0A

Detailed Design Procedure

Table 5. Brushed-DC Control

Function	IN1	EN1	IN2	EN2	OUT1	OUT2
Forward	1	1	0	1	H	L
Reverse	0	1	1	1	L	H
Brake (low-side Slow Decay)	0	1	0	1	L	L
High-side Slow Decay	1	1	1	1	H	H
Coast	X	0	X	0	Z	Z

Table 6. Solenoid Control (High-side Load)

Function	IN3	EN3	OUT3
Coast/Off	X	0	Z
On	0	1	L
Brake	1	1	H

TYPICAL APPLICATION CIRCUITS (continued)

Three Solenoid Loads

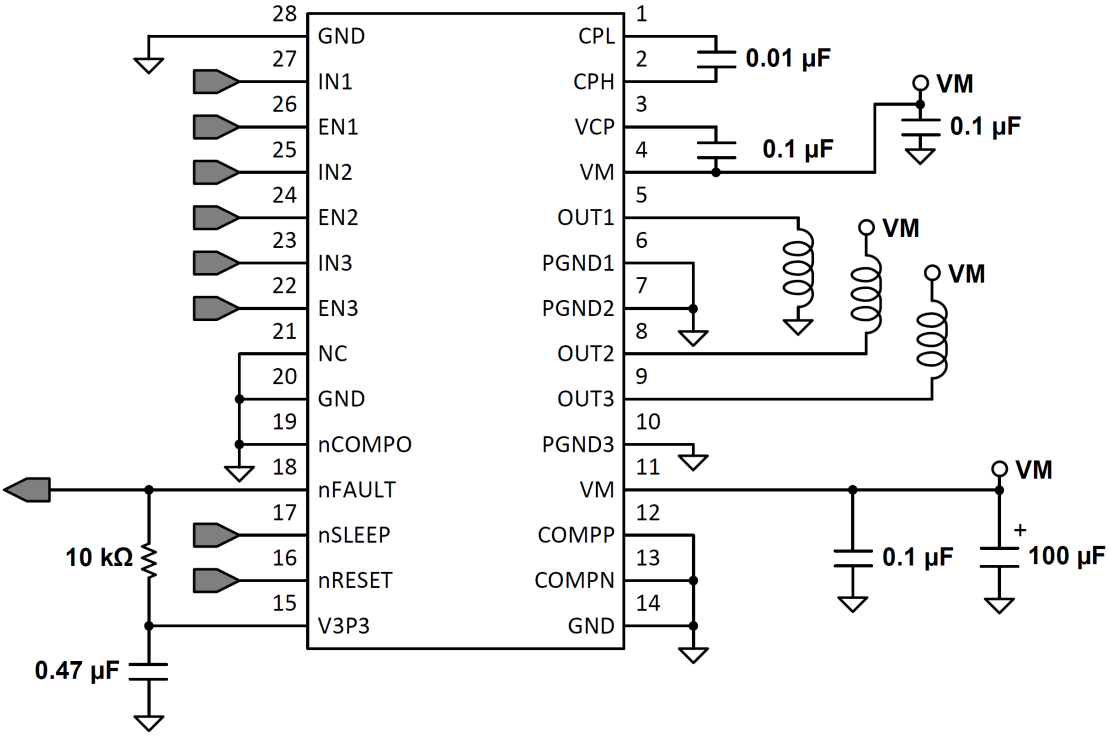


Figure 7. Three Independent Load Connections Schematic

Design Requirements

Table 7gives design input parameters for system design.

Table 7. Design Parameters

Design Parameter	Reference	Example Value
Solenoid rms Current	$I_{RMS, SOL}$	1.0 A
Solenoid Peak Current	$I_{PEAK, SOL}$	1.5 A

Detailed Design Procedure

Table 8. Solenoid Control (High-side Load)

Function	IN2	EN2	OUT2
Coast/Off	X	0	Z
On	0	1	L
Brake	1	1	H

Table 9. Solenoid Control (Low-side Load)

Function	IN1	EN1	OUT1
Coast/Off	X	0	Z
On	1	1	H
Brake	0	1	L

FUNCTIONAL BLOCK DIAGRAM

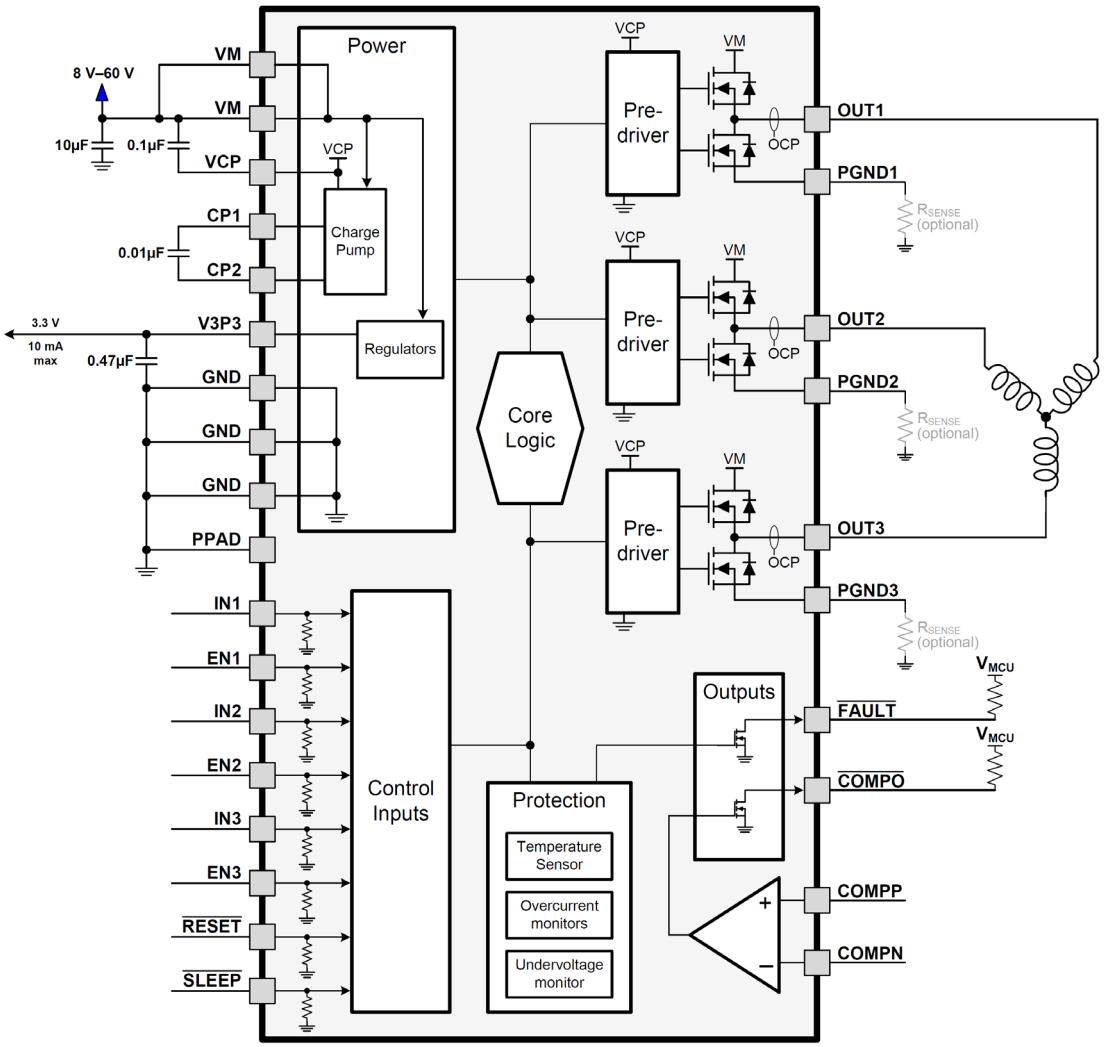


Figure 8. Block Diagram

DETAILED DESCRIPTION

Overview

The SGM42553 integrates three independent 3A half-H bridges, protection circuits, sleep mode, fault reporting, and a comparator. The single power supply supports a wide 8V to 60V range, making it well-suited for motor drive applications.

Output Stage

The SGM42553 contains three half-H-bridge drivers. The source terminals of the low-side FETs of all three half-H-bridges terminate at separate pins (PGND1, PGND2, and PGND3) to allow the use of a low-side current sense resistor on each output, if desired. The user can also connect all three together to a single low-side sense resistor, or can connect them directly to ground if current sensing is unneeded.

If using a low-side sense resistor, ensure that the voltage on the PGND1, PGND2, or PGND3 pin does not exceed ±500mV.

The device has two V_M motor power-supply pins. Connect both V_M pins together to the motor supply voltage.

Bridge Control

The INx input pins directly control the state (high or low) of the OUTx outputs; the ENx input pins enable or disable the OUTx driver. Table 10 shows the logic:

Table 10. Logic States

INx	ENx	OUTx
X	0	Z
0	1	L
1	1	H

Charge Pump

Because the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to enhance the high-side FETs fully. The SGM42553 integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose.

The charge pump requires two external capacitors for operation. See the block diagram and pin descriptions for details on these capacitors (value, connection, and so forth). The charge pump shuts down when nSLEEP is low.

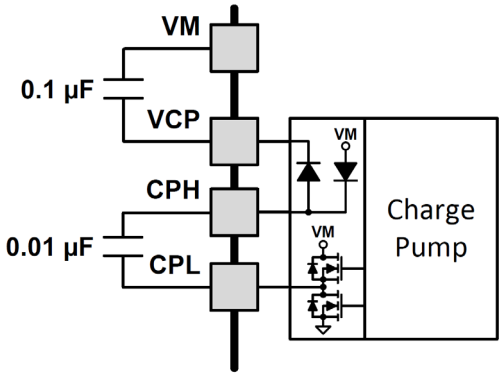


Figure 9. SGM42553 Charge Pump

Comparator

The SGM42553 includes an uncommitted comparator, which can find use as a current-limit comparator or for other purposes.

Figure 10 shows connections to use the comparator to sense current for implementing a current limit. Current from all three low-side FETs is sensed using a single low-side sense resistor. The voltage across the sense resistor is compared with a reference, and when the sensed voltage exceeds the reference, a current limit condition is signaled to the controller. The V3P3 internal voltage regulator can be used to set the reference voltage of the comparator.

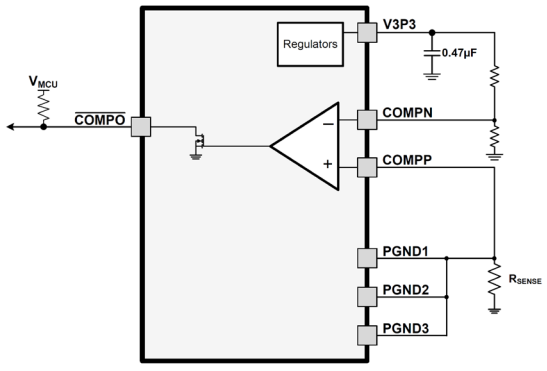


Figure 10. Comparator as Current Monitor

DETAILED DESCRIPTION (continued)

Protection Circuits

The SGM42553 has full protection against under-voltage, over-current, and over-temperature events.

Under-Voltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the under-voltage threshold voltage (V_{UVLO}), all FETs in the H-bridge will be disabled, the charge pump will be disabled, the internal logic is reset, and the nFAULT pin will be driven low. Operation will resume when VM rises above the UVLO threshold. The nFAULT pin will be released after operation has resumed.

Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume. The nFAULT pin will be released after operation has resumed.

Over-Current Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than t_{OCP}, the device disables the channel experiencing the overcurrent and drives the nFAULT pin low. The driver remains off until either assertion of nRESET or the cycling of VM power.

Over-current conditions on both high- and low-side devices, that is, a short to ground, supply, or across the motor winding, all result in an over-current shutdown.

Table 11. Fault Condition Summary

Fault	Condition	Error Report	H-Bridge	Charge Pump	V3P3	Recovery
VM Under-Voltage (UVLO)	$V_M < V_{UVLO}$ (max 8V)	nFAULT	Disabled	Disabled	Operating	$V_M > V_{UVLO}$ (max 8V)
Thermal Shutdown (T_{SD})	$T_J > T_{TSD}$ (min 150°C)	nFAULT	Disabled	Operating	Operating	$T_J < T_{TSD} - T_{HYS}$ (T_{HYS} typ 20°C)
Over-Current (OCP)	$I_{OUT} > I_{OCP}$ (min 3A)	nFAULT	Disabled	Operating	Operating	nRESET

Device Functional Modes

The SGM42553 is active unless the nSLEEP pin is brought logic low. In sleep mode the charge pump is disabled, the output FETs are disabled Hi-Z, and the V3P3 regulator is disabled. The SGM42553 is brought out of sleep mode automatically if nSLEEP is brought logic high.

nRESET and nSLEEP Operation

The nRESET pin, when driven low, resets any faults. It also disables the output drivers while it is active. The device ignores all inputs while nRESET is active. Note that there is an internal power-up-reset circuit, so that driving nRESET at power up is not required.

Driving nSLEEP low puts the device into a low-power sleep state. Entering this state disables the output drivers, stops the gate-drive charge pump, resets all internal logic (including faults), and stops all internal clocks. In this state, the device ignores all inputs until nSLEEP returns inactive-high. When returning from sleep mode, some time (approximately 1ms) must pass before the motor driver becomes fully operational. The V3P3 regulator remains operational in sleep mode.

Table 12. Functional Modes Summary

Fault	Condition	H-Bridge	Charge Pump	V3P3
Operating	8V < V_M < 60V nSLEEP pin = 1	Operating	Operating	Operating
Sleep Mode	8V < V_M < 60V nSLEEP pin = 0	Disabled	Disabled	Disabled
Fault Encountered	V_M Under-Voltage (UVLO)	Disabled	Disabled	Operating
	Over-Current (OCP)	Disabled	Operating	Operating
	Thermal Shutdown (TSD)	Disabled	Operating	Operating

APPLICATION INFORMATION

Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The datasheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

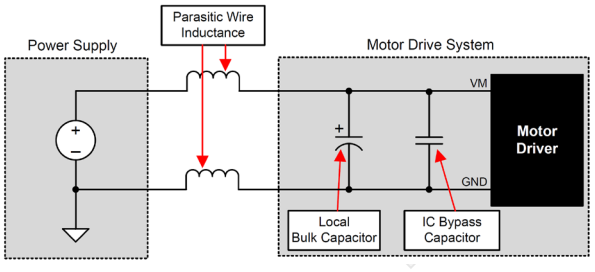
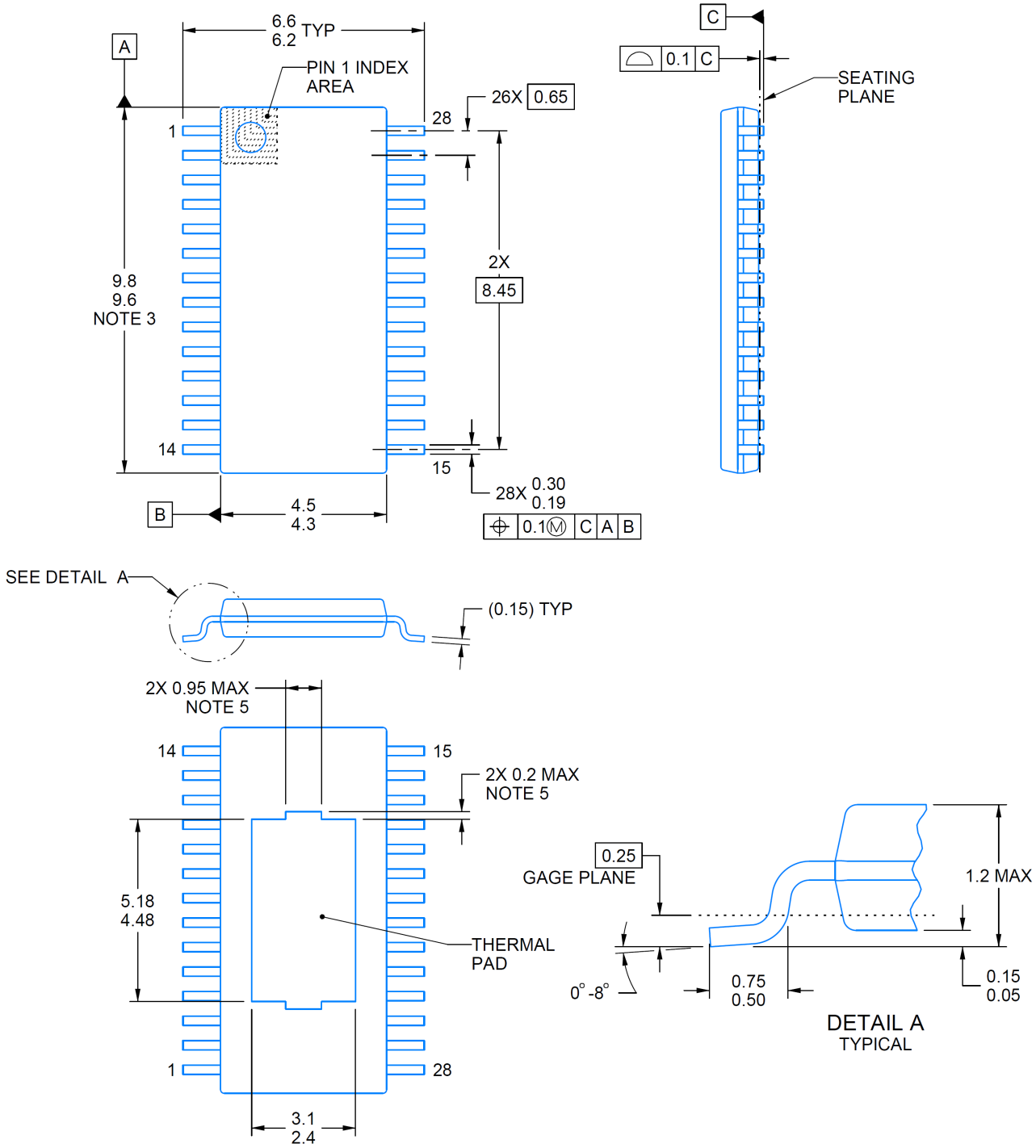


Figure 11. Example Setup of Motor Drive System with External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

PACKAGE OUTLINE DIMENSIONS

TSSOP-28 (Exposed Pad)



PACKAGE OUTLINE DIMENSIONS

TQFN-6×6-36L