

## Wide Vin 65V Non-synchronous Boost/Flyback/SEPIC Controller

### FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C
  - Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H2
  - Device CDM ESD Classification Level C3B
- Wide Input Voltage Range: 2.92V-60V
- Low Shutdown Current 3.9uA
- Low Quiescent Operating Current: 470uA
- +/- 1.5% Feedback Reference Voltage
- Adjustable Switching Frequency: 100KHz to 2.2MHz
- Integrated Frequency Dither for EMI Mitigation
- External Frequency Synchronic
- External Compensation
- Pulse Skipping Mode
- Supports additional Slope Compensation
- 14ms Internal Soft-start Time
- Integrated Protection Feature
  - Constant Peak-Current Protection Threshold Over Input Voltage
  - Output Overvoltage Protection
  - Adjustable Under-voltage Lockout
  - Hiccup Over Load Protection
  - Thermal Shutdown Protection:165°C
- MSOP-10L(3mm\*3mm)

### APPLICATIONS

- Muti-output Flyback
- LED Bias Supply
- Portable Speaker Supply
- Battery Powered Boost/Flyback/SEPIC application

### DESCRIPTION

The SCT81621Q device is a wide input, non-synchronous boost controller. The device can be used in Boost, SEPIC and Flyback converters.

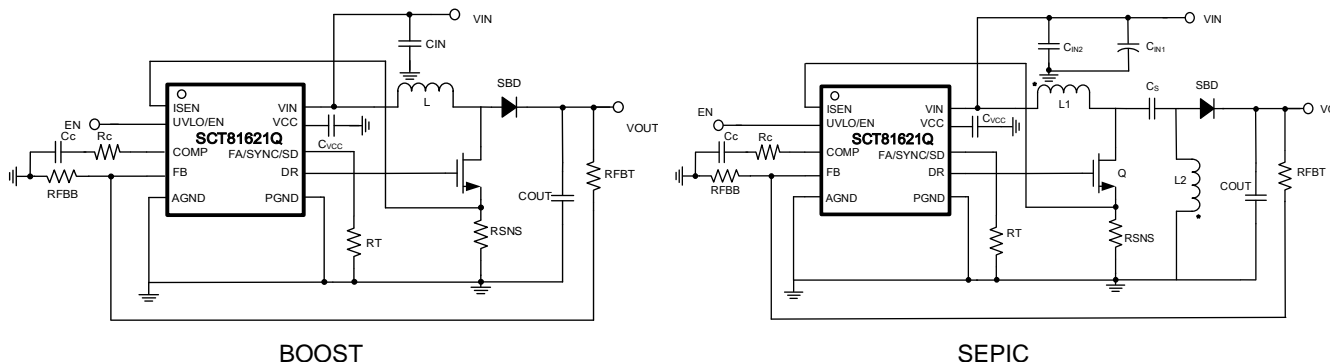
The switching frequency of the SCT81621Q device can be adjusted to any value between 100kHz and 2.2MHz by using a single external resistor or by synchronizing it to an external clock. Current mode control provides superior bandwidth and transient response in addition to cycle-by-cycle current limiting. Current limit is adjustable through an external resistor.

The SCT81621Q is an Electromagnetic Interference (EMI) friendly controller with implementing optimized design for EMI reduction. The SCT81621Q features Frequency Spread Spectrum (FSS) with  $\pm 6\%$  jittering span of the switching frequency and modulation rate 1/512 of switching frequency to reduce the conducted EMI.

The SCT81621Q device has built-in protection features such as thermal shutdown, short-circuit protection and overvoltage protection. Power-saving shutdown mode reduces the total supply current to 3.9  $\mu$ A. Integrated current slope compensation simplifies the design and, if needed for specific applications, can be increased using a single resistor.

The device is available in a MSOP-10L(3mm\*3mm) Package.

### TYPICAL APPLICATION



# SCT81621Q

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version

Revision 0.6: Customer Preview

Revision 0.81: Customer Sample

Revision 0.82: Update hiccup function

## DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT81621QMRD	1621Q	10-Lead 3mmx3mm Plastic MSOP

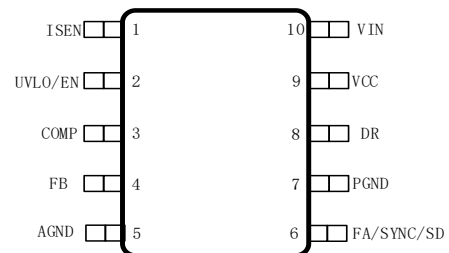
1) For Tape & Reel, Add Suffix R (e.g. SCT81621QMRDR)

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted<sup>(1)</sup>

DESCRIPTION	MIN	MAX	UNIT
VIN, UVLO_EN	-0.3	65	V
VCC, DR	-1	6.6	V
ISEN, COMP, FB, FA/SYNC/SD	-5	5.5	V
Peak Driver Output Current		1 <sup>(2)</sup>	A
Junction temperature <sup>(2)</sup>	-40	150	°C
Storage temperature T <sub>STG</sub>	-65	150	°C

## PIN CONFIGURATION



- (1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
- (2) Guaranteed by design, not tested in productions.
- (3) The IC includes over temperature protection to protect the device during overload conditions. Junction temperature will exceed 170°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

## PIN FUNCTIONS

NAME	NO.	DESCRIPTION
ISEN	1	Current sense input pin. Connect to the positive side of the current sense resistor through a short path.
UVLO_EN	2	Undervoltage lockout programming pin. The converter start-up and shutdown levels can be programmed by connecting this pin to the supply voltage through a resistor divider. This pin must not be left floating. Connect to VIN pin if not used.
COMP	3	Output of the internal transconductance error amplifier. Connect the loop compensation components between this pin and ground.
FB	4	Inverting input of the error amplifier. Connect a voltage divider from the output to this pin to set output voltage. The device regulates FB voltage to the internal reference value of 1.275V typical.
AGND	5	Analog ground pin.

FA/SYNC/SD	6	Switching frequency setting pin. The switching frequency is programmed by a single resistor between this pin and AGND. The internal clock can be synchronized to an external clock. A high level on this pin for $\geq 30 \mu\text{s}$ will turn the device off and the device will then draw $3.9 \mu\text{A}$ from the supply typically.
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**PIN FUNCTIONS (continued)**

NAME	NO.	DESCRIPTION
PGND	7	Power ground pin.
DR	8	N-channel MOSFET gate drive output. Connect directly to the gate of the N-channel MOSFET through a short, low inductance path.
VCC	9	Output of the internal VCC regulator and supply voltage input of the MOSFET driver. Connect a ceramic bypass capacitor from this pin to PGND.
VIN	10	Power supply input pin.

**RECOMMENDED OPERATING CONDITIONS**

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
$V_{\text{IN}}$	Input voltage range	2.92	60	V
$V_{\text{CC}}$	VCC voltage range	2.92	6.1	V
$T_{\text{J}}$	Operating junction temperature	-40	125	°C

**ESD RATINGS**

PARAMETER	DEFINITION	MIN	MAX	UNIT
$V_{\text{ESD}}$	Human Body Model(HBM), per AEC-Q100-002	-2	+2	kV
	Charged Device Model(CDM), per AEC-Q100-011	-1	+1	kV

**THERMAL INFORMATION**

PARAMETER	THERMAL METRIC	MSOP-10	UNIT
$R_{\theta\text{JA}}$	Junction to ambient thermal resistance <sup>(1)</sup>	142.3	°C/W
$R_{\theta\text{JC (top)}}$	Junction to case (top) thermal resistance <sup>(1)</sup>	64.6	
$R_{\theta\text{JB}}$	Junction to board thermal resistance <sup>(1)</sup>	97.3	

(1) SCT provides  $R_{\theta\text{JA}}$  and  $R_{\theta\text{JC}}$  numbers only as reference to estimate junction temperatures of the devices.  $R_{\theta\text{JA}}$  and  $R_{\theta\text{JC}}$  are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT81621Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT81621Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual  $R_{\theta\text{JA}}$  and  $R_{\theta\text{JC}}$ .

# SCT81621Q

## ELECTRICAL CHARACTERISTICS

V<sub>IN</sub>=12V, T<sub>J</sub>=-40°C~125°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>Power Supply and Output</b>						
V <sub>IN</sub>	Operating input voltage		2.92		60	V
V <sub>IN_UVLO</sub>	Input UVLO Hysteresis	V <sub>IN</sub> rising		2.9 160		V mV
I <sub>SD</sub>	Shutdown current	V <sub>FA/SYCN/SD</sub> =5V or V <sub>UVLO_EN</sub> =0		3.9	5	uA
I <sub>Q</sub>	Quiescent current from VIN	no load, no switching		470		uA
<b>VCC Power</b>						
V <sub>CC</sub>	Internal linear regulator			6.1		V
V <sub>CC_uvlo</sub>				2.92		V
V <sub>CC_uvlo_hys</sub>				80		mV
I <sub>VCC</sub>	VCC Sourcing current limit		20	65		mA
<b>UVLO/EN</b>						
V <sub>UVLOSEN</sub>	Under voltage Lockout reference voltage	V <sub>UVLO</sub> ramping up		1.43		V
I <sub>UVLO</sub>	UVLO source current		3.8	4.75	5.7	uA
V <sub>UVLOSD</sub>	UVLO shut down voltage	V <sub>UVLO</sub> ramping down		0.683		V
<b>Reference and Control Loop</b>						
V <sub>REF</sub>	Reference voltage of FB			1.275		V
I <sub>FB</sub>	FB pin leakage current	V <sub>FB</sub> =1V			100	nA
G <sub>EA</sub>	Error amplifier trans-conductance	V <sub>COMP</sub> =1.5V	320	390	460	uS
I <sub>COMP_SRC</sub>	Error amplifier maximum source current	V <sub>FB</sub> =V <sub>REF</sub> -200mV, V <sub>COMP</sub> =1.5V	340	535	710	uA
I <sub>COMP_SNK</sub>	Error amplifier maximum sink current	V <sub>FB</sub> =V <sub>REF</sub> +200mV, V <sub>COMP</sub> =1.5V	-135	-95	-50	uA
V <sub>COMP_H</sub>	COMP high clamp	V <sub>FB</sub> =0.8V		2.55		V
V <sub>COMP_L</sub>	COMP low clamp	V <sub>FB</sub> =1.7V		0.88		V
<b>Gate Driver</b>						
R <sub>DS(on)_TOP</sub>	Driver switch on resistance(top)			4.5		Ω
R <sub>DS(on)_LOW</sub>	Driver switch on resistance(bottom)			2		Ω
<b>Current Sense</b>						
V <sub>sense</sub>	Current sense threshold		124	145.5	167	mV
V <sub>SL</sub>	Internal compensation Ramp voltage			90		mV
C <sub>HICC-DEL</sub>	Hiccup mode activation delay	Clock cycles with current limiting before hiccup off-time activated (SS_done)		64		cycles
C <sub>HICCUP</sub>	Hiccup mode off-time after activation	Clock cycles with no switching followed by SS release		32768		cycles

**ELECTRICAL CHARACTERISTICS (continued)**

$V_{IN}=12V$ ,  $T_J=-40^{\circ}C\sim 125^{\circ}C$ , typical values are tested under  $25^{\circ}C$ .

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>Soft start</b>						
$T_{SS}$	Soft-start Time			14		ms
<b>Switching Frequency</b>						
$F_{SW}$	Switching frequency	$R_{FA/SYNC/SD}=47.5k\Omega$	360	400	440	kHz
$V_{SYN\_HI}$	Threshold for Synchronization on FA/SYNC/SD pin	Synchronization voltage rising		1.27		V
$V_{SYN\_LO}$		Synchronization voltage falling		0.582		V
$t_{ON\_MIN}$	Minimum on-time	$F_{sw}=400kHz$		250		ns
<b>Protection</b>						
$V_{OVTH}$	FB overvoltage threshold	FB rising		85		mV
		FB falling		15		mV
$T_{SD}$	Thermal shutdown threshold	$T_J$ rising		165		$^{\circ}C$
	Hysteresis			15		$^{\circ}C$

## TYPICAL CHARACTERISTICS

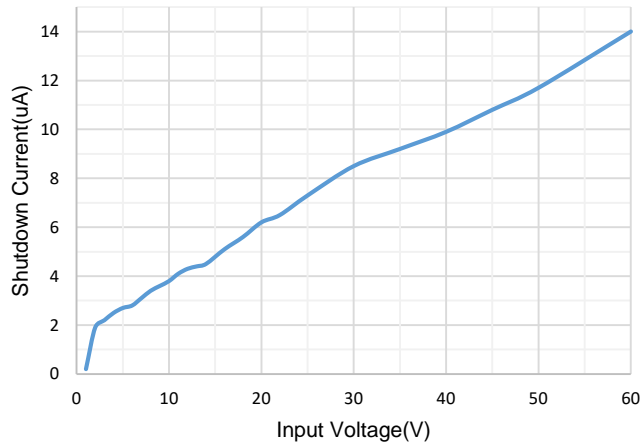


Figure 1. ISD vs Input Voltage

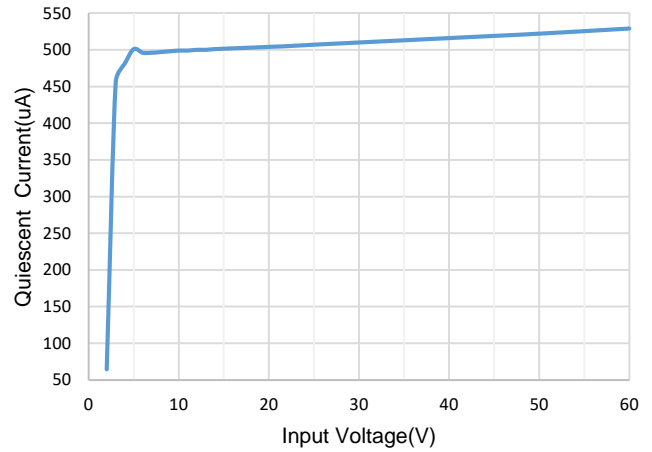


Figure 2. IQ vs Input Voltage

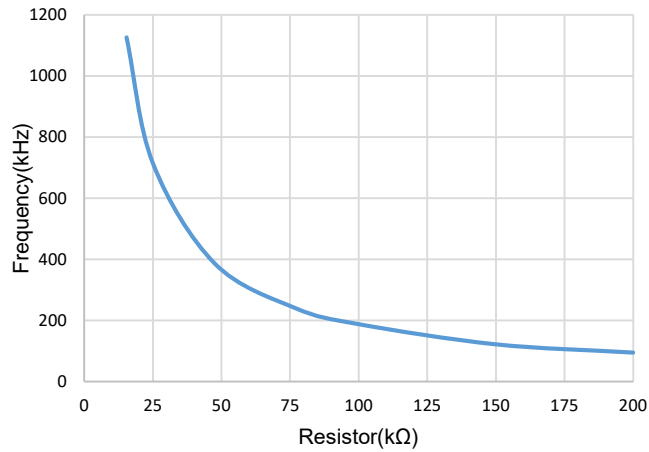


Figure 3. Switching Frequency vs RT

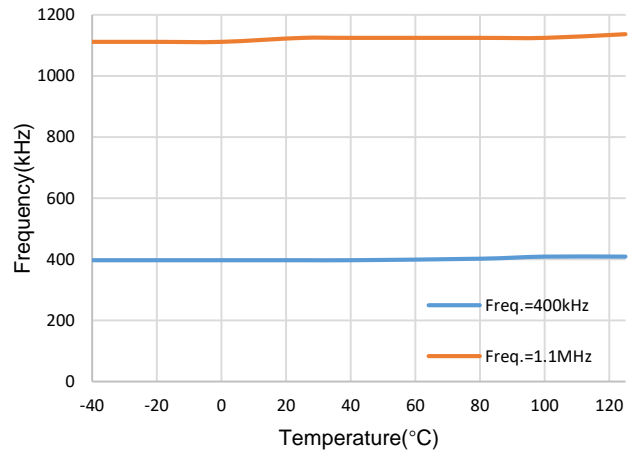


Figure 4. Switching Frequency vs Temperature

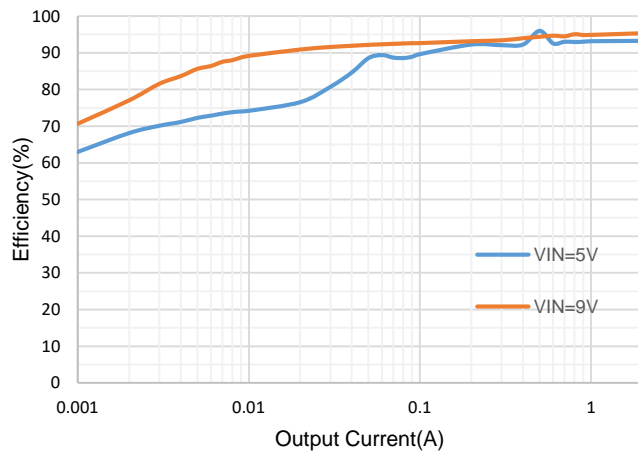


Figure 5. Efficiency vs Load Current, Boost, VOUT=12V

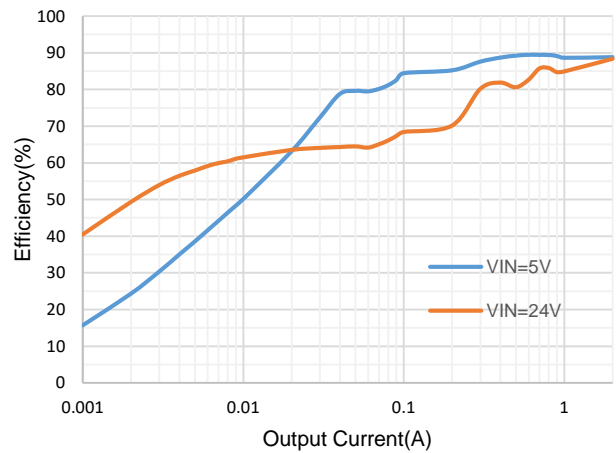


Figure 6. Efficiency vs Load Current, Sepic, VOUT=12V

## TYPICAL CHARACTERISTICS

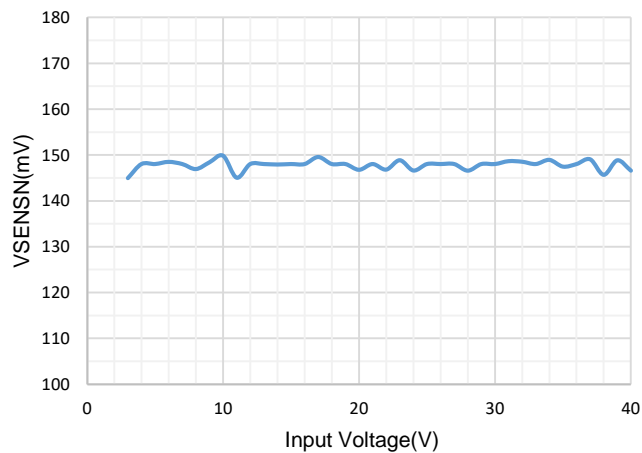


Figure 7. VSENSN vs Input Voltage

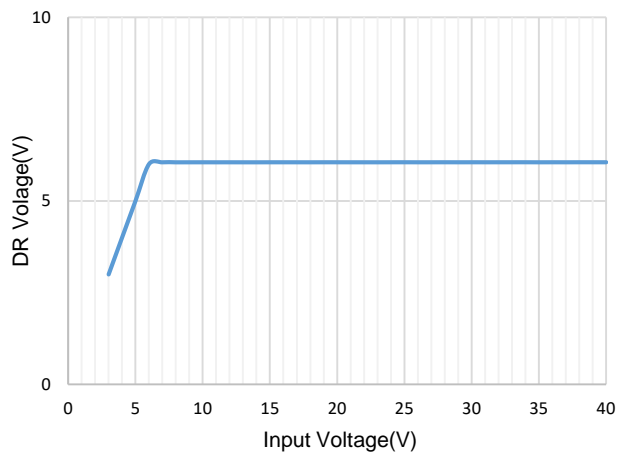


Figure 8. DR Voltage vs Input Voltage

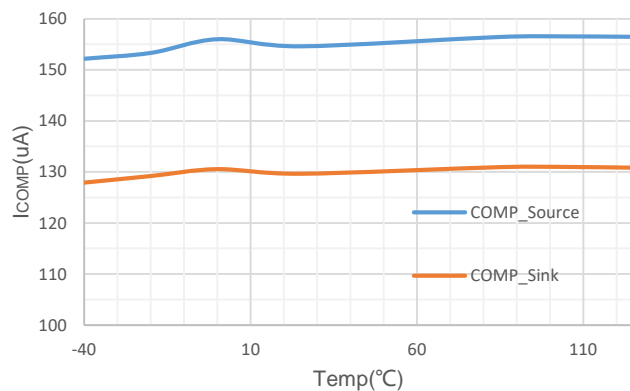


Figure 9. COMP Current vs Temperature

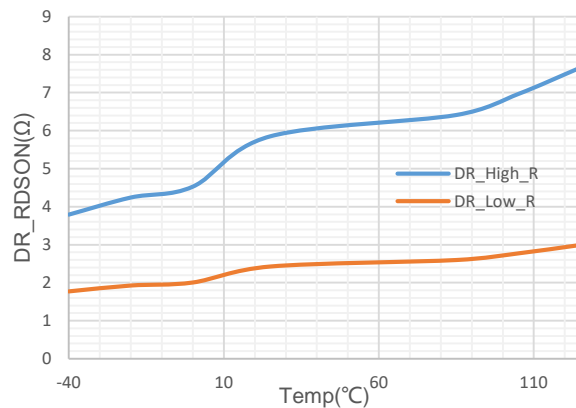


Figure 10. DR Resistance vs Temperature



## OPERATION

### Overview

The SCT81621Q device is a wide input range, non-synchronous boost controller that uses peak-current-mode control. The device can be used in boost, SEPIC, and flyback topologies.

In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the ISNS pin. This voltage is fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input. The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator. At the start of any switching cycle, the oscillator sets the RS latch using the switch logic block. This forces a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off. The voltage sensed across the sense resistor generally contains spurious noise spikes. These spikes can force the PWM comparator to reset the RS latch prematurely. To prevent these spikes from resetting the latch, a blank-out circuit inside the IC prevents the PWM comparator from resetting the latch for a short duration after the latch is set. This duration is called the blanking interval and is specified as minimum on-time in the Electrical Characteristics section. Under extremely light-load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET is on during the blanking interval is more than what is delivered to the load. An over-voltage comparator inside the SCT81621Q prevents the output voltage from rising under these conditions. The over-voltage comparator senses the feedback (FB pin) voltage and resets the RS latch. The latch remains in reset state until the output decays to the nominal value.

The SCT81621Q works at Pulse skip mode to further increase the efficiency in light load condition.

The quiescent current of SCT81621Q is 470uA typical under no-load condition and no switching. Disabling the device, the typical supply shutdown current on VIN pin is 3.9uA.

### Overvoltage Protection

The SCT81621Q has over voltage protection (OVP) for the output voltage. OVP is sensed at the feedback pin (FB). If at any time the voltage at the feedback pin rises to 1.36V (typ.), OVP is triggered. OVP will cause the DR pin to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The SCT81621Q begins switching again when the feedback voltage reaches 1.29V (typ.).

### Slope Compensation Ramp

The SCT81621Q uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch and simpler control loop characteristics. However, current mode control has a Sub-harmonic Oscillation when duty cycle is greater than 50%. To prevent the Sub-harmonic oscillations, a compensation ramp is added to the control signal.

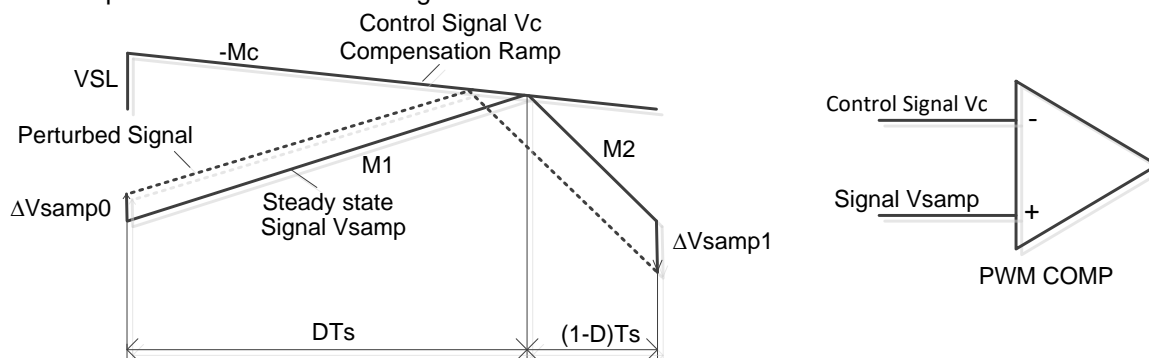


Figure12. Sub-Harmonic Oscillation for  $D > 0.5$  and Compensation Ramp to Avoid Sub-Harmonic Oscillation

The current mode control scheme samples the inductor current,  $I_L$ , and compares the sampled signal,  $V_{smp}$ , to an internally generated control signal,  $V_c$ . The current sense resistor,  $R_{SEN}$ , as shown in Figure11 converts the sampled inductor current,  $I_L$ , to the voltage signal,  $V_{smp}$ , that is proportional to  $I_L$  such that :

$$V_{smp} = I_L * R_{SEN} \quad (1)$$

Figure10 illustrate the theory why Sub-Harmonic Oscillation happen. The rising and falling slopes,  $M_1$  and  $-M_2$  respectively, of  $V_{smp}$  are also proportional to the inductor current rising and falling slopes,  $M_{on}$  and  $-M_{off}$  respectively. Where  $M_{on}$  is the inductor slope during the switch on-time and  $-M_{off}$  is the inductor slope during the switch off-time and are related to  $M_1$  and  $-M_2$  by:

$$M_1 = M_{on} * R_{SEN} \quad (2)$$

$$-M_2 = -M_{off} * R_{SEN} \quad (3)$$

For the boost topology:

$$M_1 = M_{on} * R_{SEN} = V_{in} * R_{SEN} / L \quad (4)$$

$$M_2 = M_{off} * R_{SEN} = (V_{out} - V_{in}) * R_{SEN} / L \quad (5)$$

In Figure10, a small increase in the load current causes the sampled signal to increase by  $\Delta V_{smp0}$ . The effect of this load change,  $\Delta V_{smp1}$ , at the end of the first switching cycle is

$$\Delta V_{smp1} = -\left(\frac{M_2 - M_c}{M_1 + M_c}\right) * \Delta V_{smp0} \quad (6)$$

So, When No compensation ramp signal is added, which  $M_c$  is zero, then:

$$\Delta V_{smp1} = -\left(\frac{M_2}{M_1}\right) * \Delta V_{smp0} = -\left(\frac{D}{1-D}\right) * \Delta V_{smp0} \quad (7)$$

When  $D > 0.5$ ,  $\Delta V_{smp1}$  will be greater than  $\Delta V_{smp0}$ . In other words, the disturbance is divergent. So a very small perturbation in the load will cause the disturbance to increase.

After a compensation ramp is added to the control signal. To ensure that the perturbed signal converges we must maintain:

$$\left| -\left(\frac{M_2 - M_c}{M_1 + M_c}\right) \right| < 1 \quad (8)$$

The compensation ramp has been added internally in the SCT81621Q. The slope of this compensation ramp has been selected to satisfy most applications, and it's value depends on the switching frequency. This slope can be calculated using the formula:

$$M_c = V_{SL} * F_s \quad (9)$$

$V_{SL}$  is the amplitude of the internal compensation ramp and  $F_s$  is the controller's switching frequency.

For more flexibility, slope compensation can be increased by adding one external resistor,  $R_{SL}$ , in the  $I_{SEN}$ 's path. Figure11 shows the setup. The externally generated slope compensation is then added to the internal slope compensation of the SCT81621Q. When using external slope compensation, the formula for  $M_c$  becomes:

$$M_c = (V_{SL} + K * R_{SL}) * F_s \quad (10)$$

A typical value for factor K is 40  $\mu A$ .

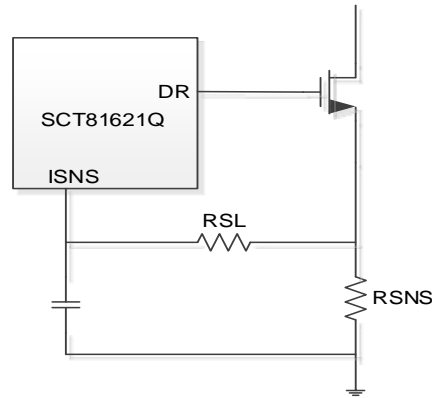


Figure13. External RSL to increase slope compensation

### Adjustable Peak Current Limit

The device provides cycle-by-cycle peak current limit protection that turns off the MOSFET when the sum of the inductor current and the programmable slope compensation ramp reaches the current limit threshold. Peak inductor current limit (IPEAK-CL) in steady state is calculated as shown in:

$$I_{PEAK\_CL} = \frac{V_{SENSE} - 40\mu A \times R_{SL} \times D}{R_{SNS}} \quad (11)$$

Where

- VSENSE is ISEN pin limiting voltage (TYP=145.5mV)
- IPEAK-CL is the inductor peak current limit
- RSL is Slope compensation resistor
- D is Duty cycle
- RSNS is the Inductance peak current detection resistance

When overload happens, the converter cannot provide output current to satisfy loading requirement. The inductor current is clamped at over current limitation. Thus, the output voltage drops below regulated voltage with FB voltage less than internal reference voltage continuously. The internal COMP voltage ramps up to high. When COMP voltage is clamped for 64 cycles, the controller stops working. After remaining OFF for 32768 cycles, the device restarts from soft starting phase. If overload or hard short condition still exists during soft-start and make COMP voltage clamped at high, after soft start time and COMP still keep high for 64 cycles, the device enters into turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation

Because D can be variable under different Vin, IPEAK-CL is not stable under different Vin when using external slope compensation resistor. So for an accurate peak current limit operation over the input supply voltage, SCT recommends using only the fixed slope compensation.

### Output Voltage

The output voltage is set by an external resistor divider RFBT and RFBB in typical application schematic. A minimum current of typical 20uA flowing through feedback resistor divider gives good accuracy and noise covering. The value of RFBT can be calculated by Equation 12.

$$R_{FBT} = \frac{V_{OUT} - V_{REF}}{V_{REF}} \times R_{FBB} \quad (12)$$

where:

- VREF is the feedback reference voltage, typical 1.275V

# SCT81621Q

## Frequency Adjust/Shutdown/ Synchronization

The switching frequency of the SCT81621Q can be adjusted between 100 kHz and 2.2 MHz using a single external resistor. This resistor must be connected between the FA/SYNC/SD pin and ground. Equation 13 can be used to estimate the frequency adjust resistor.

$$R_{FA} (K\Omega) = \frac{19000}{f_{sw}(kHz)} \quad (13)$$

The SCT81621Q can also be synchronized to an external clock. The external clock must be connected between the FA/SYNC/SD pin and ground, as shown in Figure 15. The frequency adjust resistor may remain connected while synchronizing a signal, therefore if there is a loss of signal, the switching frequency will be set by the frequency adjust resistor.

The FA/SYNC/SD pin also functions as a shutdown pin. If a high signal (>1.27V) appears on the FA/SYNC/SD pin over 30μS, the SCT81621Q stops switching and goes into a low current mode. The total supply current of the IC reduces to 3.9 μA, typically, under these conditions.

Figure 16 and Figure 17 show an implementation of a shutdown function when operating in frequency adjust mode and synchronization mode, respectively. In frequency adjust mode, connecting the FA/SYNC/SD pin to ground forces the clock to run at a certain frequency. Pulling this pin high shuts down the IC. In frequency adjust or synchronization mode, a high signal for more than 30 μs shuts down the IC

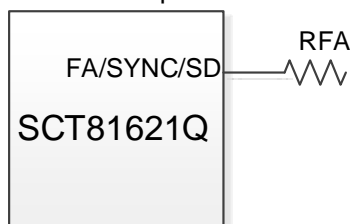


Figure14. Frequency Adjust

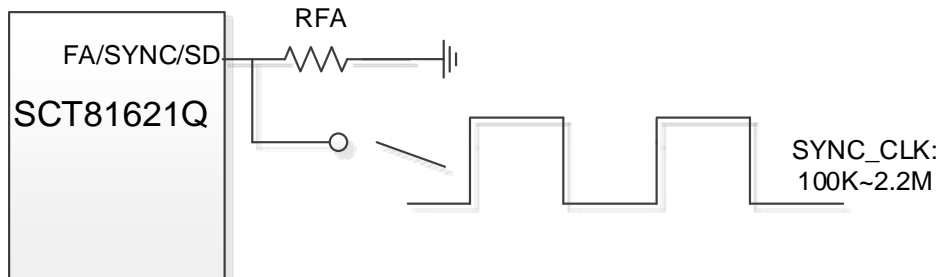


Figure15. Frequency Sync

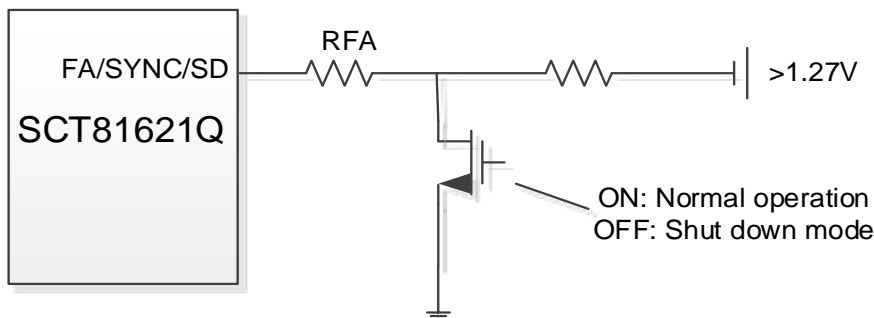


Figure16. Shutdown operation in Frequency Adjust Mode

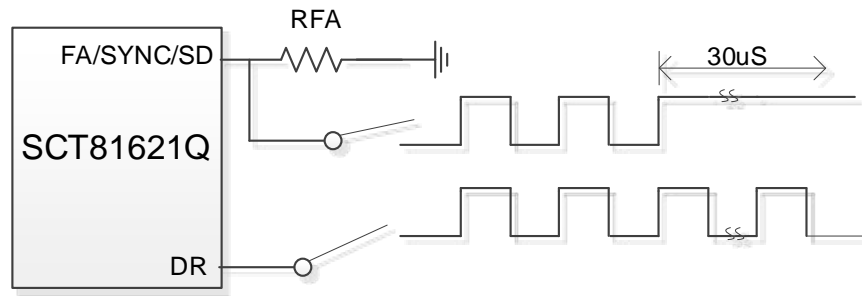


Figure17. Shutdown operation in Frequency Synchronization Mode

## APPLICATION INFORMATION

### Typical Application (Boost)

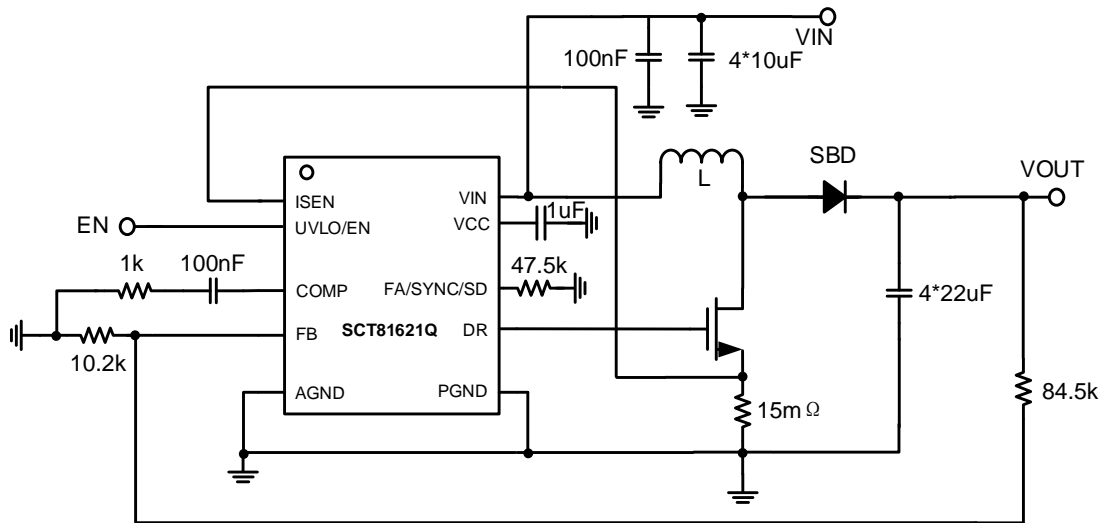


Figure 18. Application Schematic, 3V to 11V, 2A Boost Regulator at 400kHz

#### Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal 3V to 11V
Output Voltage	12V
Maximum Output Current	3A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

## Inductor Selection (Boost)

The performance of inductor affects the power supply's steady state operation, transient behavior, loop stability, and boost converter efficiency. The inductor value, DC resistance, and saturation current influences both efficiency and the magnitude of the output voltage ripple. Larger inductance value reduces inductor current ripple and therefore leads to lower output voltage ripple. For a fixed DC resistance, a larger value inductor yields higher efficiency via reduced RMS and core losses. However, a larger inductor within a given inductor family will generally have a greater series resistance, thereby counteracting this efficiency advantage.

Inductor values can have  $\pm 20\%$  or even  $\pm 50\%$  tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the value at 0-A current depending on how the inductor vendor defines saturation. When selecting an inductor, choose its rated current especially the saturation current larger than its peak current during the operation.

To calculate the current in the worst case, use the minimum input voltage, maximum output voltage, maximum load current and minimum switching frequency of the application, while considering the inductance with -30% tolerance and low-power conversion efficiency.

For a boost converter, calculate the inductor DC current as in Equation 14

$$I_{LDC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (14)$$

Where

- $V_{OUT}$  is the output voltage of the boost converter
- $I_{OUT}$  is the output current of the boost converter
- $V_{IN}$  is the input voltage of the boost converter
- $\eta$  is the power conversion efficiency

Calculate the inductor current peak-to-peak ripple,  $I_{LPP}$ , as in Equation 15.

$$I_{LPP} = \frac{1}{L \times \left( \frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times f_{SW}} \quad (15)$$

Where

- $I_{LPP}$  is the inductor peak-to-peak current
- $L$  is the inductance of inductor
- $f_{SW}$  is the switching frequency
- $V_{OUT}$  is the output voltage
- $V_{IN}$  is the input voltage

Therefore, the peak switching current of inductor,  $I_{LPEAK}$ , is calculated as in Equation 16

$$I_{LPEAK} = I_{LDC} + \frac{I_{LPP}}{2} \quad (16)$$

Set the current limit of the SCT81621Q higher than the peak current  $I_{LPEAK}$  and select the inductor with the saturation current higher than the current limit.

## Input Capacitor Selection

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The RMS current in the input capacitor is given using Equation 17.

$$I_{CIN(RMS)} = \frac{(V_{OUT} - V_{IN}) \times V_{IN}}{\sqrt{12} \times V_{OUT} \times L \times f_{SW}} \quad (17)$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore, a good quality capacitor should be chosen in the range of 10  $\mu\text{F}$  to 40  $\mu\text{F}$ . If a value lower than 10  $\mu\text{F}$  is used, then problems with impedance interactions or switching noise can affect the SCT81621Q. To improve performance, especially with  $V_{\text{IN}}$  below 8 volts, it is recommended to use a 2.2 Ohm resistor at the input to provide an RC filter. The resistor is placed in series with the VIN pin with only a bypass capacitor attached to the VIN pin directly. A 0.1- $\mu\text{F}$  or 1- $\mu\text{F}$  ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor at the input power supply.

## Output Capacitor Selection

For small output voltage ripple, choose a low-ESR output capacitor like a ceramic capacitor. Typically, 3~4x 22 $\mu\text{F}$  ceramic output capacitors work for most applications. A 0.1 $\mu\text{F}$  ceramic bypass capacitor is recommended to be placed as close as possible to the switch node. Higher capacitor values can be used to improve the load transient response. Due to a capacitor's derating under DC bias, the bias can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. From the required output voltage ripple, use the equation x and x to calculate the minimum required effective capacitance,  $C_{\text{OUT}}$ .

$$V_{\text{ripple}_C} = \frac{(V_{\text{OUT}} - V_{\text{IN\_MIN}}) \times I_{\text{OUT}}}{V_{\text{OUT}} \times f_{\text{SW}} \times C_{\text{OUT}}} \quad (18)$$

$$V_{\text{ripple\_ESR}} = I_{\text{Lpeak}} \times \text{ESR} \quad (19)$$

where

- $V_{\text{ripple}_C}$  is output voltage ripple caused by charging and discharging of the output capacitor.
- $V_{\text{ripple\_ESR}}$  is output voltage ripple caused by ESR of the output capacitor.
- $V_{\text{IN\_MIN}}$  is the minimum input voltage of boost converter.
- $V_{\text{OUT}}$  is the output voltage.
- $I_{\text{OUT}}$  is the output current.
- $I_{\text{Lpeak}}$  is the peak current of the inductor.
- $f_{\text{SW}}$  is the converter switching frequency.
- ESR is the ESR resistance of the output capacitors.

## Power MOSFET Selection

The following parameters should be taken into consideration for MOSFET: the on-resistance  $R_{\text{DS\_ON}}$ , the minimum gate threshold voltage  $V_{\text{TH\_MIN}}$ , the total gate charge  $Q_g$ , the reverse transfer capacitance  $C_{\text{RSS}}$ , and the maximum drain to source voltage  $V_{\text{Q\_MAX}}$ . The peak switching voltage between drain to source in a Boost is given by

$$V_{\text{SW\_PEAK}} = V_{\text{IN}} + V_D \quad (20)$$

Then the  $V_{\text{Q\_MAX}}$  of power MOSFET should be greater than the peak switching voltage.

The peak switching current flowing through the MOSFET is given by:

$$I_{\text{Q\_PEAK}} = I_{\text{LPEAK}} \quad (21)$$

The RMS current through the MOSFET is calculated by:

$$I_{\text{Q\_RMS}} = \sqrt{(I_{\text{LDC}}^2 + \frac{I_{\text{LPP}}}{12}) * D} \quad (22)$$

Then power dissipation in MOSFET can be estimated by:

$$P_{\text{DIS}} = I_{\text{Q\_RMS}}^2 \times R_{\text{DS\_ON}} \times D_{\text{MAX}} + (V_O + V_{\text{IN\_MIN}}) \times I_{\text{Q\_PEAK}} \times \frac{Q_g \times f_{\text{SW}}}{I_G} \quad (23)$$

Where

$I_G$  is the gate drive current.

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

## Output Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than its peak current. The peak diode current can be calculated using Equation 24.

$$I_{D(PEAK)} = \frac{I_{OUT}}{(1-D)} + \Delta I_L \quad (24)$$

Thermally the diode must be able to handle the maximum average current delivered to the output. The peak reverse voltage for boost converters is equal to the regulated output voltage. The diode must be capable of handling this voltage. To improve efficiency, a low forward drop schottky diode is recommended.

# SCT81621Q

## Application Waveforms

Vin=5V, Vout=12V, unless otherwise noted

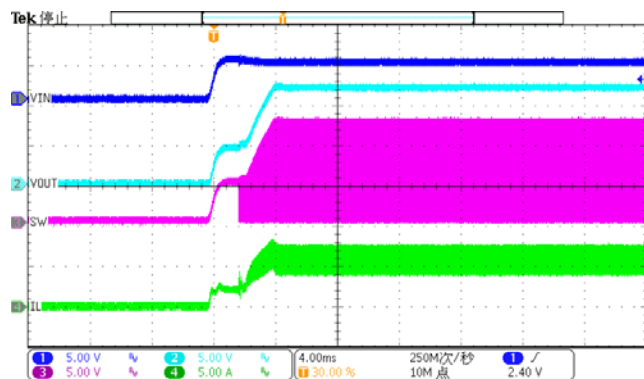


Figure 19. Power up(Iload=2A)

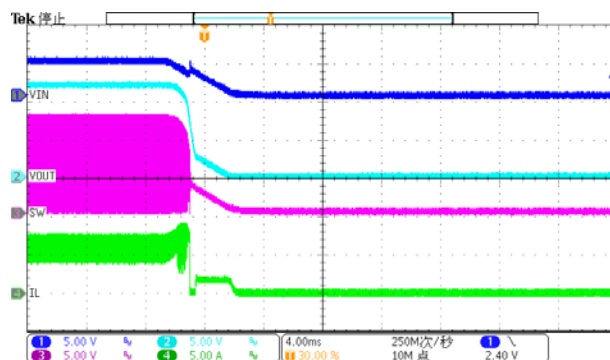


Figure 20. Power down(Iload=2A)

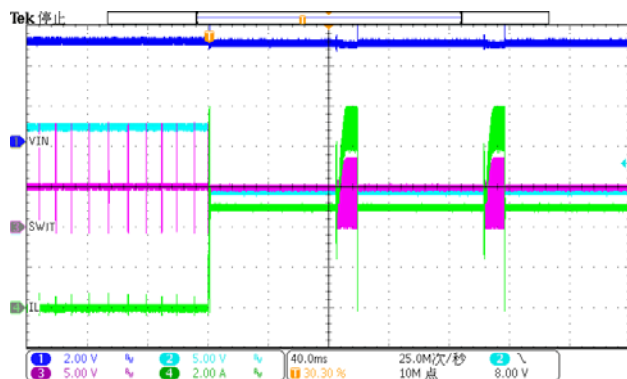


Figure 21. Over current protection (Iload=5A)

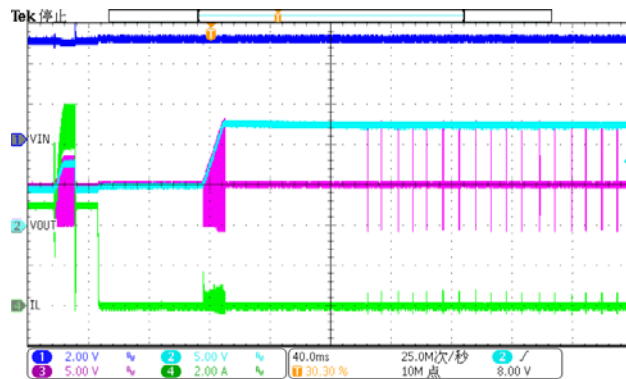


Figure 22. Over current recovery (Iload=5A)

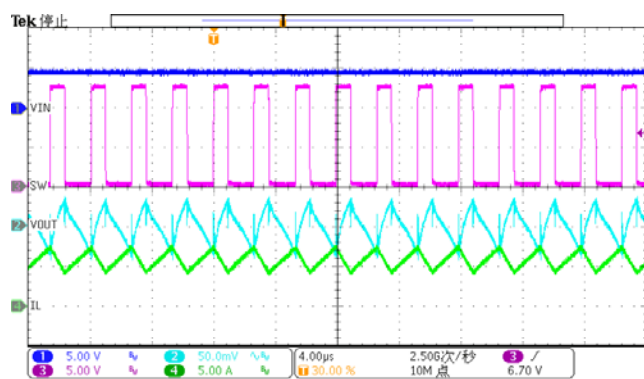


Figure 23. Steady-state (Iload=2A)

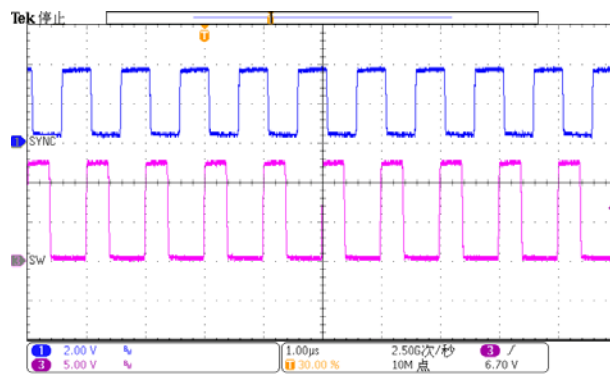


Figure 24. Sync Frequency

## APPLICATION INFORMATION

## Typical Application(Sepic)

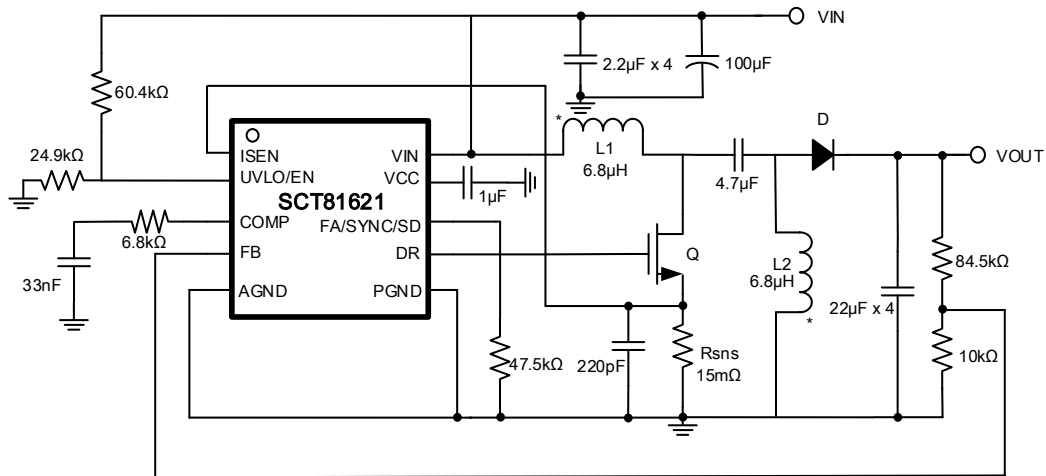


Figure 25. Application Schematic, 5V to 60V, 2A Sepic Regulator at 400kHz

## Design Parameters

Design Parameters	Example Value
Input Voltage	24V Normal 5V to 60V
Output Voltage	12V
Maximum Output Current	2A
Switching Frequency	400 KHz
Output voltage ripple (peak to peak)	75mV (Load=2A)

## Inductor Selection (Sepic)

A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 20% to 40% of the maximum input current at the minimum input voltage. The current ripple flowing in inductors L1 and L2 is given by:

$$\Delta I_{L1} = I_{IN} \times 40\% = I_O \times \frac{V_O}{V_{IN\_MIN}} \times 40\% \quad (25)$$

$$\Delta I_{L2} = I_O \times 40\% = I_O \times 40\% \quad (26)$$

Normally we can select equal value for the inductors L1 and L2, derived as:

$$L_1 = L_2 = L = \frac{V_{IN\_MIN}}{\Delta I_L \times f_{SW}} \times D_{MAX} \quad (27)$$

Where

- $f_{SW}$  is the switching frequency.

Note that the saturation current of inductors should be greater than peak current flowing in inductors, given by:

$$I_{L1\_PEAK} = I_{IN} + \frac{\Delta I_L}{2} = I_O \times \frac{V_O}{V_{IN\_MIN}} \times \left(1 + \frac{40\%}{2}\right) \quad (28)$$

$$I_{L2\_PEAK} = I_O + \frac{\Delta I_L}{2} = I_O \times \left(1 + \frac{40\%}{2}\right) \quad (29)$$

If L1 and L2 are wound in same core as a coupled inductor, the inductance required will be half due to the mutual induction, calculated by:

$$L_1 = L_2 = \frac{L}{2} = \frac{V_{IN\_MIN}}{2 \times \Delta I_L \times f_{SW}} \times D_{MAX} \quad (30)$$

## Power MOSFET Selection

The following parameters should be taken into consideration for MOSFET: the on-resistance  $R_{DS\_ON}$ , the minimum gate threshold voltage  $V_{TH\_MIN}$ , the total gate charge  $Q_g$ , the reverse transfer capacitance  $C_{RSS}$ , and the maximum drain to source voltage  $V_{Q\_MAX}$ . The peak switching voltage between drain to source in a SEPIC is given by:

$$V_{SW\_PEAK} = V_{IN} + V_O + V_D \quad (31)$$

Then the  $V_{Q\_MAX}$  of power MOSFET should be greater than the peak switching voltage.

The peak switching current flowing through the MOSFET is given by:

$$I_{Q\_PEAK} = I_{L1\_PEAK} + I_{L2\_PEAK} \quad (32)$$

The RMS current through the MOSFET is calculated by:

$$I_{Q\_RMS} = I_O \times \sqrt{\frac{(V_O + V_{IN\_MIN} + V_D) \times (V_O + V_D)}{V_{IN\_MIN}^2}} \quad (33)$$

Then power dissipation in MOSFET can be estimated by:

$$P_{DIS} = I_{Q\_RMS}^2 \times R_{DS\_ON} \times D_{MAX} + (V_O + V_{IN\_MIN}) \times I_{Q\_PEAK} \times \frac{Q_g \times f_{SW}}{I_G} \quad (34)$$

Where

$I_G$  is the gate drive current.

The total power dissipation of MOSFET includes conduction loss as shown in the first term and switching loss as shown in the second term. The total power dissipation should be within package thermal ratings.

### Output Diode Selection

The diode at the output side must withstand the reverse voltage when the MOSFET is turned-on. The peak reverse voltage is given by:

$$V_{D\_PEAK} = V_{IN\_MAX} + V_{O\_MAX} \quad (35)$$

The diode should also be capable to flow switch peak current  $I_{Q\_PEAK}$ .

The power dissipation of the diode is equal to the forward voltage drop multiplies output current. Schottky diodes are recommended here to minimize the power loss.

### Coupling Capacitor Selection

For ceramic capacitors with low-ESR, the peak to peak voltage ripple on coupling capacitor is estimated by:

$$\Delta V_{CS} = \frac{I_O \times D_{MAX}}{C_S \times f_{SW}} \quad (36)$$

The maximum voltage across the coupling capacitor is maximum input voltage. The voltage rating of the coupling capacitor must be greater than it.

The RMS current of coupling capacitor is given by:

$$I_{CS\_RMS} = I_O \times \sqrt{\frac{V_O + V_D}{V_{IN\_MIN}}} \quad (37)$$

There is a large RMS current through coupling capacitor relative to output power. Ensure the coupling capacitor can withstand it with good heat generation to have proper thermal performance.

### Input Capacitor Selection

The SEPIC has an inductor at input side thus the input current is continuous and triangular. The RMS current flowing through the input capacitor is given by:

$$I_{IN\_RMS} = \frac{\Delta I_{L1}}{\sqrt{12}} \quad (38)$$

Since input current ripple is relative low, the capacitance would be not too critical. While 100μF in total or higher value is strongly recommended in order to provide stable input supply.

### Output Capacitor Selection

Similar to boost converter, the SEPIC output capacitor suffers large current ripple. The capacitance must be enough to provide the load current. The maximum voltage ripple in the output capacitor is:

$$\Delta V_{OUT} = \frac{I_O \times D_{MAX}}{C_{OUT} \times f_{SW}} + ESR \times (I_{L1\_PEAK} + I_{L2\_PEAK}) \quad (39)$$

Assuming ceramic capacitors are used here and ESR can be ignored, the output capacitor is given by:

$$C_{OUT} \geq \frac{I_O \times D_{MAX}}{\Delta V_{OUT} \times f_{SW}} \quad (40)$$

The output capacitor must have an enough RMS current rating to handle the maximum RMS current in the output capacitor, calculated by:

$$I_{COUT\_RMS} = I_O \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}} \quad (41)$$

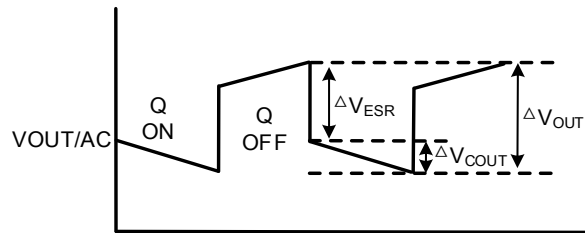


Figure 26. Output Voltage Ripple

## Application Waveforms

$V_{in}=5V$ ,  $V_{out}=12V$ , unless otherwise noted

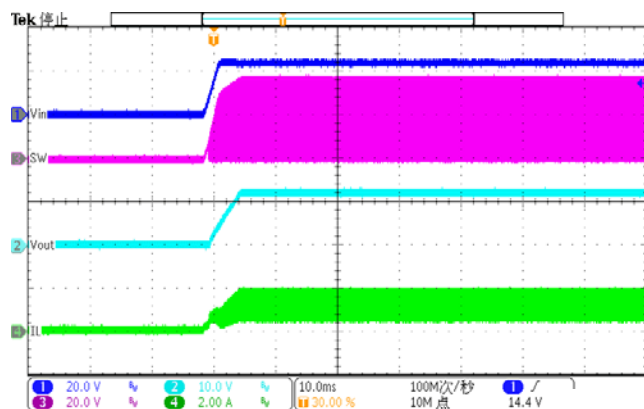


Figure 27. Power up( $I_{load}=2A$ )

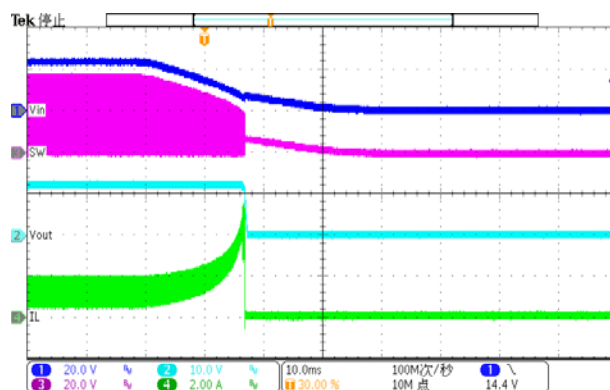


Figure 28. Power down( $I_{load}=2A$ )

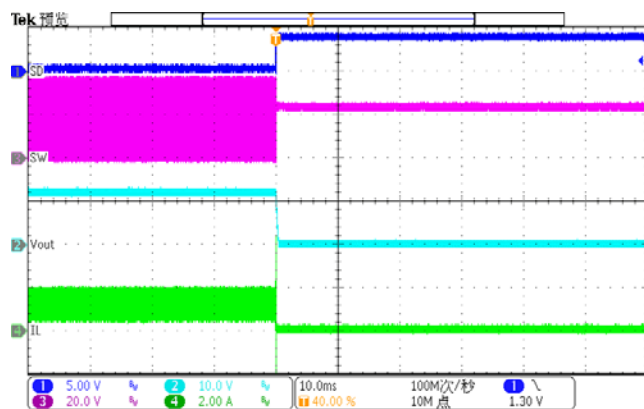


Figure 29. Shutdown entry

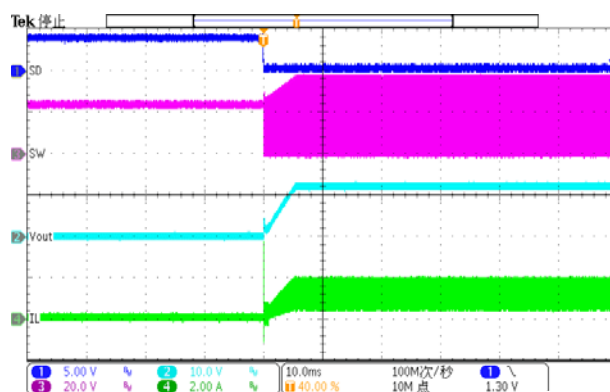


Figure 30. Shutdown remove

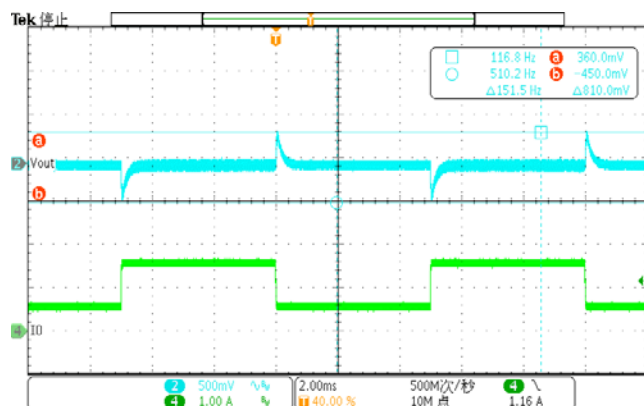


Figure 31. LoadTrans ( $I_{load}=0.5A-1.5A$ )

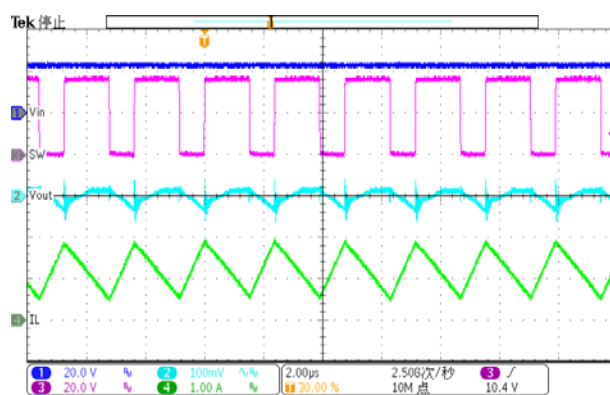


Figure 32. steady-state ( $I_{load}=2A$ )

## Layout Guideline

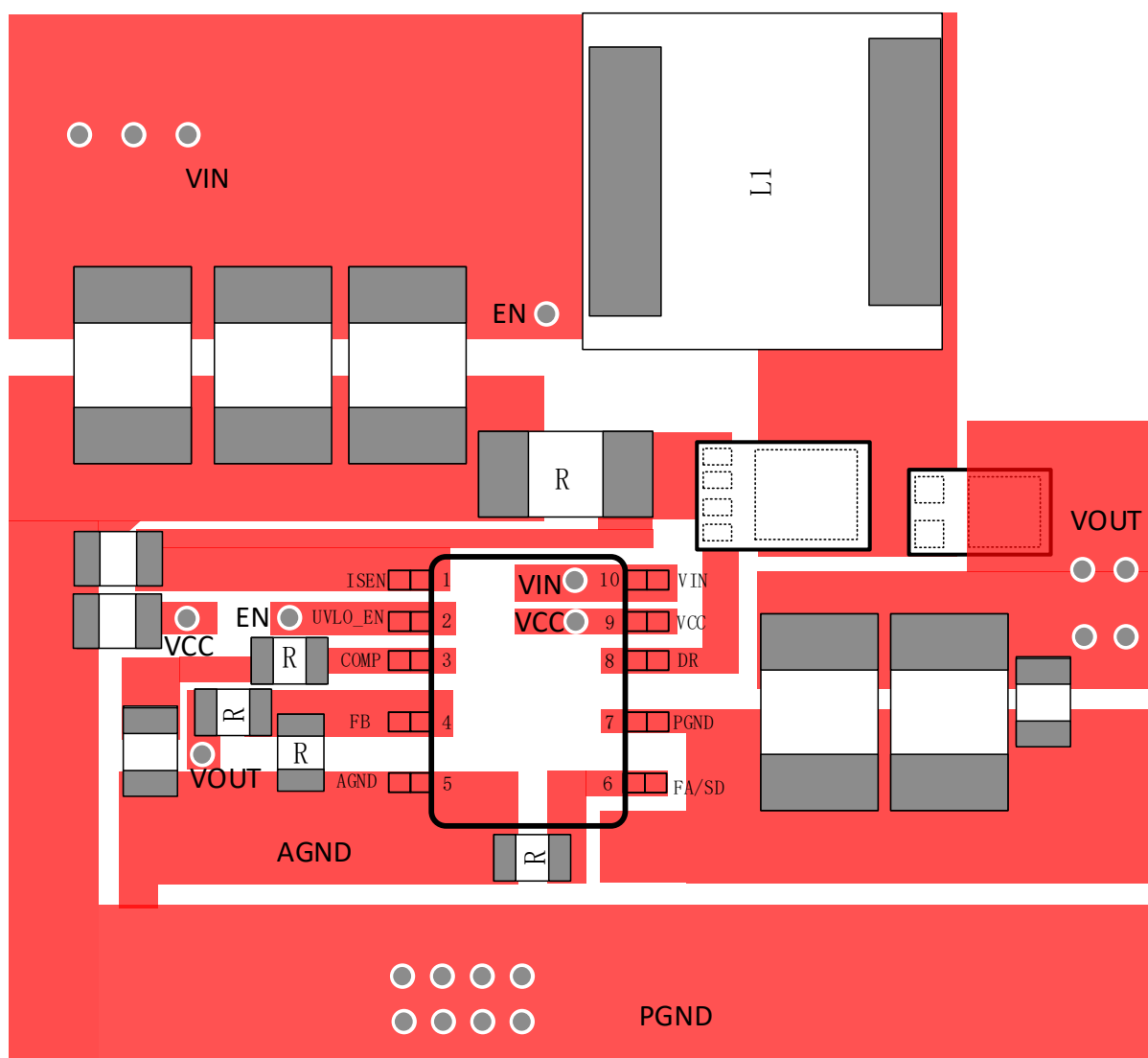
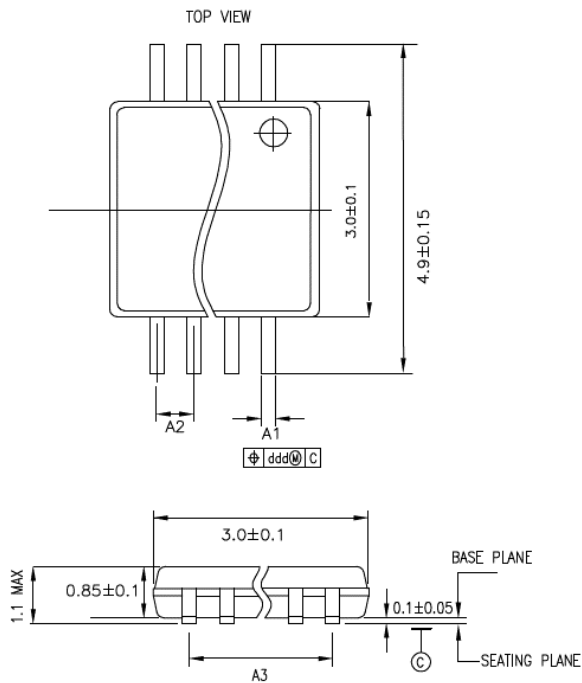


Figure 33. BOOST PCB Layout

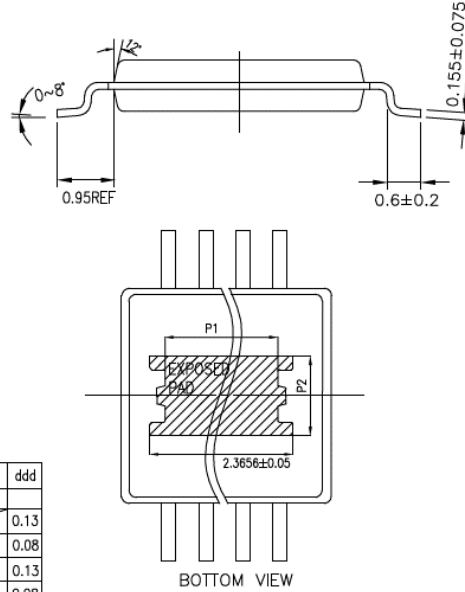
## PACKAGE INFORMATION



LEAD	A1		A2	A3	PAD SIZE	P1		P2		ddd
	MIN	MAX				MIN	MAX	MIN	MAX	
MSOP/BLD	0.22	0.38	0.65 BSC	1.95 BSC	1.83*1.83					0.13
MSOP/10LD	0.17	0.27	0.50 BSC	2.00 BSC	1.83*1.83					0.08
MSOP-EP/BLD	0.22	0.38	0.65 BSC	1.95 BSC	1.83*1.83	1.63	1.88	1.47	1.73	0.13
MSOP-EP/10LD	0.17	0.27	0.50 BSC	2.00 BSC	1.83*1.83	1.63	1.88	1.47	1.73	0.08

## NOTES:

- 1) LEAD FRAME : C7025(THICKNESS :0.127MM)
- 2) LEAD FINISH : SOLDER PLATED
- 3) BOTH PACKAGE LENGTH AND WIDTH  
DO NOT INCLUDE FLASH.
- 4) FORMED LEAD SHALL BE PLANAR WITH RESPECT  
TO ONE ANOTHER WITHIN 0.10(0.004)
- 5) CONTROLLING DIMENSION : MM .
- 6) UNREMOVED FLASH BETWEEN LEADS&PACKAGE END FLASH SHALL  
NOT EXCEED 0.15MM FROM BOTTOM BODY PER SIDE.

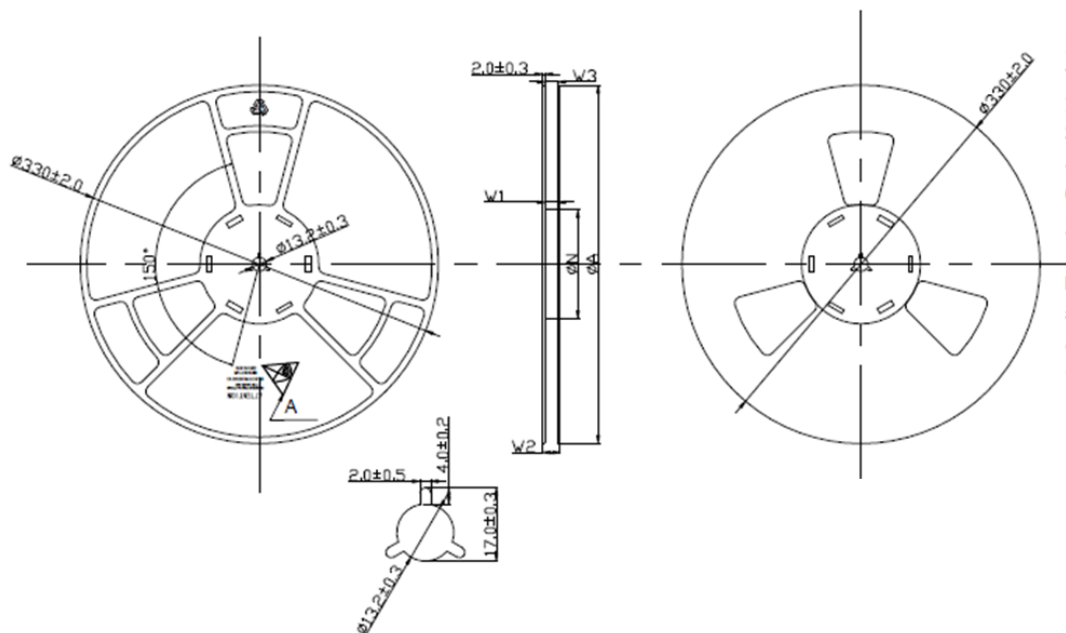


## NOTE:

1. Drawing proposed to be made a JEDEC package outline MO-220 variation.
2. Drawing not to scale.
3. All linear dimensions are in millimeters.
4. Thermal pad shall be soldered on the board.
5. Dimensions of exposed pad on bottom of package do not include mold flash.
6. Contact PCB board fabrication for minimum solder mask web tolerances between the pins.

## TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT81621QMRDR	MSOP	10	4000



PRODUCT SPECIFICATIONS					
TYPE WIDTH	ØA	ØN	W1(+20)	W2(Max)	W3(Max)
12MM	330±2.0	100±1.0	12.4	18.4	11.9/15.4

