SGM41280
Low-, Wide- Voltage Battery Front-End DC/DC Converter

GENERAL DESCRIPTION

The SGM41280 device provides a power supply solution for products powered by either by a Li-Ion, Nickel-Rich, Silicon Anode, Li-Ion or LiFePO4 battery. The voltage range is optimized for single-cell portable applications like in smart-phones or tablet PCs. Acted as the high-power pre-regulator, the SGM41280 can implement the high density supply to overcome battery system current and voltage limitations.

Used as high density power supply, the SGM41280 can facilitate high current WLED flash, WLED flash module, RF engine PMIC, audio PA etc. with maximum allowed output.

During operation, when the battery is at a good state-of-charge, a low-ohmic, high-efficient integrated pass- through path (Bypass mode) connects the battery to the powered system.

If the battery gets to a lower state of charge and its voltage becomes lower than the desired minimum system voltage, the device seamlessly transits into boost mode to utilize the full battery capacity.

The SGM41280 operates in synchronous, 2.5MHz boost mode and enters power-save mode operation (PFM) at light load currents to maintain high efficiency over the entire load current range.

The SGM41280 is available in Green WLCSP-1.27×1.67-12B and TQFN-3×3-16L packages. It operates over an ambient temperature range of -40℃ to +85℃.

FEATURES

- **Wide V_{IN} Range from 2.2V to 4.9V**
- **3.85V/3.0A Continues Output at 3.4V Input**
- **95% Efficiency at 2.5MHz PWM Frequency**
- **Simple I/O Control Interface**
- **Programmable Output Voltage: 3.35V/3.45V/3.65V/3.85V(Default)/4.25V**
- **I_Q = 14μA & $R_{DS(ON)}$ = 25mΩ in Bypass Mode**
- **Seamless Transition between Boost Mode and Bypass Mode**
- **Short-Circuit Protection**
- **Internal Soft-Start**
- **-40℃ to +85℃ Operating Temperature Range**
- **Available in Green WLCSP-1.27×1.67-12B and TQFN-3×3-16L Packages**

APPLICATIONS

Smart-Phones
Tablet PCs
Portable Electronic Equipment
Brownout Prevention when High Power Loads

TYPICAL APPLICATION

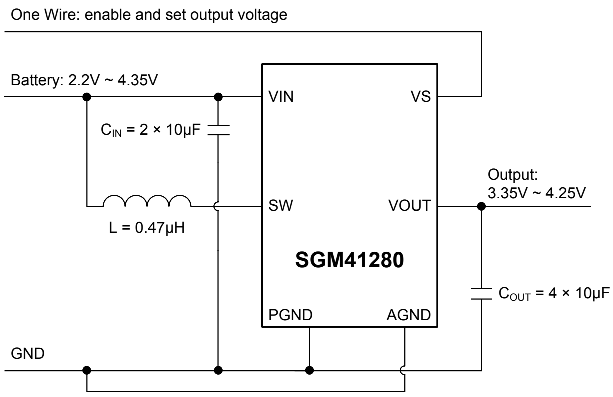


Figure 1. Typical Application Circuit

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41280	WLCSP-1.27×1.67-12B	-40℃ to +85℃	SGM41280YG/TR	XXXX GD3	Tape and Reel, 3000
	TQFN-3×3-16L	-40℃ to +85℃	SGM41280YTQ16G/TR	41280TQ XXXXX	Tape and Reel, 4000

NOTE: XXXX = Date Code. XXXXX = Date Code and Vendor Code.

Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VIN, SW, VOUT to GND .... -0.3V to 6V
VS to GND .... -0.3V to V_{CC} + 0.3V
Package Thermal Resistance
WLCSP-1.27×1.67-12B, θ_{JA} .... 90℃/W
TQFN-3×3-16L, θ_{JA} .... 50℃/W
Junction Temperature .... +150℃
Storage Temperature Range........................ -65℃ to +150℃
Lead Temperature (Soldering, 10s) .... +260℃
ESD Susceptibility
HBM 2000V
MM 200V

RECOMMENDED OPERATING CONDITIONS

Input Voltage Range .... 2.2V to 4.9V
Operating Temperature Range .... -40℃ to +85℃
Operating Junction Temperature Range ...... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed may cause permanent damage to the device. Functional operation of the device at these or any other conditions beyond those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ESD SENSITIVITY CAUTION

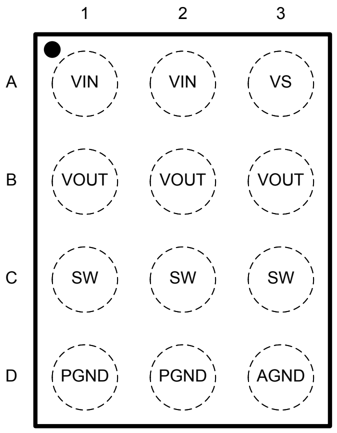
This integrated circuit can be damaged by ESD if you don’t pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time.

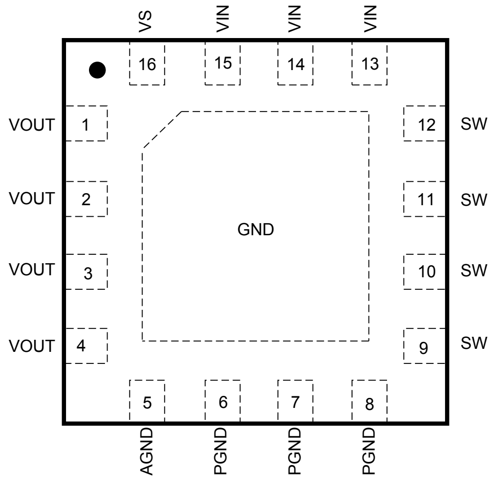
PIN CONFIGURATIONS

(TOP VIEW)



WLCSP-1.27×1.67-12B

(TOP VIEW)



TQFN-3×3-16L

PIN DESCRIPTION

PIN		NAME	FUNCTION
WLCSP-1.27×1.67-12B	TQFN-3×3-16L		
A1, A2	13, 14, 15	VIN	Power Supply Input.
A3	16	VS	Simple Control Interface. Set the output voltage through pulse counting. Pull this pin up for longer period (t_{BLK} + t_{SS}) to start from shutdown state to output a default voltage or a programmable voltage, pull this pin down for longer period (t_{STOP}) to select the default voltage or shutdown its operation.
B1, B2, B3	1, 2, 3, 4	VOUT	Output Voltage.
C1, C2, C3	9, 10, 11, 12	SW	Switching Node. Connect to external inductor.
D1, D2	6, 7, 8	PGND	Power Ground Pin.
D3	5	AGND	Signal Ground Pin.
–	Exposed Pad	GND	The exposed pad should be connected to GND.

ELECTRICAL CHARACTERISTICS

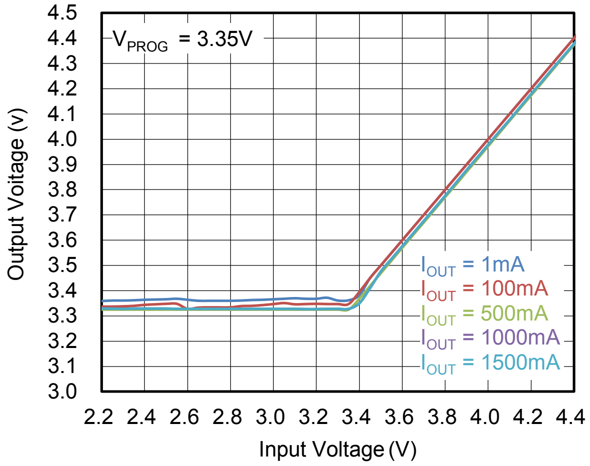
(V_{IN} = 3.6V, V_{OUT} = 3.85V, T_A = +25℃, unless otherwise noted.)

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLIES							
Input Voltage Range		V_{IN}		2.2		4.9	V
Quiescent Current into VIN		I_Q	DC/DC Boost Mode, I_{OUT} = 0mA		18		μA
			Bypass Mode, I_{OUT} = 0mA		14		μA
Shutdown Supply Current		I_{SHDN}	Disable		0.5		μA
Under-Voltage Lockout Threshold		V_{UVLO}	Rising V_{IN}		1.9		V
Under-Voltage Lockout Hysteresis		V_{UVHYST}			0.1		V
Power-On Blanking Time		t_{BLK}			40		ms
SWITCHING AND SYNCHRONIZATION							
Switching Frequency		f_{SW}			2.5		MHz
OUTPUT							
Output Voltage Accuracy		V_{OUT}	DC/DC Boost Mode, No Load, Open Loop		3		%
Programmable Output Voltage		V_{PROG}	V1		3.35		V
			V2		3.45		V
			V3		3.65		V
			V4, Default Voltage		3.85		V
			V5		4.25		V
Soft Start Time		t_{SS}			10		ms
POWER SWITCH							
Low Side Switch MOSFET On Resistance in Boost Mode	WLCSP				27		mΩ
	TQFN				42		
High Side Switch MOSFET On Resistance in Boost Mode	WLCSP				45		mΩ
	TQFN				56		
High Side Switch MOSFET On Resistance in Bypass Mode	WLCSP		SW Pin Connects to VIN Pin		25		mΩ
	TQFN		SW Pin Connects to VIN Pin		30		
PROTECTION							
Valley Current Limit in Boost Mode			V_{IN} = 3.3V, V_{OUT} = 3.85V, Inductor Current		6000		mA
Current Limit in Bypass Mode			V_{IN} = 4.2V, V_{PROG} = 3.85V, Output Current		6000		mA
Thermal Shutdown			T_J Increasing		165		℃
Thermal Shutdown Hysteresis					15		℃
INTERFACE CHARACTERICS							
Input High Threshold		V_{IH}	VS Pin		1.0		V
Input Low Threshold		V_{IL}	VS Pin		0.4		V
Input Leakage Current			VS Pin		1		μA
VS Change Stop Time		t_{STOP}			2		ms
Shutdown Delay Time		t_{OFF}			100		ms
t_{OFF} Hold On Time		$t_{OFF-HOLD}$			40		ms
Effective Pulse Time		t_{PULSE}			1		ms

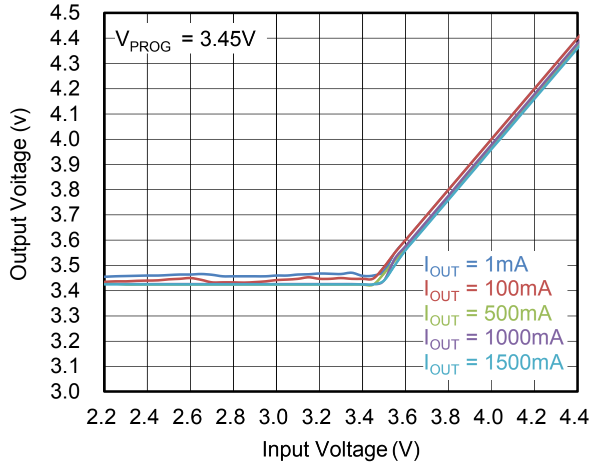
TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 2×10μF, C_{OUT} = 4×10μF, L = 0.47μH, T_A = +25℃, unless otherwise noted.

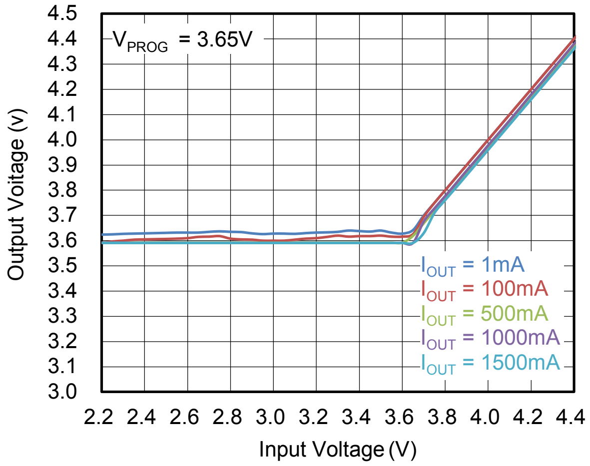
DC Output Voltage vs. Input Voltage



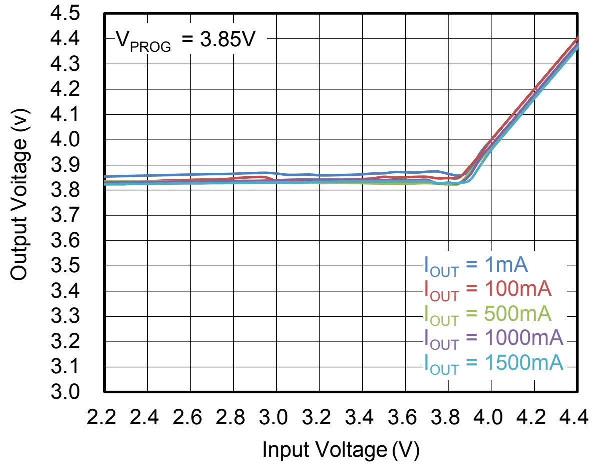
DC Output Voltage vs. Input Voltage



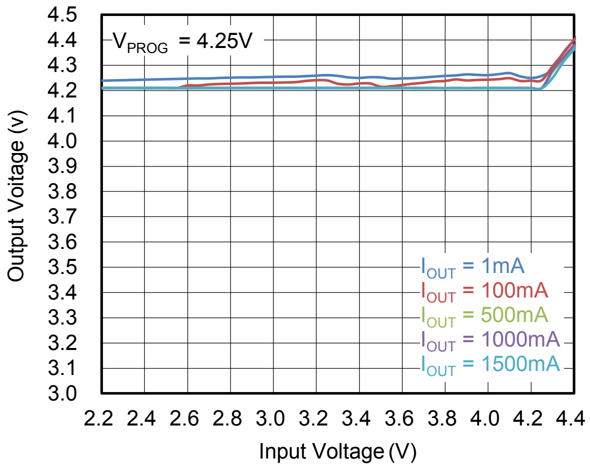
DC Output Voltage vs. Input Voltage



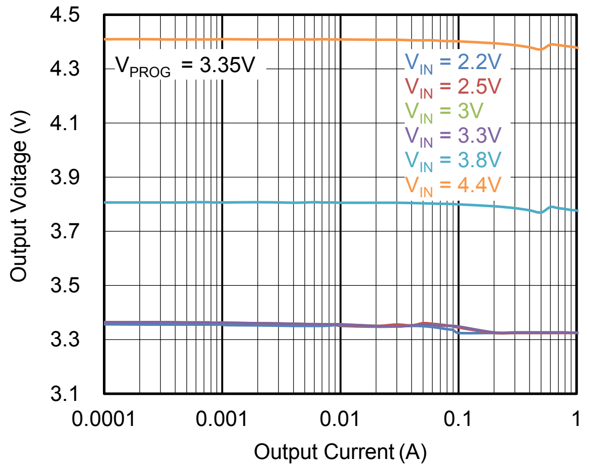
DC Output Voltage vs. Input Voltage



DC Output Voltage vs. Input Voltage

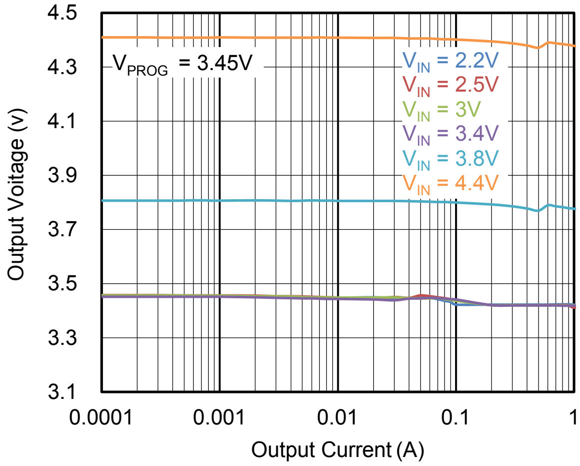


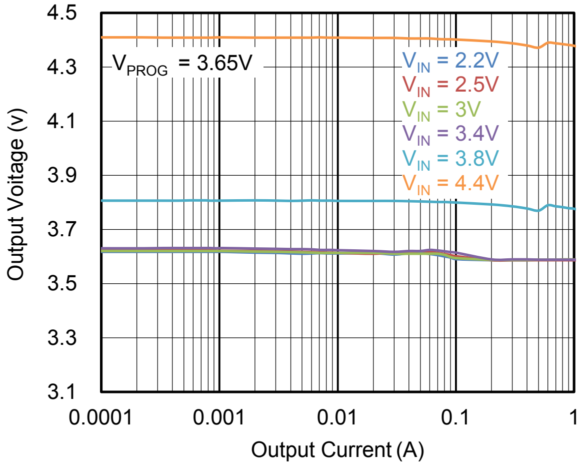
DC Output Voltage vs. Output Current

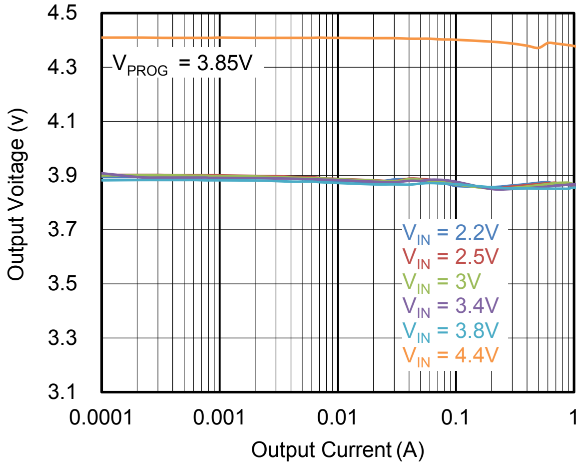


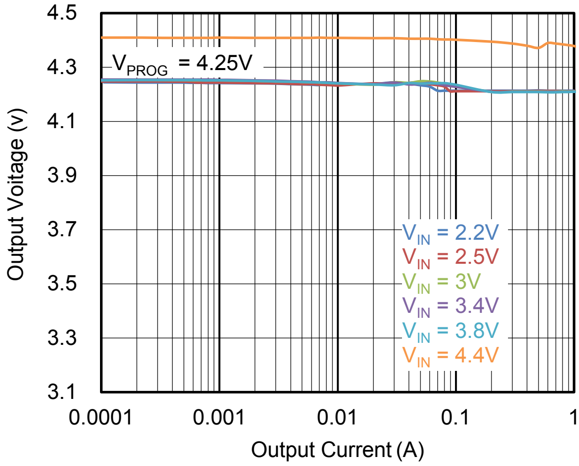
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

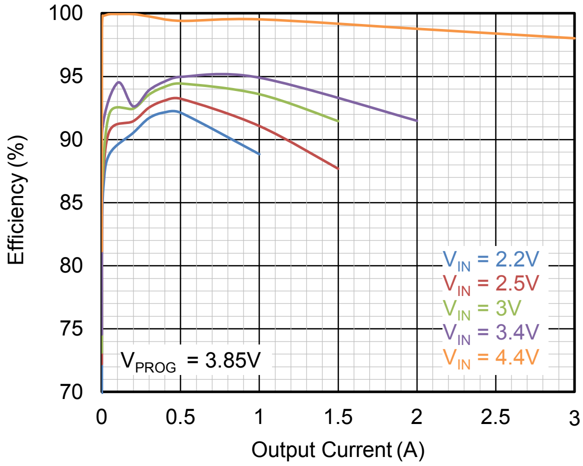
C_{IN} = 2×10μF, C_{OUT} = 4×10μF, L = 0.47μH, T_A = +25℃, unless otherwise noted.

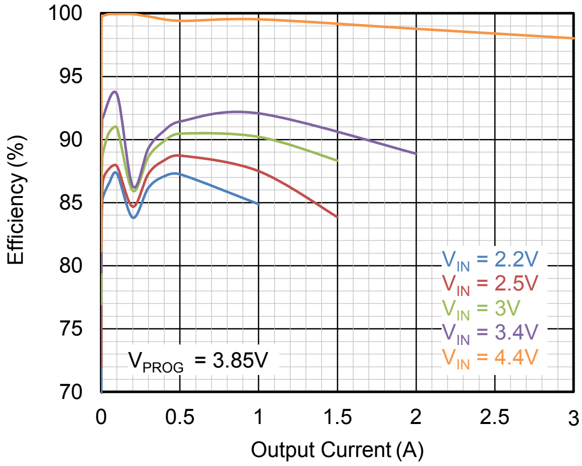








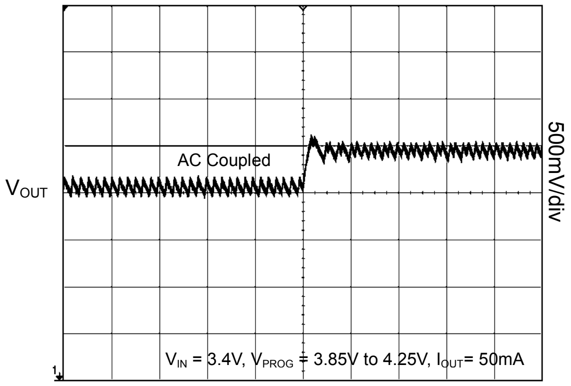




TYPICAL PERFORMANCE CHARACTERISTICS (continued)

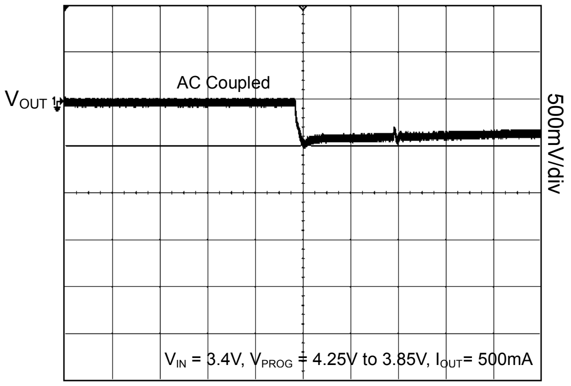
C_{IN} = 2×10μF, C_{OUT} = 4×10μF, L = 0.47μH, T_A = +25℃, unless otherwise noted.

Dynamic Voltage Management



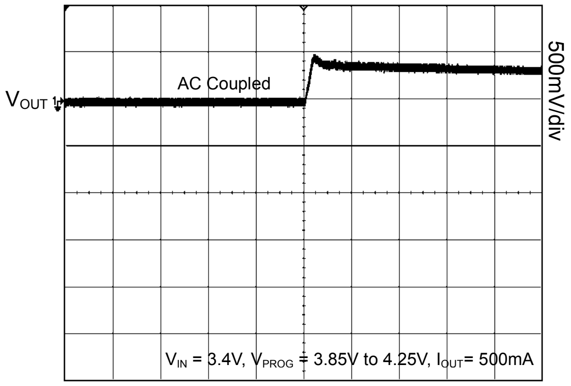
Time (500μs/div)

Dynamic Voltage Management



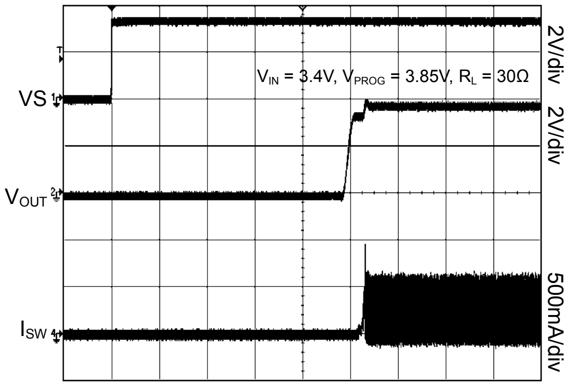
Time (500μs/div)

Dynamic Voltage Management



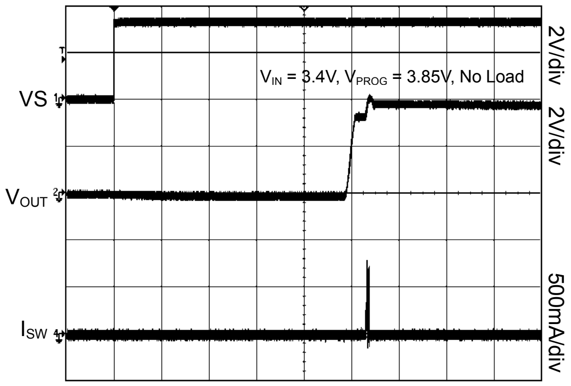
Time (500μs/div)

Start-Up



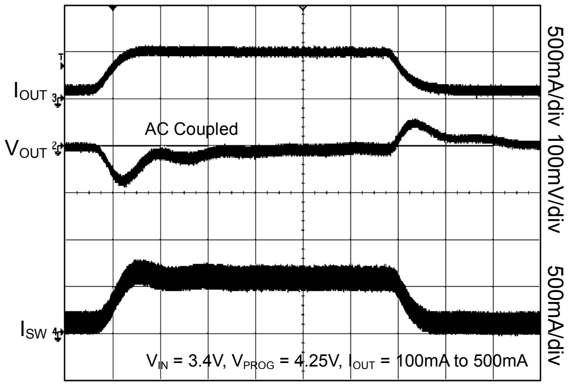
Time (2ms/div)

Start-Up



Time (2ms/div)

Load Transient Response

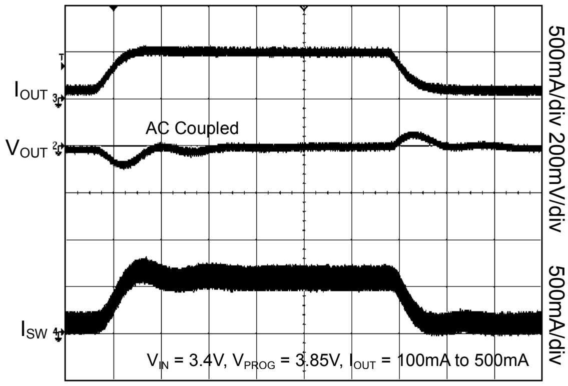


Time (50μs/div)

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

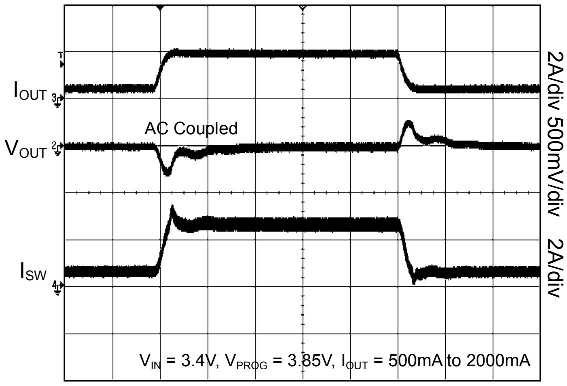
C_{IN} = 2×10μF, C_{OUT} = 4×10μF, L = 0.47μH, T_A = +25℃, unless otherwise noted.

Load Transient Response



Time (50μs/div)

Load Transient Response



Time (100μs/div)

FUNCTIONAL BLOCK DIAGRAM

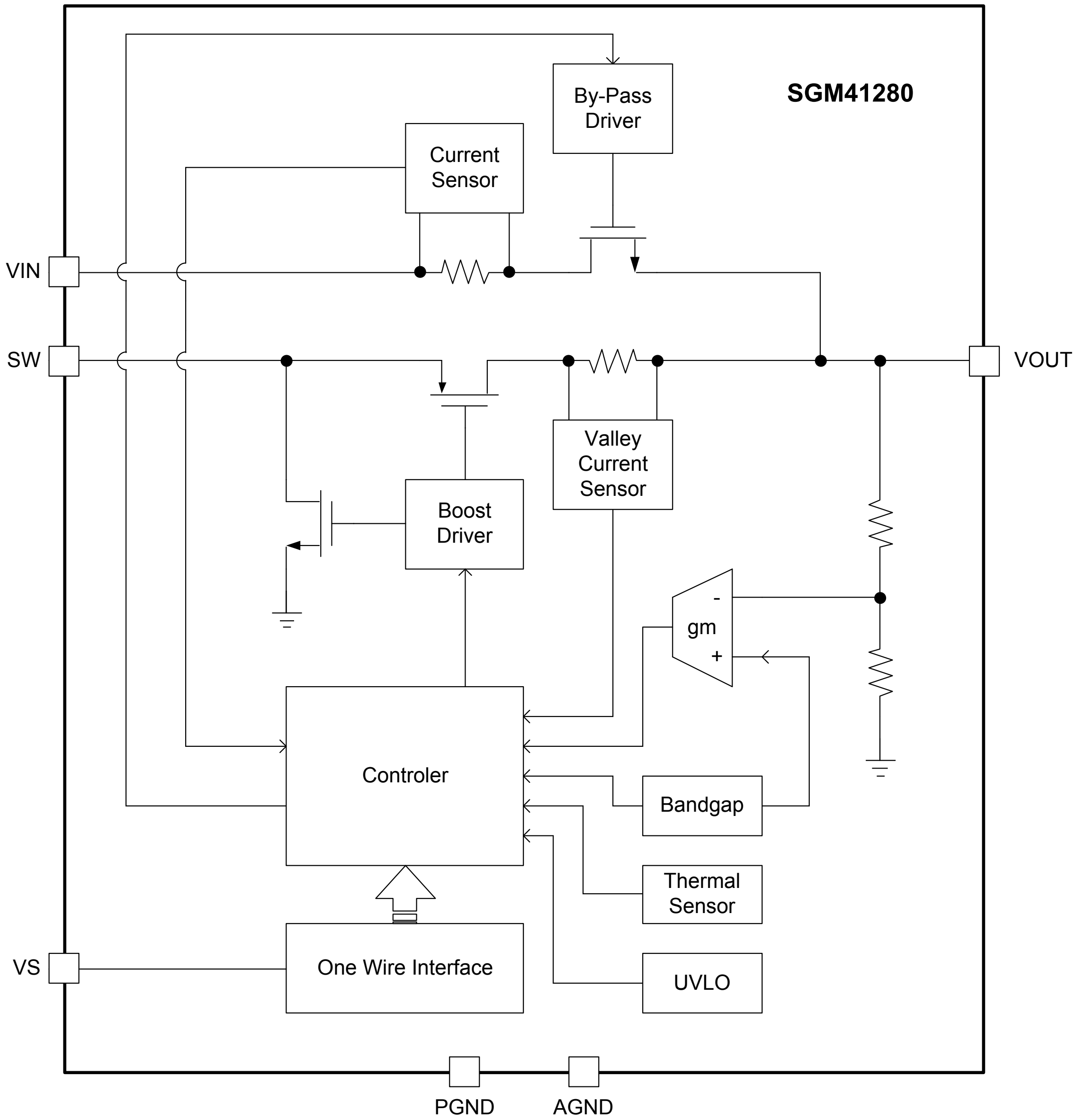


Figure 2. Block Diagram

OPERATION DESCRIPTION

The SGM41280 device provides a power supply solution for products powered by either by a Li-Ion, Nickel-Rich, Silicon Anode, Li-Ion or LiFePO4 battery. The voltage range is optimized for single-cell portable applications like in smart-phones or tablet PCs.

Acted as the high-power pre-regulator, the SGM41280 can implement the high density supply to overcome battery system current and voltage limitations. Used as high density power supply, the SGM41280 can facilitate high current WLED flash, WLED flash module, RF engine PMIC, audio PA etc. with maximum allowed output.

During operation, when the battery is at a good state-of-charge, a low-ohmic, high-efficient integrated pass- through path (Bypass Mode) connects the battery to the powered system. If the battery gets to a lower state of charge and its voltage becomes lower than the desired minimum system voltage, the device seamlessly transits into boost mode to utilize the full battery capacity.

Boost Mode

The SGM41280 uses a current-mode modulator with CCM and DCM operation. During CCM operation, the device maintains a switching frequency of about 2.5MHz. In light load operation, its frequency is reduced into Power-Save Mode.

Power-Save Mode

The SGM41280 integrates a power-save mode to improve efficiency at light load. In power-save mode the converter only operates when the output voltage trips below a set threshold voltage (about 1.01 × V_{PROG}). It ramps up the output voltage with several pulses and goes into power-save mode once the output voltage exceeds the set threshold voltage. The PFM mode is left and PWM mode entered in case the output current can not longer be supported in PFM mode (Figure 3).

Bypass Mode

The SGM41280 contains an internal switch for bypassing the dc/dc boost converter during bypass mode. When the input voltage is larger than the preset output voltage (V_{PROG}), the converter seamlessly transitions into 0% duty cycle operation and the bypass NMOSFET is fully enhanced. Entry in bypass mode is triggered by condition where V_{IN} > V_{PROG} and no switching has occurred.

During bypass operation, the output voltage follows the input voltage and will not fall below the programmed output voltage threshold (V_{PROG}) as the input voltage decreases. The output voltage drop during bypass mode depends on the load current and input voltage. The device consumes only a standby current of 14μA (typ).

Start-Up Mode

The device has an internal soft-start circuit that limits the inrush current during start-up. The first phase in the start-up procedure is to bias the output node close to the input level (so called pre-charge phase).In this operating mode, the device limits its output current to ca. 3500mA. If the output voltage still fails to reach its target after 1ms, a fault condition is declared. After waiting 10ms, a restart is attempted.

Thermal Shutdown

A thermal shutdown is implemented to prevent damages due to excessive heat and power dissipation. Typically, the thermal shutdown happens at a junction temperature of +165℃. When the thermal shutdown is triggered, the device stops switching until the junction temperature falls below typically +150℃, then the device starts switching again.

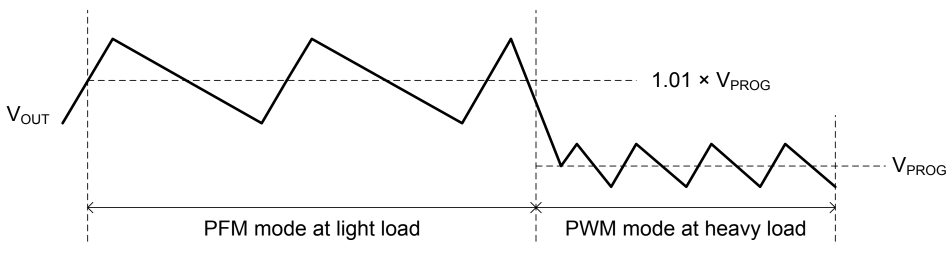


Figure 3. Power-Save Mode

OPERATION DESCRIPTION (continued)

Effective Pulse at VS Pin

If a change at VS pin recovers during t_{PULSE}, this change will be treated as a pulse. Please refer to Figure 4 for a graphical explanation.

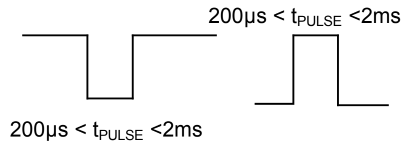


Figure 4. Effective Pulse at VS Pin

Program Output Voltage via VS Pin

After t_{BLK} + t_{SS} time since V_{IN} is higher than UVLO threshold, the signal added at VS pin is effective. If add 1 pulse at VS pin, and VS pin stays low for longer than t_{OFF}, the regulator will enter shutdown mode. The regulator can't be controlled during the $t_{OFF\text{-}HOLD}$ time after shutdown and VS pin must be high for at least t_{SS} time if attempts to restart the regulator. And the signal added at VS pin will be effective only after t_{SS} time. If VS pin stays high for longer than t_{STOP} after 1 pulse is added at VS pin, the output voltage will be the same as last set. If add 2-6 pulses at VS pin, and VS pin stays low for longer than t_{STOP}, output voltage will be set to default voltage. If VS pin stays high for longer than t_{STOP} after 2-6 pulses are added at VS pin, the output voltage will be set to V1, V2, V3, V4 and V5 respectively. Please refer to Figure 5 for a graphical explanation.

VS Control Enable and Shutdown

In order to enable the IC from shutdown mode, two conditions must be met:

1. VIN voltage is higher than UVLO threshold.

2. VS pin stays logic high for at least t_{BLK} + t_{SS} time. Pull VS pin low for longer than t_{OFF} time after no pulse or only 1 pulse is added at VS pin can shut down the IC.

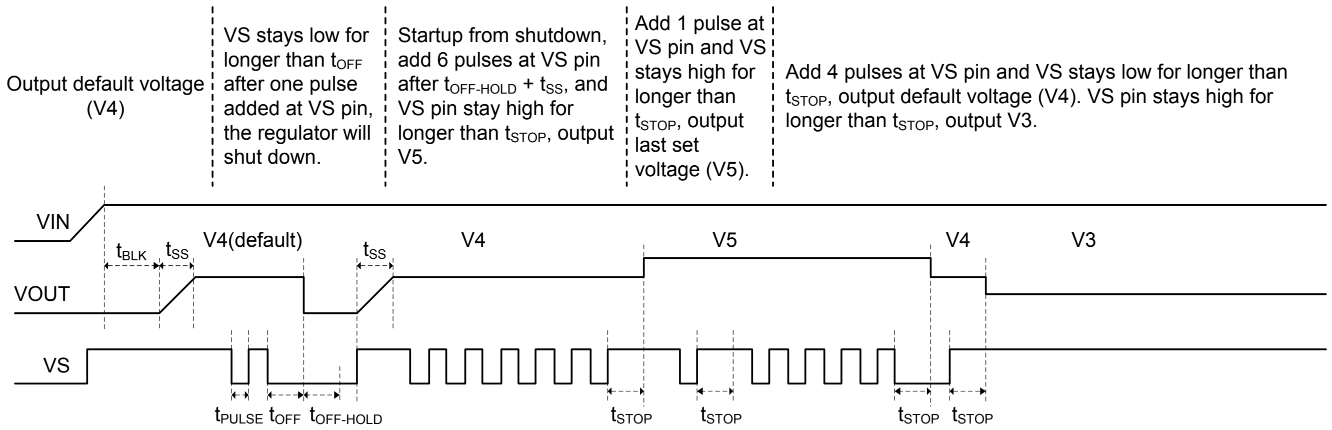


Figure 5. Program Output Voltage via VS Pin

APPLICATION INFORMATION

Inductor Selection

The recommended nominal inductance value is 0.47µH. SGM41280 employs valley-current limiting; peak inductor current can exceed 6A during overload conditions. Saturation effects cause the inductor current ripple to become higher under high loading as only valley of the inductor current ripple is controlled.

Output Capacitor

For the output capacitor, it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, using a smaller ceramic capacitor in parallel to the large one is highly recommended. This small capacitor should be placed as close as possible to the VOUT and GND pins of the IC.

To get an estimate of the recommended minimum output capacitance, Equation 1 can be used.

$$C_{MIN} = \frac{I_{OUT} \times (V_{OUT} - V_{IN})}{f \times \Delta V \times V_{OUT}} \quad (1)$$

Where f is the switching frequency which is 2.5MHz (typ.) and ΔV is the maximum allowed output ripple.

The total ripple is larger due to the ESR and ESL of the output capacitor. This additional component of the ripple can be calculated using Equation 2.

$$\Delta V_{OUT(ESR)} = ESR \times (\frac{I_{OUT}}{1 - D} + \frac{\Delta I_L}{2}) \quad (2)$$

$$\Delta V_{OUT(ESL)} = ESL \times (\frac{I_{OUT}}{1 - D} + \frac{\Delta I_L}{2} - I_{OUT}) \times \frac{1}{t_{SW(RISE)}} \quad (3)$$

$$\Delta V_{OUT(ESL)} = ESL \times (\frac{I_{OUT}}{1 - D} - \frac{\Delta I_L}{2} - I_{OUT}) \times \frac{1}{t_{SW(FALL)}} \quad (4)$$

with: I_{OUT} = output current of the application, D = duty cycle, ΔI_L = inductor ripple current, $t_{SW(RISE)}$ = switch node rise time, $t_{SW(FALL)}$ = switch node fall time, ESR = equivalent series resistance of the used output capacitor, ESL = equivalent series inductance of the used output capacitor.

An MLCC capacitor with twice the value of the calculated minimum should be used due to DC bias effects. This is required to maintain control loop stability. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from their wide variation in capacitance over temperature, become resistive at high frequencies. There are no additional requirements regarding minimum ESR. Larger capacitors cause lower output voltage ripple as well as lower output voltage drop during load transients.

In applications featuring high (pulsed) load currents (e.g. ≥2Amps), it is recommended to run the converter with a reasonable amount of effective output capacitance and low-ESL device, for instance x2 22µF X5R 6.3V (0603) MLCC capacitors connected in parallel with a 1µF X5R 6.3V (0306-2T) MLCC LL capacitor.

DC bias effect: high cap. ceramic capacitors exhibit DC bias effects, which have a strong influence on the device's effective capacitance. Therefore the right capacitor value has to be chosen carefully. Package size and voltage rating in combination with material are responsible for differences between the rated capacitor value and it's effective capacitance. For instance, a 10µF X5R 6.3V (0603) MLCC capacitor would typically show an effective capacitance of less than 5µF (under 3.5V bias condition, high temperature).

High values of output capacitance are mainly achieved by putting capacitors in parallel. This reduces the overall series resistance (ESR) to very low values. This results in almost no voltage ripple at the output and therefore the regulation circuit has no voltage drop to react on. Nevertheless to guarantee accurate output voltage regulation even with very low ESR the regulation loop can switch to a pure comparator regulation scheme.

APPLICATION INFORMATION (continued)

Input Capacitor

Multilayer ceramic capacitors are an excellent choice for input decoupling of the step-up converter as they have extremely low ESR and are available in small footprints. Input capacitors should be located as close as possible to the device. While a 10μF input capacitor is sufficient for most applications, larger values may be used to reduce input current ripple without limitations.

Take care when using only ceramic input capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the VIN pin. This ringing can couple to the output and be mistaken as loop instability or could even damage the part. Additional "bulk" capacitance (electrolytic or tantalum) should in this circumstance be placed between C_{IN} and the power source lead to reduce ringing that can occur between the inductance of the power source leads and C_{IN}.

Layout Guidelines

• For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies.
• If the layout is not carefully done, the regulator could show stability problems as well as EMI problems.
• Therefore, use wide and short traces for the main current path and for the power ground tracks.
• To minimize voltage spikes at the converter's output:
– Place the output capacitor(s) as close as possible to GND and VOUT, as shown in Figure 6.
– The input capacitor and inductor should also be placed as close as possible to the IC.
– Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise.
– Connect these ground nodes at any place close to the ground pins of the IC.
– Junction-to-ambient thermal resistance is highly application and board-layout dependent.
– It is suggested to maximize the pour area for all planes other than SW. Especially the ground pour should be set to fill available PWB surface area and tied to internal layers with a cluster of thermal vias.

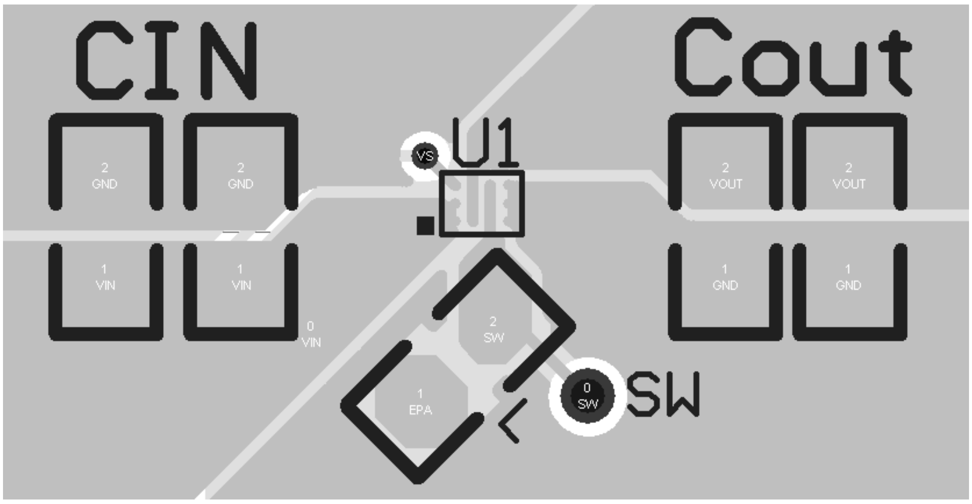
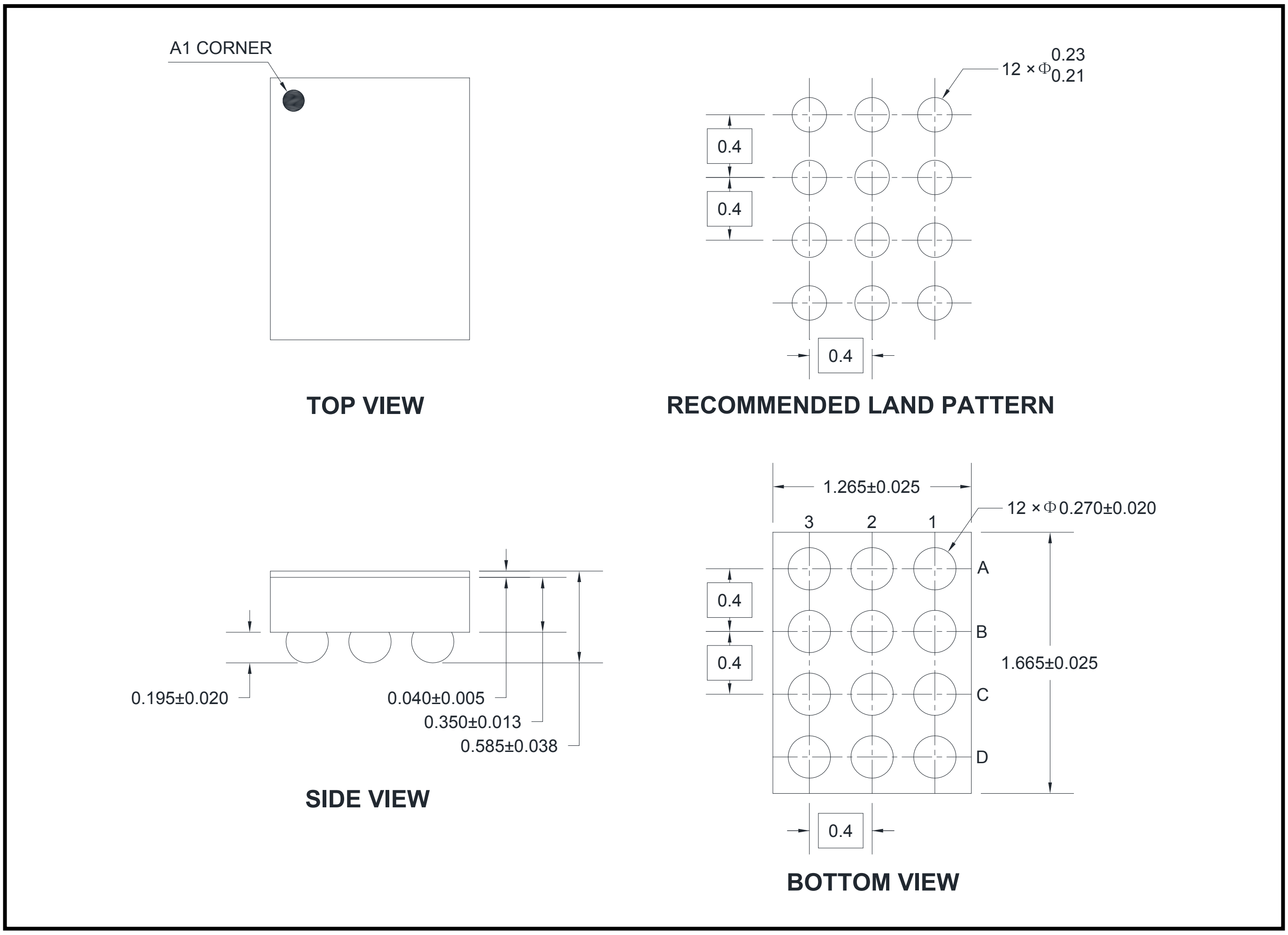


Figure 6. Suggested Layout

PACKAGE OUTLINE DIMENSIONS

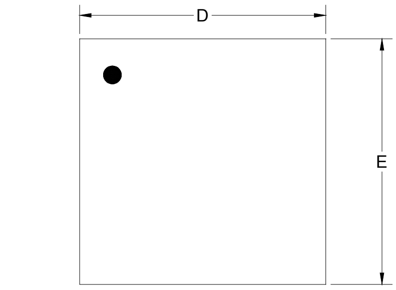
WLCSP-1.27×1.67-12B



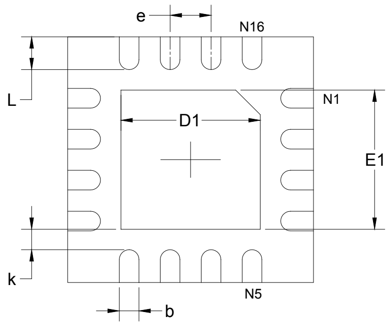
NOTE: All linear dimensions are in millimeters.

PACKAGE OUTLINE DIMENSIONS

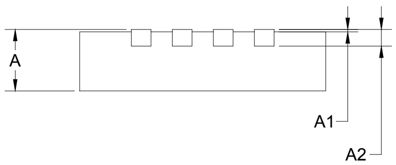
TQFN-3×3-16L



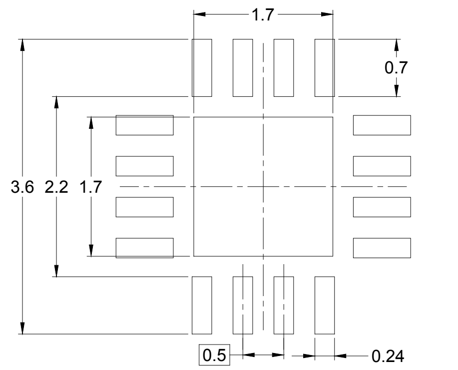
TOP VIEW



BOTTOM VIEW



SIDE VIEW

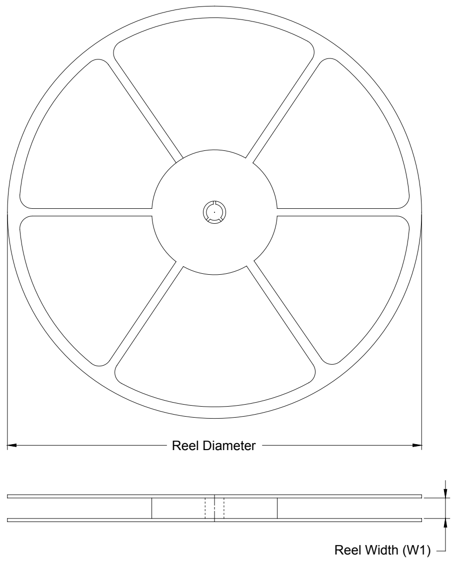


RECOMMENDED LAND PATTERN (Unit: mm)

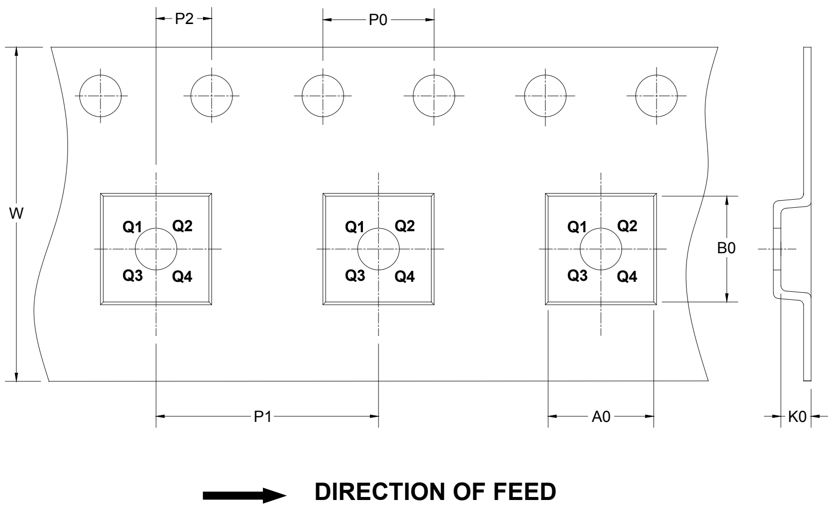
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E	2.900	3.100	0.114	0.122
E1	1.600	1.800	0.063	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



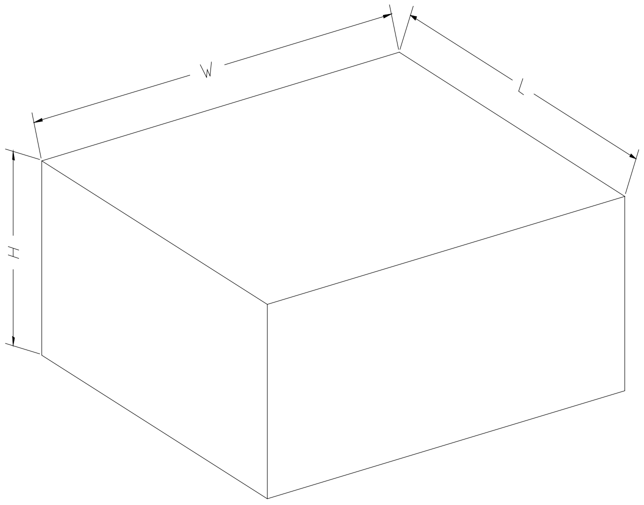
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-1.27×1.67-12B	7″	9.5	1.42	1.80	0.69	4.0	4.0	2.0	8.0	Q1
TQFN-3×3-16L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q2

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
7″ (Option)	368	227	224	8
7″	442	410	224	18
13″	386	280	370	5

DD0002