EFC6602R

N-Channel Power MOSFET
12V, 18A, 5.9mΩ, Dual EFCP

Features

- 2.5V drive
- Common-drain type
- 2KV ESD HBM
- Protection diode in
- Halogen free compliance

Specifications

Absolute Maximum Ratings at Ta=25°C

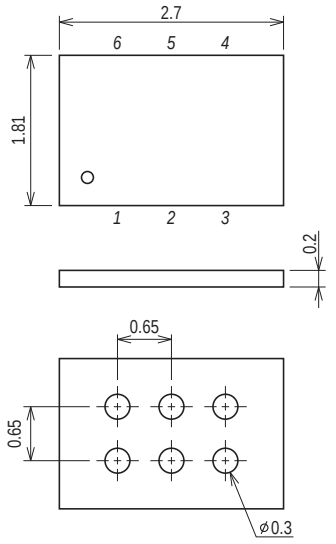
Parameter	Symbol	Conditions	Ratings	Unit
Source-to-Source Voltage	V_{SSS}		12	V
Gate-to-Source Voltage	V_{GSS}		±12	V
Source Current (DC)	I_S		18	A
Source Current (Pulse)	I_{SP}	PW≤10μs, duty cycle≤1%	60	A
Total Dissipation	P_T	When mounted on ceramic substrate (5000mm²×0.8mm)	2.0	W
Channel Temperature	Tch		150	°C
Storage Temperature	Tstg		−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Package Dimensions

unit : mm (typ)

7073-001



EFC6602R-TR

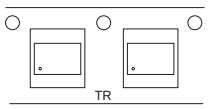
1 : Source1
2 : Gate1
3 : Source1
4 : Source2
5 : Gate2
6 : Source2

EFCP2718-6CE-020

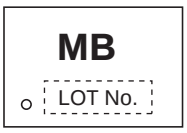
Product & Package Information

- Package : EFCP
- JEITA, JEDEC : -
- Minimum Packing Quantity : 5,000 pcs./reel

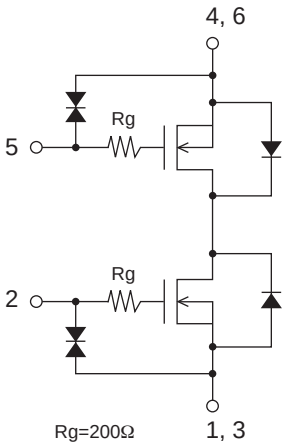
Taping Type : TR



Marking



Electrical Connection



Electrical Characteristics at Ta=25°C

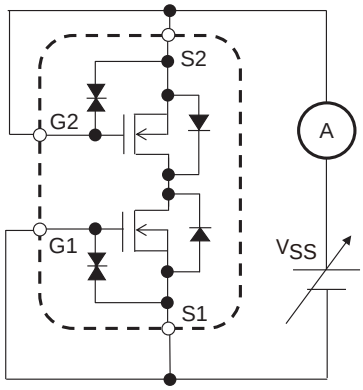
Parameter	Symbol	Conditions		Ratings			Unit
				min	typ	max	
Source-to-Source Breakdown Voltage	$V_{(BR)SSS}$	I_S=1mA, V_{GS}=0V	Test Circuit 1	12			V
Zero-Gate Voltage Source Current	I_{SSS}	V_{SS}=10V, V_{GS}=0V	Test Circuit 1			1	μA
Gate-to-Source Leakage Current	I_{GSS}	V_{GS}=±8V, V_{SS}=0V	Test Circuit 2			±1	μA
Cutoff Voltage	V_{GS}(off)	V_{SS}=6V, I_S=1mA	Test Circuit 3	0.5		1.3	V
Forward Transfer Admittance	| yfs |	V_{SS}=6V, I_S=3A	Test Circuit 4		13		S
Static Source-to-Source On-State Resistance	R_{SS}(on)1	I_S=3A, V_{GS}=4.5V	Test Circuit 5	3.1	4.5	5.9	mΩ
	R_{SS}(on)2	I_S=3A, V_{GS}=4.0V	Test Circuit 5	3.3	4.8	6.3	mΩ
	R_{SS}(on)3	I_S=3A, V_{GS}=3.8V	Test Circuit 5	3.5	5	6.5	mΩ
	R_{SS}(on)4	I_S=3A, V_{GS}=3.1V	Test Circuit 5	4.0	5.8	8.2	mΩ
	R_{SS}(on)5	I_S=3A, V_{GS}=2.5V	Test Circuit 5	5.2	7.5	11	mΩ
Turn-ON Delay Time	t_d(on)	V_{DD}=6V, V_{GS}=4.5V, I_S=3A	Test Circuit 7		530		ns
Rise Time	t_r				2100		ns
Turn-OFF Delay Time	t_d(off)				6200		ns
Fall Time	t_f				5500		ns
Total Gate Charge	Qg	V_{DD}=6V, V_{GS}=4.5V, I_S=18A	Test Circuit 8		55		nC
Forward Source-to-Source Voltage	$V_{F(S-S)}$	I_S=3A, V_{GS}=0V	Test Circuit 6		0.76	1.2	V

Ordering Information

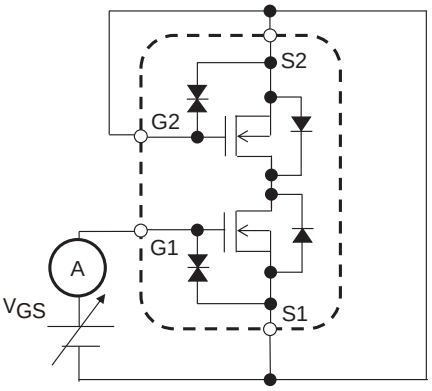
Device	Package	Shipping	memo
EFC6602R-TR	EFCP	5,000pcs./reel	Pb Free and Halogen Free

Test circuits are example of measuring FET1 side

Test Circuit 1
I_{SSS}

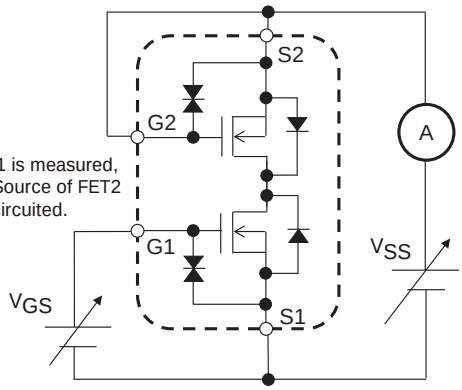


Test Circuit 2
I_{GSS}



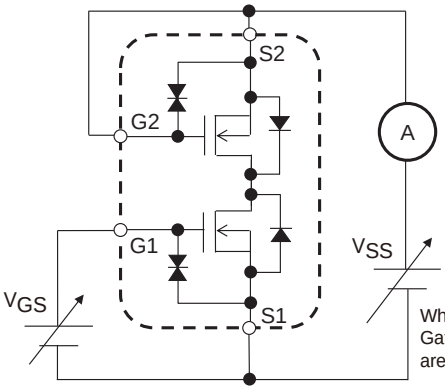
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 3
$V_{GS(off)}$



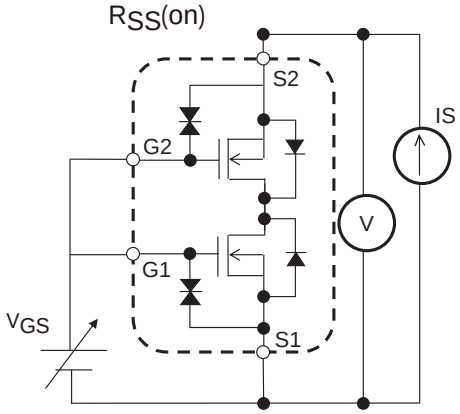
When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 4
$|y_{fs}|$

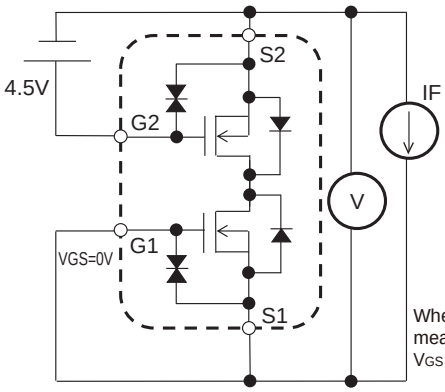


When FET1 is measured, Gate and Source of FET2 are short-circuited.

Test Circuit 5
$R_{SS(on)}$

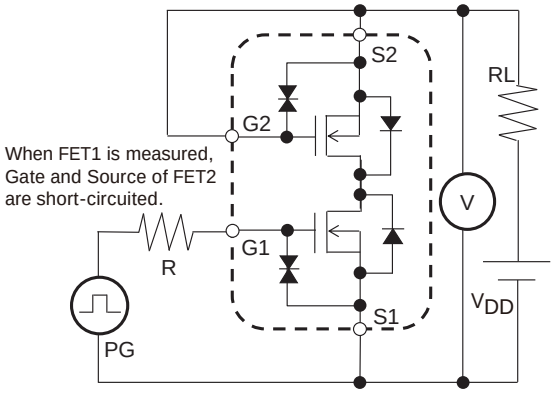


Test Circuit 6
$V_{F(S-S)}$



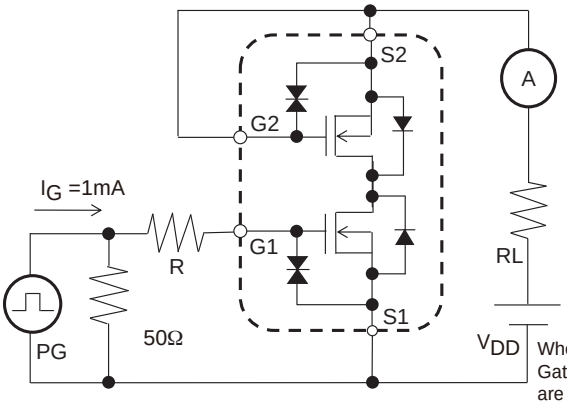
When FET1 is measured,+4.5V is added to V_{GS} of FET2.

Test Circuit 7
$t_{d(on)}$, t_r, $t_{d(off)}$, t_f

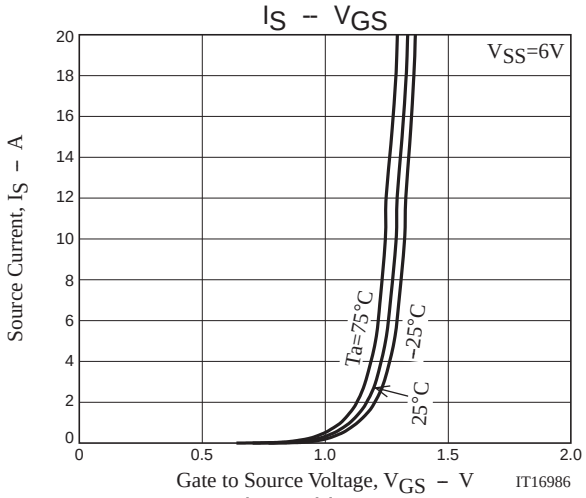


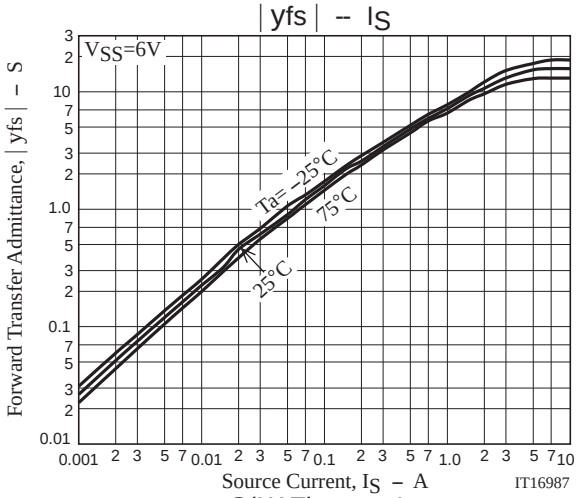
When FET1 is measured, Gate and Source of FET2 are short-circuited.

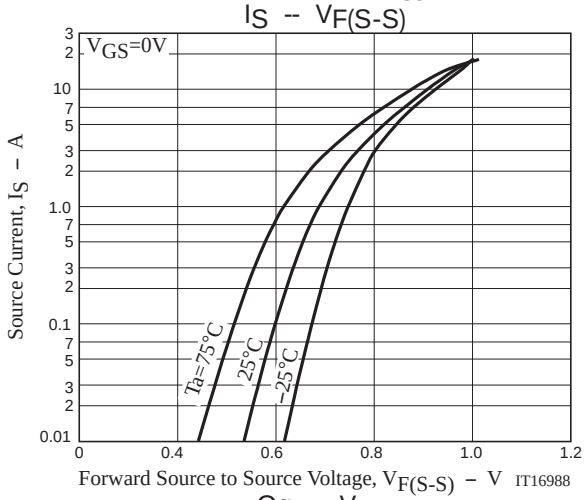
Test Circuit 8
Qg

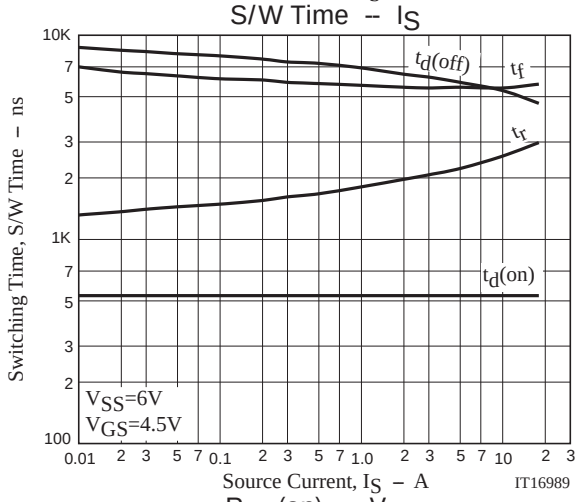


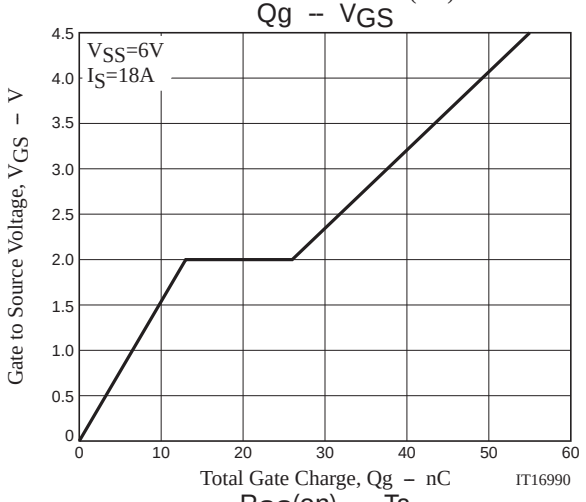
When FET1 is measured, Gate and Source of FET2 are short-circuited.

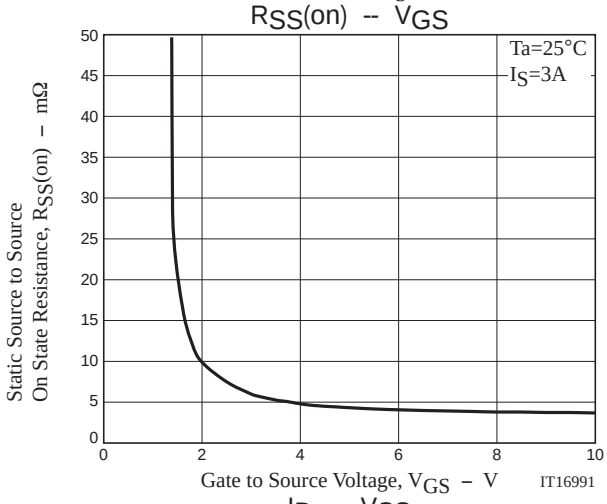

IS – VGS
VSS=6V
Ta=75°C
25°C
–25°C
Source Current, IS – A
Gate to Source Voltage, VGS – V
IT16986

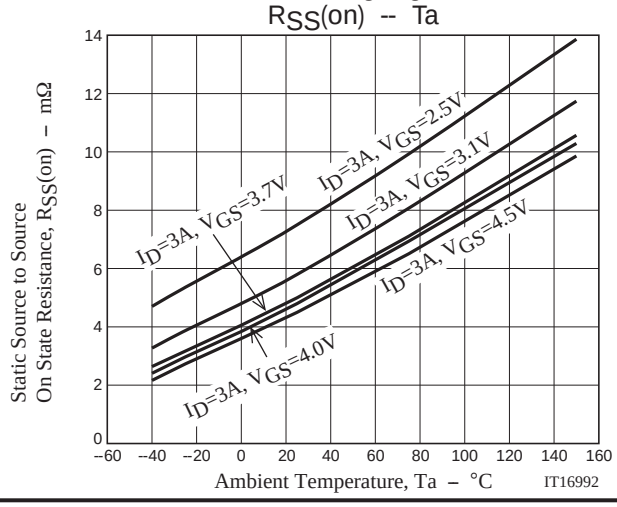

| yfs | – IS
VSS=6V
Ta= –25°C
75°C
25°C
Forward Transfer Admittance, | yfs | – S
Source Current, IS – A
IT16987

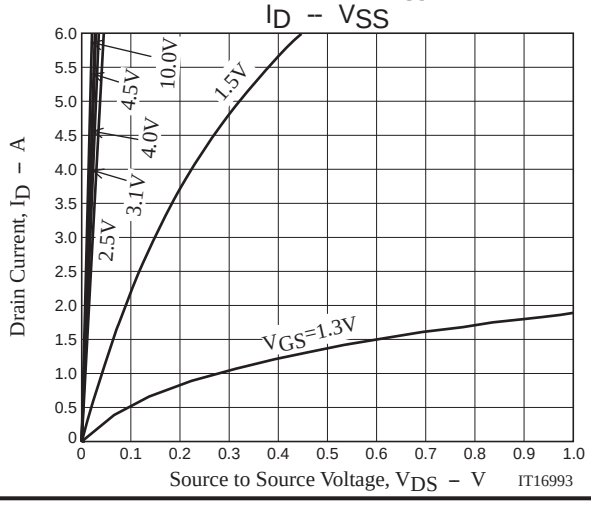

IS – VF(S-S)
VGS=0V
Ta=75°C
25°C
–25°C
Source Current, IS – A
Forward Source to Source Voltage, VF(S-S) – V
IT16988


S/W Time – IS
td(off)
tf
tr
td(on)
VSS=6V
VGS=4.5V
Switching Time, S/W Time – ns
Source Current, IS – A
IT16989

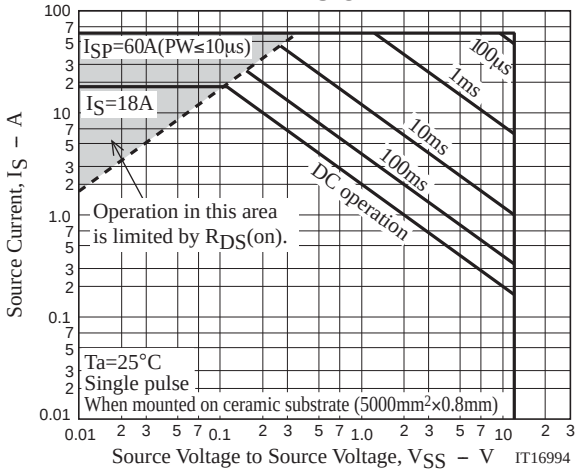

Qg – VGS
VSS=6V
IS=18A
Gate to Source Voltage, VGS – V
Total Gate Charge, Qg – nC
IT16990


RSS(on) – VGS
Ta=25°C
IS=3A
Static Source to Source
On State Resistance, RSS(on) – mΩ
Gate to Source Voltage, VGS – V
IT16991

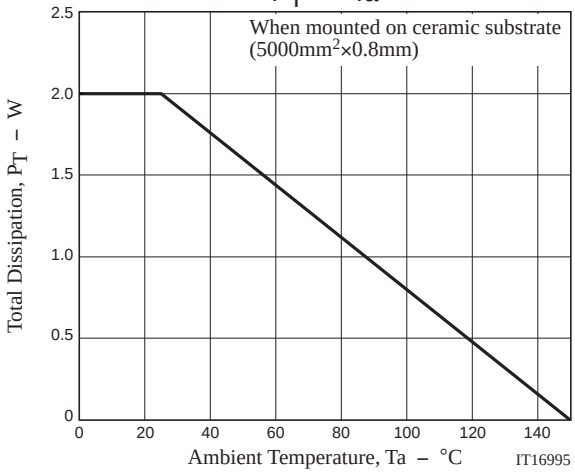

RSS(on) – Ta
ID=3A, VGS=3.7V
ID=3A, VGS=2.5V
ID=3A, VGS=3.1V
ID=3A, VGS=4.5V
ID=3A, VGS=4.0V
Static Source to Source
On State Resistance, RSS(on) – mΩ
Ambient Temperature, Ta – °C
IT16992


ID – VSS
10.0V
4.5V
4.0V
3.1V
2.5V
1.5V
VGS=1.3V
Drain Current, ID – A
Source to Source Voltage, VDS – V
IT16993

ASO


ISP=60A(PW≤10μs)
IS=18A
100μs
1ms
10ms
100ms
DC operation
Operation in this area
is limited by RDS(on).
Ta=25°C
Single pulse
When mounted on ceramic substrate (5000mm2×0.8mm)
Source Current, IS – A
Source Voltage to Source Voltage, VSS – V
IT16994

PT – Ta

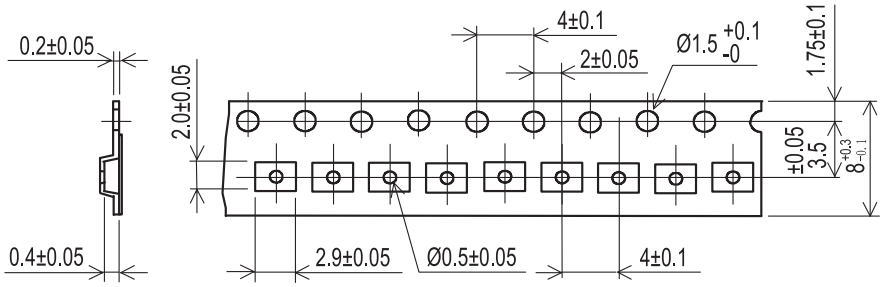

When mounted on ceramic substrate
(5000mm2×0.8mm)
Total Dissipation, PT – W
Ambient Temperature, Ta – °C
IT16995

Taping Specification

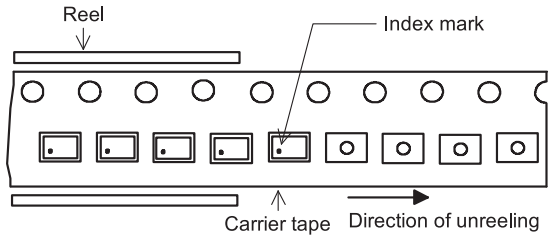
EFC6602R-TR

1.Taping Configuration

1-1 .Carrier Tape Size (unit:mm)

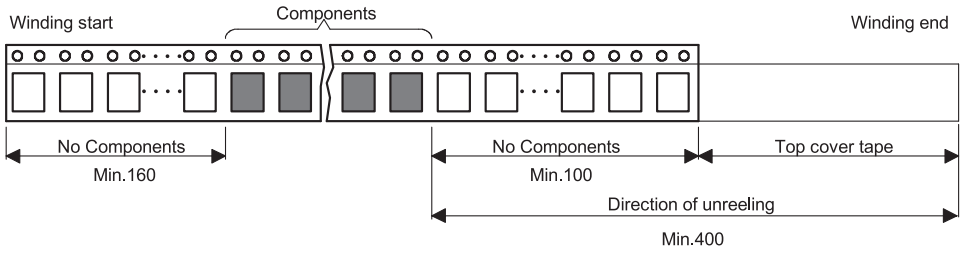


1-2 .Device Placement Direction



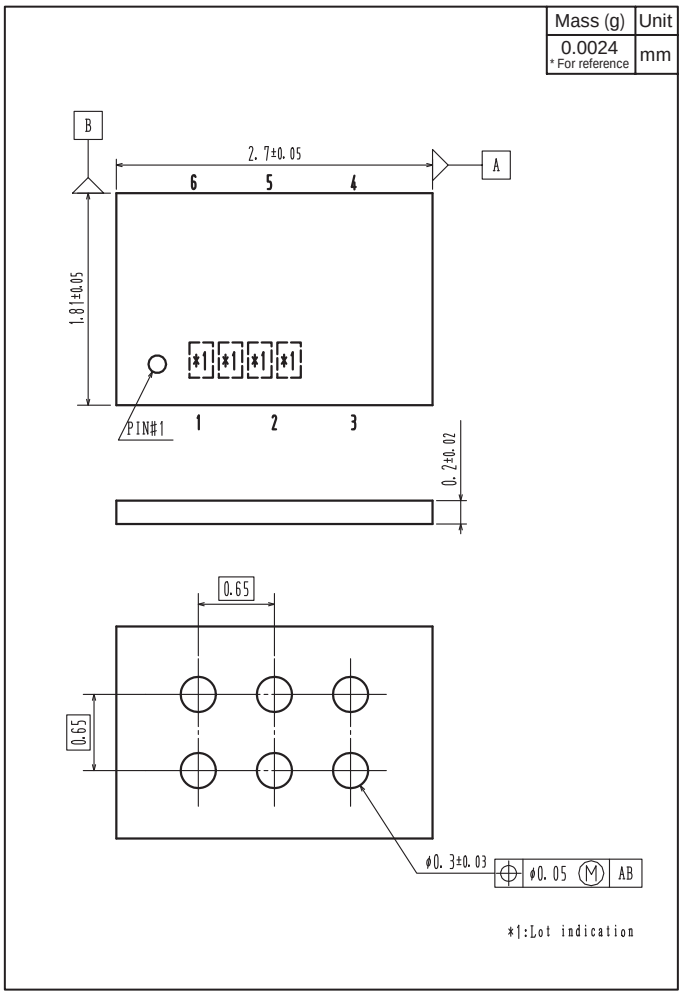
Packing type·····TR

1-3 .Leader portion and Trailer portion (unit:mm)



Outline Drawing

EFC6602R-TR



Land Pattern Example