

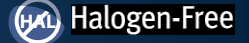
# EPC2212 - Automotive 100 V (D-S) Enhancement Mode Power Transistor

$V_{DS}$ , 100 V

$R_{DS(on)}$ , 13.5 m $\Omega$

$I_D$ , 18 A

AEC-Q101



Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

## Maximum Ratings

PARAMETER		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage (Continuous)	100	V
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ )	18	A
	Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300 \mu\text{s}$ )	75	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
$T_J$	Operating Temperature	-40 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-40 to 150	

## Thermal Characteristics

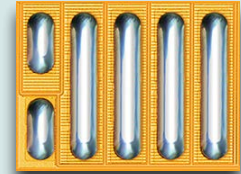
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	4	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	69	

## Static Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$ , $I_D = 250 \mu\text{A}$	100			V
$I_{DSS}$	Drain-Source Leakage	$V_{DS} = 100 \text{ V}$ , $V_{GS} = 0 \text{ V}$		10	250	$\mu\text{A}$
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 6 \text{ V}$ , $T_J = 25^\circ\text{C}$		0.005	1.8	$\text{mA}$
	Gate-to-Source Forward Leakage <sup>#</sup>	$V_{GS} = 6 \text{ V}$ , $T_J = 125^\circ\text{C}$		0.015	3	$\text{mA}$
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		10	250	$\mu\text{A}$
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 3 \text{ mA}$	0.7	1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$ , $I_D = 11 \text{ A}$		10	13.5	$\text{m}\Omega$
$V_{SD}$	Source-Drain Forward Voltage	$I_S = 0.5 \text{ A}$ , $V_{GS} = 0 \text{ V}$		1.5		V

All measurements were done with substrate connected to source.

<sup>#</sup> Defined by design. Not subject to production test.



EPC2212 eGaN<sup>®</sup> FETs are supplied only in passivated die form with solder bars. Die size: 2.1 x 1.6 mm

## Applications

- Lidar/Pulsed Power Applications
- High Power Density DC-DC Converters
- Class-D Audio
- High Intensity Headlamps

## Benefits

- Ultra High Efficiency
- Ultra Low  $R_{DS(on)}$
- Ultra Low  $Q_G$
- Ultra Small Footprint

**Dynamic Characteristics ( $T_j = 25^\circ\text{C}$  unless otherwise stated)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{ISS}$	Input Capacitance <sup>#</sup>	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		339	407	pF
$C_{RSS}$	Reverse Transfer Capacitance			3		
$C_{OSS}$	Output Capacitance <sup>#</sup>			238	357	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0\text{ V}$		292		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			359		
$R_G$	Gate Resistance			0.4		$\Omega$
$Q_G$	Total Gate Charge <sup>#</sup>	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 11\text{ A}$		3.2	4	nC
$Q_{GS}$	Gate-to-Source Charge	$V_{DS} = 50\text{ V}, I_D = 11\text{ A}$		0.9		
$Q_{GD}$	Gate-to-Drain Charge			0.6		
$Q_{G(TH)}$	Gate Charge at Threshold			0.55		
$Q_{OSS}$	Output Charge <sup>#</sup>	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		18	27	
$Q_{RR}$	Source-Drain Recovery Charge			0		

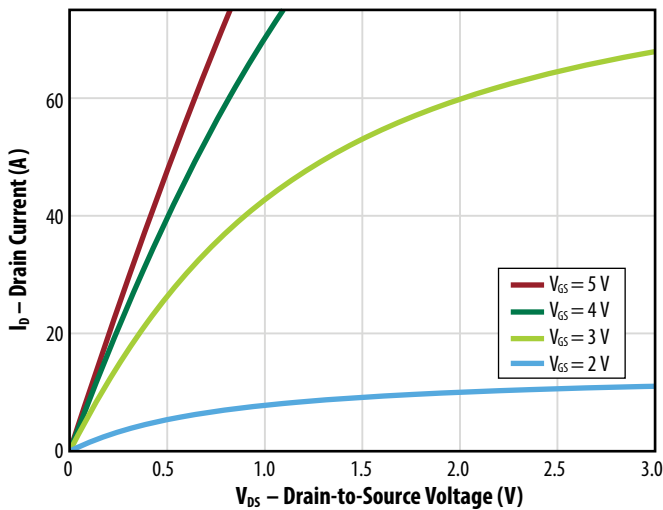
All measurements were done with substrate connected to source.

<sup>#</sup> Defined by design. Not subject to production test.

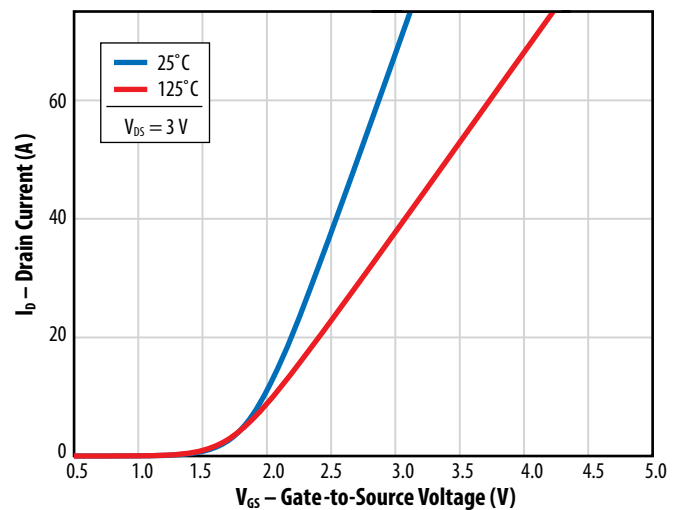
Note 2:  $C_{OSS(ER)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

Note 3:  $C_{OSS(TR)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

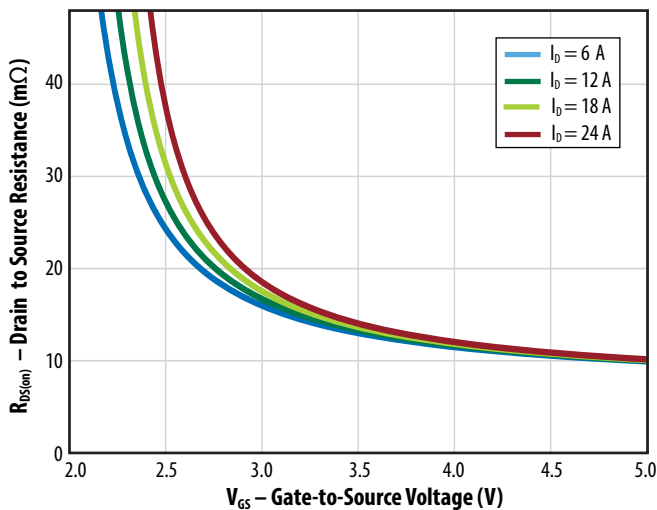
**Figure 1: Typical Output Characteristics at 25°C**



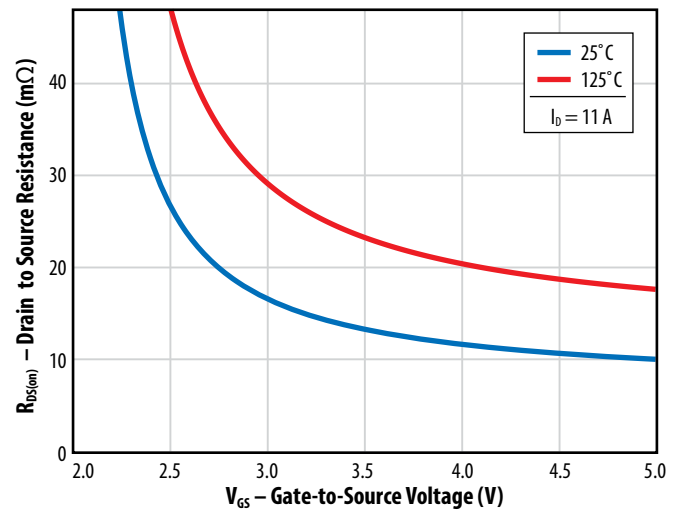
**Figure 2: Transfer Characteristics**



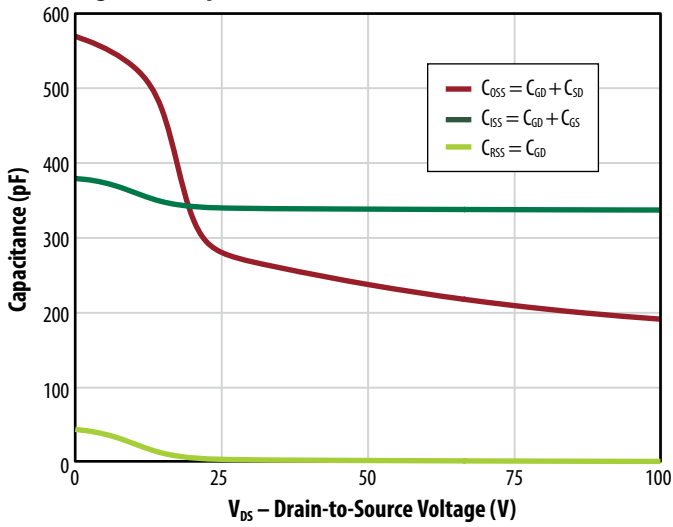
**Figure 3:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents**



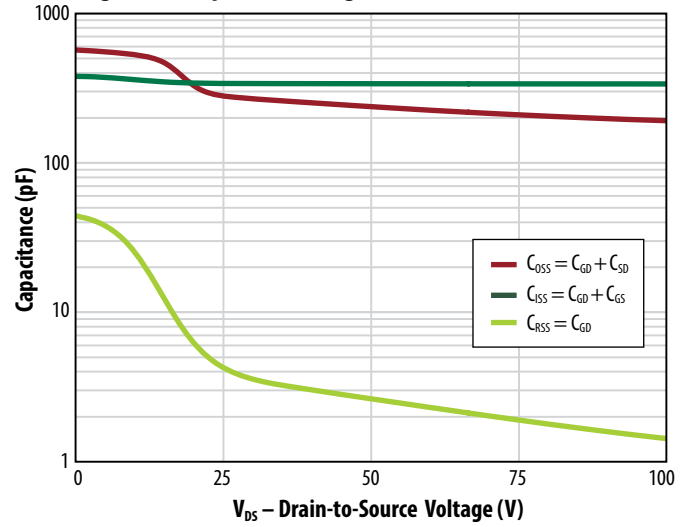
**Figure 4:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures**



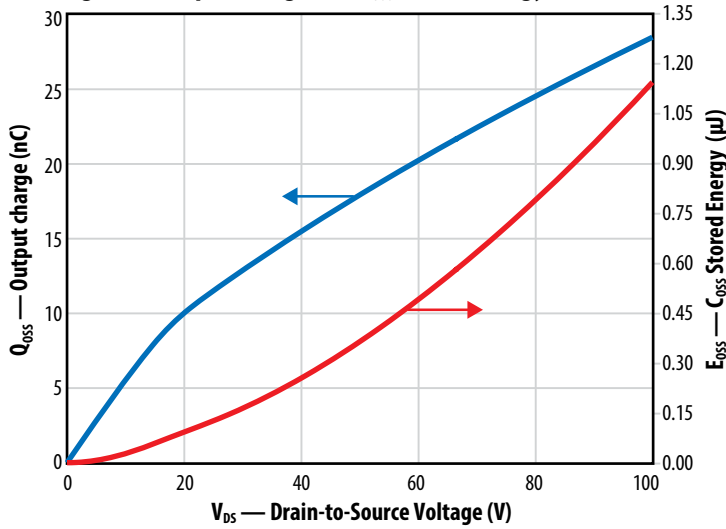
**Figure 5a: Capacitance (Linear Scale)**



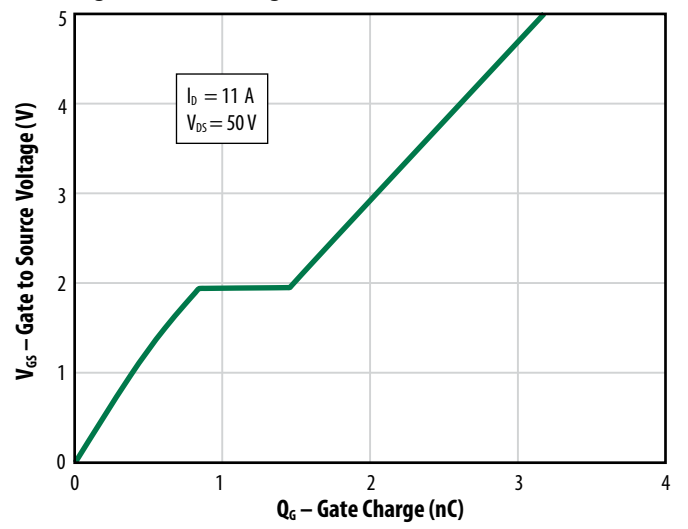
**Figure 5b: Capacitance (Log Scale)**



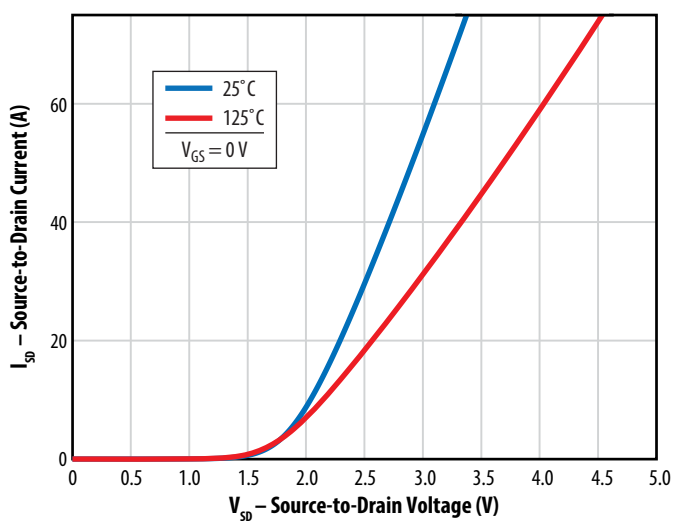
**Figure 6: Output Charge and  $C_{OSS}$  Stored Energy**



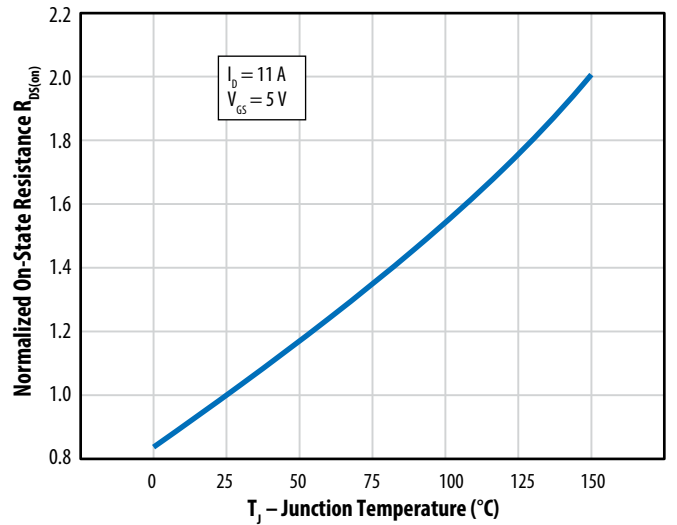
**Figure 7: Gate Charge**



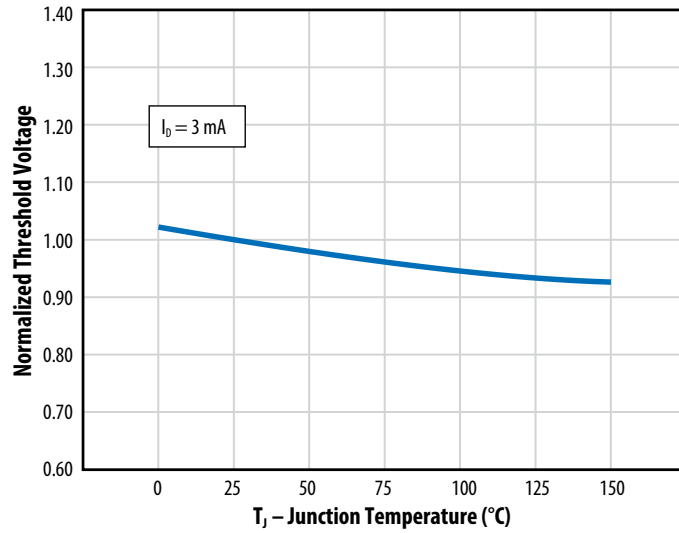
**Figure 8: Reverse Drain-Source Characteristics**



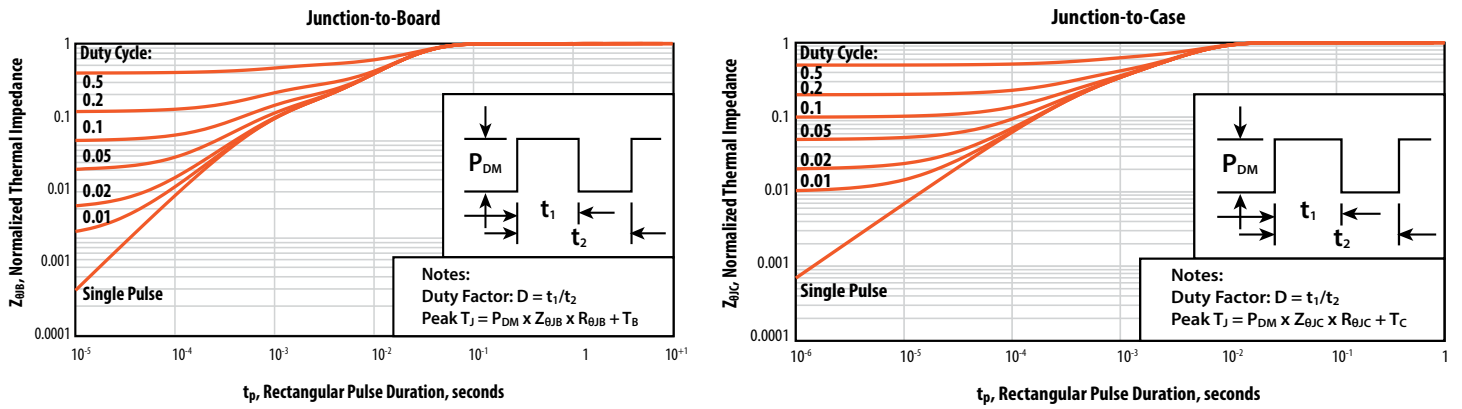
**Figure 9: Normalized On-State Resistance vs. Temperature**



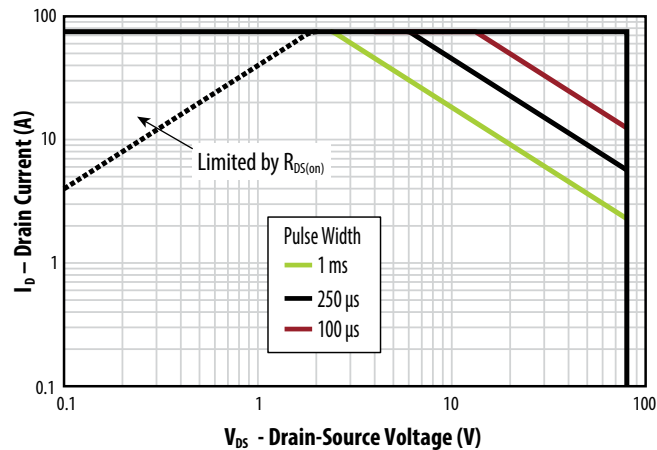
**Figure 10: Normalized Threshold Voltage vs. Temperature**



**Figure 11: Transient Thermal Response Curves**

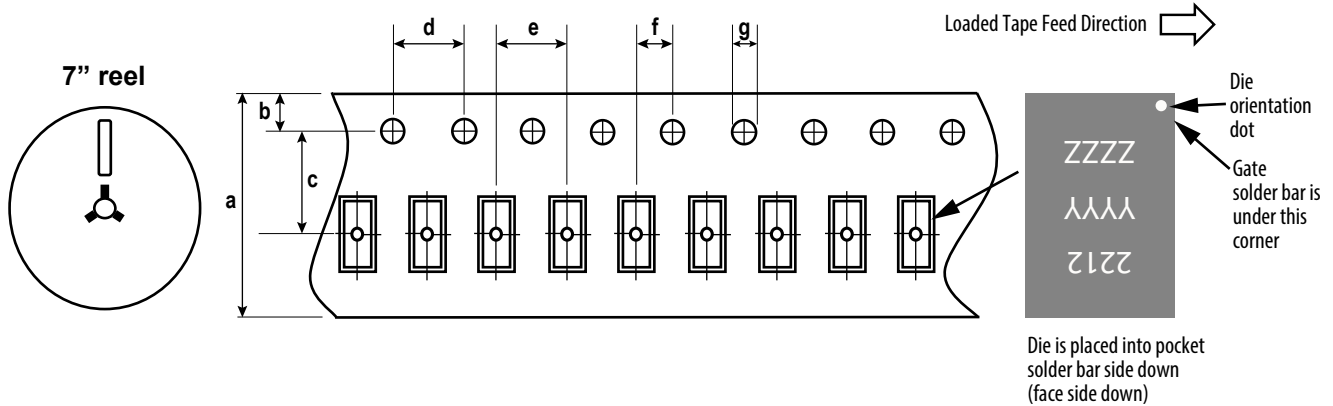


**Figure 12: Safe Operating Area**



## TAPE AND REEL CONFIGURATION

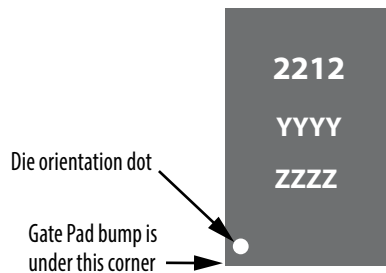
4mm pitch, 8mm wide tape on 7" reel



Dimension (mm)	EPC2212 (note 1)		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.  
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

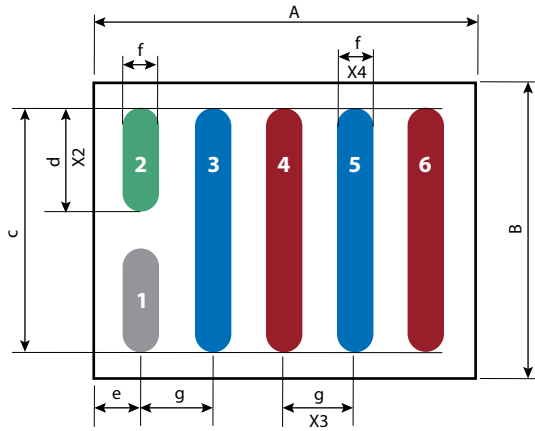
## DIE MARKINGS



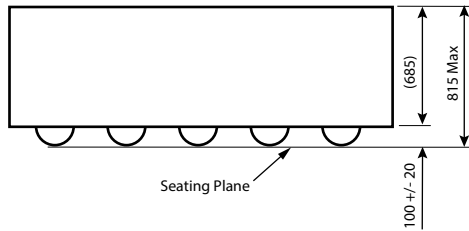
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC2212	2212	YYYY	ZZZZ

## DIE OUTLINE

Solder Bar View



Side View



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	2076	2106	2136
B	1602	1632	1662
c	1379	1382	1385
d	577	580	583
e	235	250	265
f	195	200	205
g	400	400	400

Pad no. 1 is Gate;

Pads no. 3, 5 are Drain;

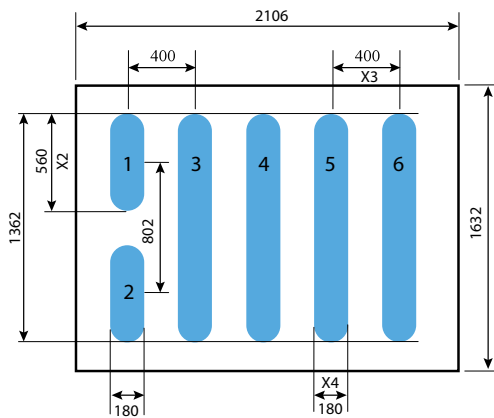
Pads no. 4, 6 are Source;

Pad no. 2 is Substrate.\*

\*Substrate pin should be connected to Source

## RECOMMENDED LAND PATTERN

(units in  $\mu\text{m}$ )



The land pattern is solder mask defined.

Pad no. 1 is Gate;

Pads no. 3, 5 are Drain;

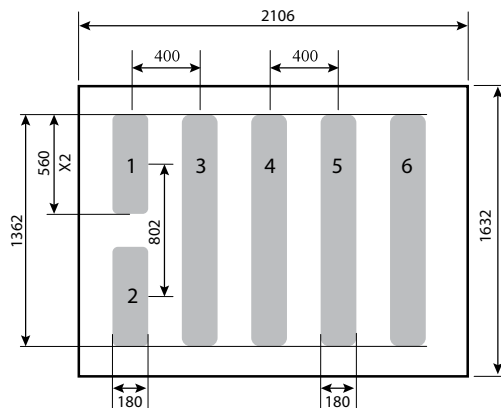
Pads no. 4, 6 are Source;

Pad no. 2 is Substrate.\*

\*Substrate pin should be connected to Source

## RECOMMENDED STENCIL DRAWING

(measurements in  $\mu\text{m}$ )



Recommended stencil should be 4mil (100  $\mu\text{m}$ )

thick, must be laser cut, opening per drawing.

The corner has a radius of R60

Intended for use with SAC305 Type 3 solder,  
reference 88.5% metals content.

Additional assembly resources available at