# 3A Sink and Source DDR Termination Regulator

## Features

- VIN Voltage: Supports 2.5V or 3.3V Power Rail
- VLDOIN Voltage Range: 1.1V to 3.5V
- Sink and Source Termination Regulator Includes Droop Compensation
- PGOOD to Monitor Output Regulation
- Remote Sensing (VOSNS)
- REFIN Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider
- ±25mA Buffered Reference (REFOUT)
- Built-in Soft Start, UVLO, and OCL
- Supports DDR, DDR2, DDR3, DDR3L, Low-Power DDR3, and DDR4 VTT Applications
- Thermal Shutdown

## Application

- Memory Termination Regulator for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4
- Notebooks, Desktops, and Servers
- Telecom ,Datacom and Base Stations
- LCD-TVs and PDP-TVs
- Copiers and Printers, Set-Top Boxes

## Description

The TMI62033 is a 3A sink and source double data rate (DDR) termination regulator. It supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4 VTT bus termination.

The TMI62033 maintains a fast transient response and requires a minimum output capacitance of only 20μF for low-cost, low-noise systems where space is a key consideration.

In addition, the TMI62033 provides an open-drain PGOOD signal to monitor the output regulation for VTT regulation indication and an EN signal that can be used to discharge VTT for DDR applications.

The TMI62033 is available in the thermally efficient 10-pin 3x3 DFN thermal pad package, and is rated both Green and Pb-free.

## Typical Application

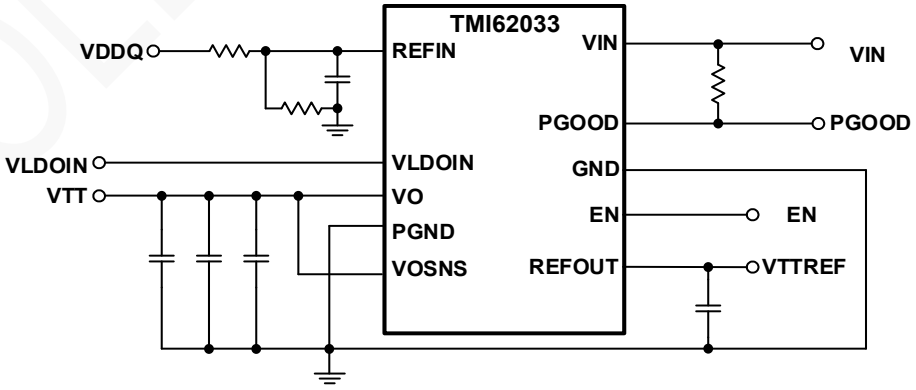
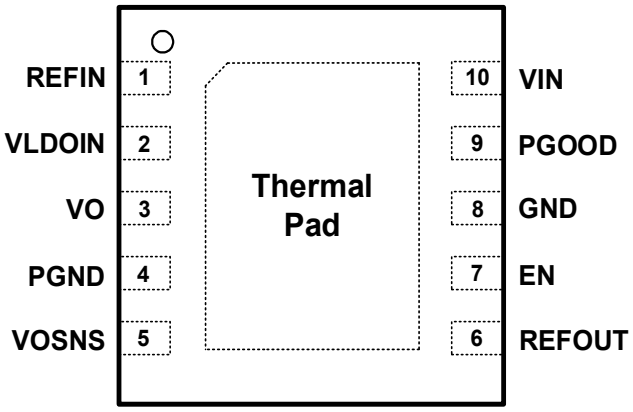



**Figure 1. TMI62033 Typical Application Circuit**

## Package




**Top View**

**DFN3x3-10**

**Top Marking: T62033/XXXXX (T62033: Device Code, XXXXX: Inside Code)**

## Order Information

| Part Number | Package | Top Marking | Quantity/Reel |
|---|---|---|---|
| TMI62033 | DFN3x3-10 | T62033<br>XXXXX | 5000 |

TMI62033 devices are Pb-free and RoHS compliant.

## Pin Functions

| Pin | Name | Function |
|---|---|---|
| 1 | REFIN | Reference input pin. |
| 2 | VLDOIN | LDO power supply input pin. |
| 3 | VO | LDO power output pin. |
| 4 | PGND | Power ground for the LDO. |
| 5 | VOSNS | Voltage sense input for the LDO. Connect to positive terminal of the output capacitor or the load. |
| 6 | REFOUT | Reference output. Connect to GND through 0.1μF ceramic capacitor. |
| 7 | EN | For DDR VTT application. For any other application, use the EN pin as the ON/OFF function. |
| 8 | GND | Ground pin. |
| 9 | PGOOD | Open-drain, power-good output pin. |
| 10 | VIN | 2.5V/3.3V Power supply input pin. A 1μF or larger ceramic capacitor from IN to ground (as close as possible to VIN pin) is required to reduce the jitter from previous-stage power supply. |
| Thermal Pad | | Thermal Pad must be connected to a large-area ground plane to maximum the thermal performance. |

## Absolute Maximum Ratings (Note 1)

| Parameter | Min | Max | Unit |
|---|---|---|---|
| REFIN, VIN, VLDOIN, VOSNS Voltage | -0.3 | 3.6 | V |
| EN Voltage | -0.3 | 6.5 | V |
| PGND to GND | -0.3 | 0.3 | V |
| REFOUT, VO Voltage | -0.3 | 3.6 | V |
| PGOOD Voltage | -0.3 | 6.5 | V |
| Storage Temperature Range | -55 | 150 | °C |
| Junction Temperature (Note2) | -40 | 150 | °C |

## ESD Rating (Note2)

| Items | Description | Value | Unit |
|---|---|---|---|
| $V_{ESD\_HBM}$ | Human Body Model for all pins | ±4000 | V |
| $V_{ESD\_CDM}$ | Charged Device Model for all pins | ±1000 | V |

JEDEC specification JS-001

## Recommended Operating Conditions

| Items | Description | Min | Max | Unit |
|---|---|---|---|---|
| VIN | Supply Voltage | 2.375 | 3.5 | V |
| EN, VLDOIN, VOSNS | EN, LDO input and LDO Sense Voltage | -0.1 | 3.5 | |
| REFIN | Reference Input Voltage | 0.5 | 1.8 | |
| PGOOD, VO | Power Good and LDO Output Voltage | -0.1 | 3.5 | |
| REFOUT | Reference Output Voltage | -0.1 | 1.8 | |
| PGND | Power Ground Voltage to GND | -0.1 | 0.1 | |
| $T_J$ (Note3) | Junction Temperature | -40 | 125 | °C |

## Thermal Resistance (Note4)

| Items | Description | Value | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 65 | °C/W |
| $\theta_{JC(top)}$ | Junction-to-case(top) thermal resistance | 26 | °C/W |
| $\psi_{JT}$ | Junction-to-case(top) characterization parameter | 5.5 | °C/W |

## Electrical Characteristics

**$V_{VIN}$=3.3V, $V_{VLDOIN}$=1.8V, $V_{REFIN}$=0.9V, $V_{VOSNS}$=0.9V, $V_{EN}$= $V_{VIN}$, $C_{OUT}$ =3x10μF, $T_A$ = 25°C, and unless otherwise noted.**

| Symbol | Parameter | Conditions | Min | Type | Max | Units |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $I_{IN}$ | VIN Input Current Range | $T_A$ = 25°C, $V_{EN}$= 3.3V, No Load | | 0.7 | 1 | mA |
| $I_{IN(SDN)}$ | VIN shutdown current | $T_A$ = 25°C, $V_{EN}$= 0V, $V_{REFIN}$=0V No Load | | 30 | 80 | μA |
| | | $T_A$ = 25°C, $V_{EN}$= 0V, $V_{REFIN}$=0.9V o Load | | 200 | 400 | |
| $I_{LDOIN}$ | VLDOIN Input Current Range | $T_A$ = 25°C, $V_{EN}$= 3.3V, No Load | | 1 | 50 | |
| $I_{LDOIN(SDN)}$ | VLDOIN shutdown current | $T_A$ = 25°C, $V_{EN}$= 0V, No Load | | 2 | 50 | |
| $I_{REFIN}$ | REFIN Input Current Range | $V_{EN}$= 3.3V | | | 1 | |
| **VO OUTPUT** | | | | | | |
| VOSNS | Output DC voltage, VO | $V_{REFOUT}$ =1.25V (DDR1), $I_O$= 0A | | 1.25 | | V |
| | | | -15 | | 15 | mV |
| | | $V_{REFOUT}$ =0.9V (DDR2), $I_O$= 0A | | 0.9 | | V |
| | | | -15 | | 15 | mV |
| | | $V_{REFOUT}$ =0.75V (DDR3), $I_O$= 0A | | 0.75 | | V |
| | | | -15 | | 15 | mV |
| | | $V_{REFOUT}$ =0.675V (DDR3L), $I_O$= 0A | | 0.675 | | V |
| | | | -15 | | 15 | mV |
| | | $V_{REFOUT}$ =0.6V (DDR4), $I_O$= 0A | | 0.6 | | V |
| | | | -15 | | 15 | mV |
| $V_{VOTOL}$ | Output voltage tolerance to REFOUT | -2A<$I_{VO}$<2A | -25 | | 25 | mV |
| $I_{VOSRCL}$ | VO source current Limit | With reference to REFOUT, $V_{OSNS}$=90%x$V_{REFOUT}$ | 3 | | 5.5 | A |
| $I_{VOSNCL}$ | VO sink current Limit | With reference to REFOUT, $V_{OSNS}$=110%x$V_{REFOUT}$ | 3.5 | | 5.5 | A |
| $I_{DSCHRG}$ | Discharge current, VO | $V_{REFIN}$=0V, $V_{VO}$= 0.3V, $V_{EN}$= 0V $T_A$ = 25°C | | 20 | 30 | Ω |
| **POWERGOOD COMPAPATOR** | | | | | | |
| $V_{TH(PG)}$ | VO PGOOD threshold | PGOOD window lower threshold with respect to REFOUT | -23.5 | -20 | -17.5 | % |
| | | PGOOD window upper threshold with respect to REFOUT | 17.5 | 20 | 23.5 | |
| | | PGOOD hysteresis | | 5 | | |
| $t_{PGSTUPDLY}$ | PGOOD start-up delay | Start-up rising edge, VOSNS within 15% of REFOUT | | 2 | | ms |
| $V_{PGOODLOW}$ | Output low voltage | $I_{SINK}$ = 4 mA | | | 0.4 | V |
| $t_{PBADDLY}$ | PGOOD bad delay | VOSNS is outside of the ±20% PGOOD window | | 20 | | μs |
| $I_{PGOODLK}$ | Leakage current | $V_{OSNS}$ = $V_{REFIN}$ (PGOOD high impedance), $V_{PGOOD}$ = $V_{VIN}$ + 0.2V | | | 1 | μA |

## Electrical Characteristics (Continued)

**$V_{VIN}$ = 3.3V, $V_{VLDOIN}$ = 1.8V, $V_{REFIN}$ = 0.9V, $V_{VOSNS}$ = 0.9V, $V_{EN}$ = $V_{VIN}$, $C_{OUT}$ = 3*10μF, $T_A$ = 25°C, and unless otherwise noted.**

| Symbol | Parameter | Conditions | Min | Type | Max | Units |
|---|---|---|---|---|---|---|
| **REFIN AND REFOUT** | | | | | | |
| $V_{REFIN}$ | REFIN voltage range | | 0.5 | | 1.8 | V |
| $V_{REFINUVLO}$ | REFIN under voltage lockout | REFIN rising | 340 | 390 | 440 | mV |
| $V_{REFINUVHYS}$ | REFIN under voltage lockout hysteresis | | | 60 | | mV |
| $V_{REFOUT}$ | REFOUT voltage | | | REFIN | | V |
| $V_{REFOUTTOL}$ | REFOUT voltage tolerance to $V_{REFIN}$ | − 1mA < $I_{REFOUT}$ < 1mA<br>$V_{REFIN}$ = 1.25 V | -12 | | 12 | mV |
| | | − 1mA < $I_{REFOUT}$ < 1mA<br>$V_{REFIN}$ = 0.9 V | -12 | | 12 | |
| | | − 1mA < $I_{REFOUT}$ < 1mA<br>$V_{REFIN}$ = 0.75 V | -12 | | 12 | |
| | | − 1mA < $I_{REFOUT}$ < 1mA<br>$V_{REFIN}$ = 0.675V | -12 | | 12 | |
| | | − 1mA < $I_{REFOUT}$ < 1mA<br>$V_{REFIN}$ = 0.6 V | -12 | | 12 | |
| $I_{REFOUTSRCL}$ | REFOUT source current limit | $V_{REFOUT}$ = 0 V | 25 | 50 | | mA |
| $I_{REFOUTSNCL}$ | REFOUT sink current limit | $V_{REFOUT}$ = 0 V | 25 | 50 | | mA |
| **VIN UVLO AND EN LOGIC THRESHOLD** | | | | | | |
| $U_{VINUV}$ | UVLO threshold of VIN | VIN rising, $T_A$ = 25°C | | 2.3 | 2.375 | V |
| | | Hysteresis | | 150 | | mV |
| $V_{ENIH}$ | High-level threshold voltage | VIN=3.3V | | 1.35 | 1.7 | V |
| $V_{ENIL}$ | Low-level threshold voltage | VIN=3.3V | 0.5 | 1.05 | | |
| $V_{ENYST}$ | Hysteresis voltage | VIN=3.3V | | 0.3 | | |
| $I_{ENLEAK}$ | Logic input leakage current | EN, $T_A$ = 25°C | -1 | | 1 | μA |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SON}$ | Thermal shutdown threshold | Shutdown temperature | | 155 | | °C |
| | | Hysteresis | | 25 | | |

**Note 1**: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2**: Devices are ESD sensitive. Handling precaution is recommended.

**Note 3**: $T_J$ is calculated from the ambient temperature $T_A$ and power dissipation $P_D$ according to the following formula: $T_J = T_A + P_D \times \theta_{JA}$.

**Note 4**: Measured on JESD51-7, 4-layer PCB.

## Block Diagram

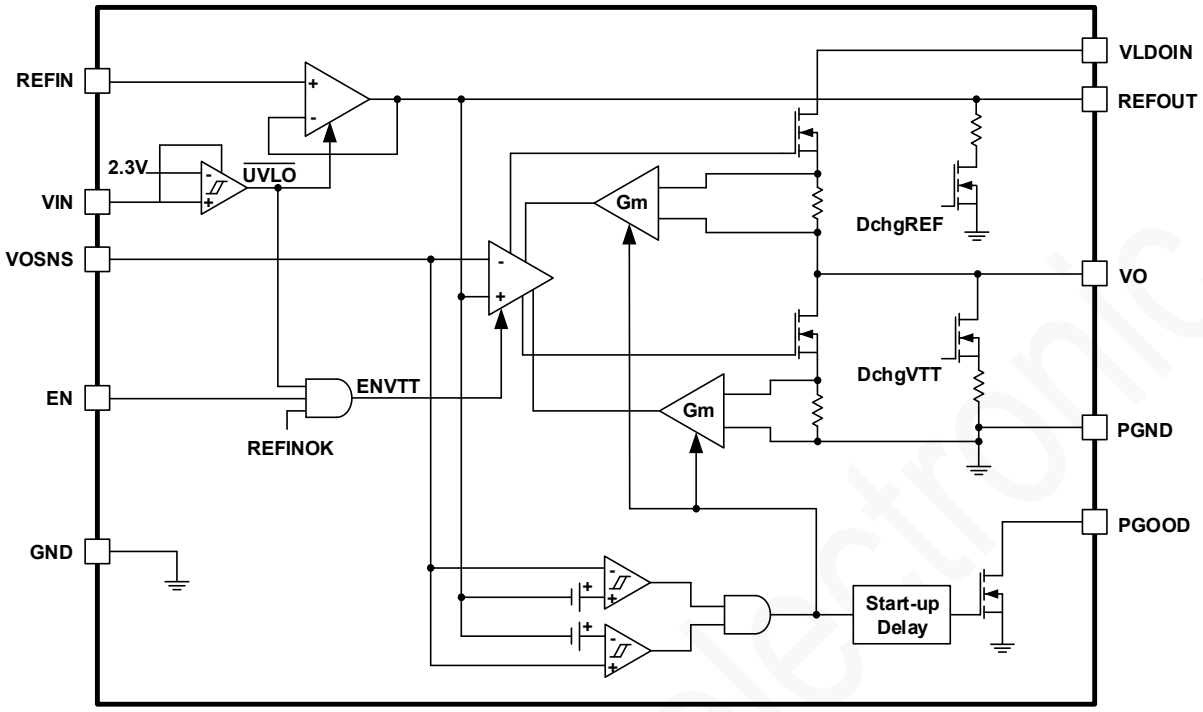
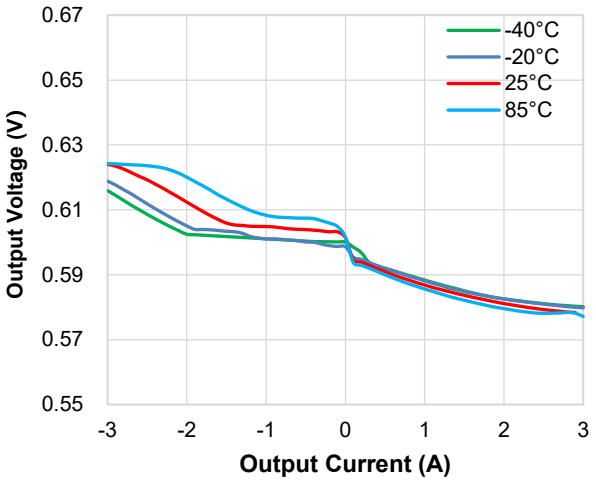



**Figure 2. TMI62033 Block Diagram**

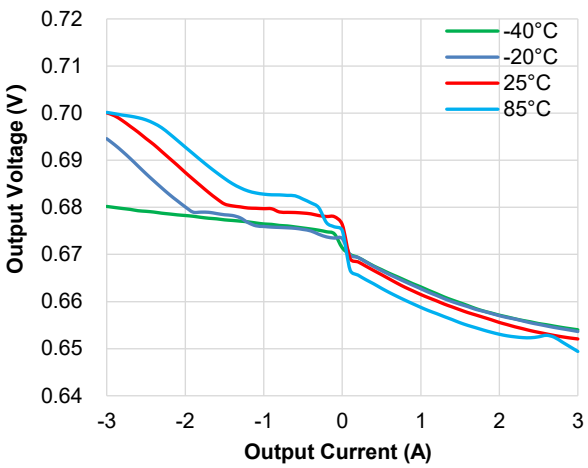
## TYPICAL CHARACTERISTICS

**$V_{IN}$ = 3.3V, $V_{EN}$ = $V_{VIN}$, $C_{OUT}$ = 3x10μF, $T_A$ = 25°C, and unless otherwise noted.**

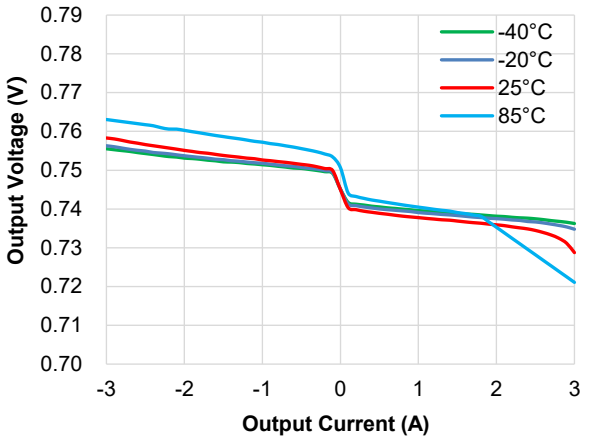
Load Regulation VIN=3.3V DDR4



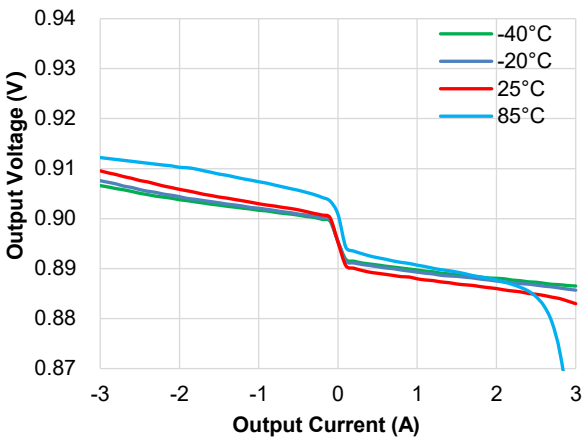

Load Regulation VIN=3.3V DDR3L



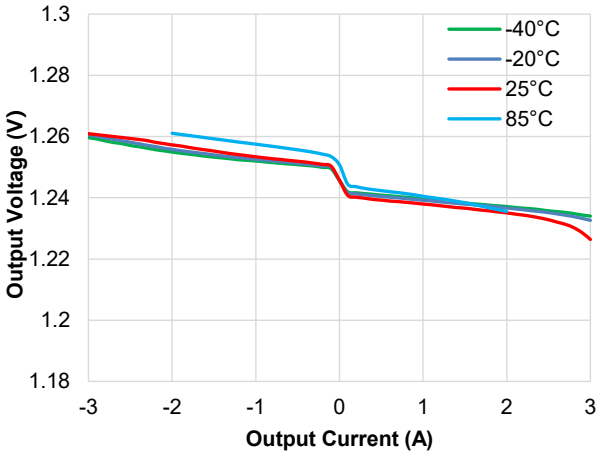

Load Regulation VIN=3.3V DDR3



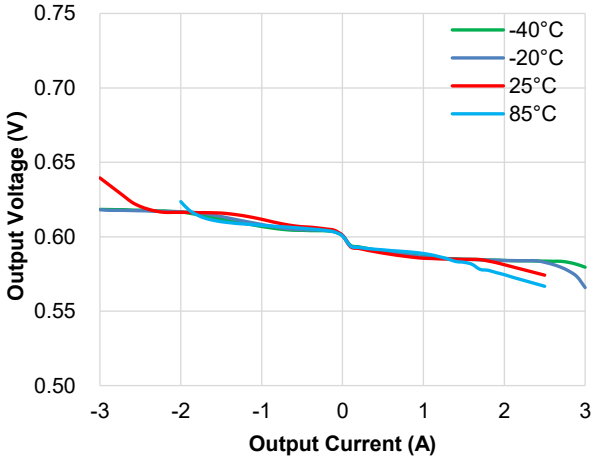

Load Regulation VIN=3.3V DDR2




Load Regulation VIN=3.3V DDR



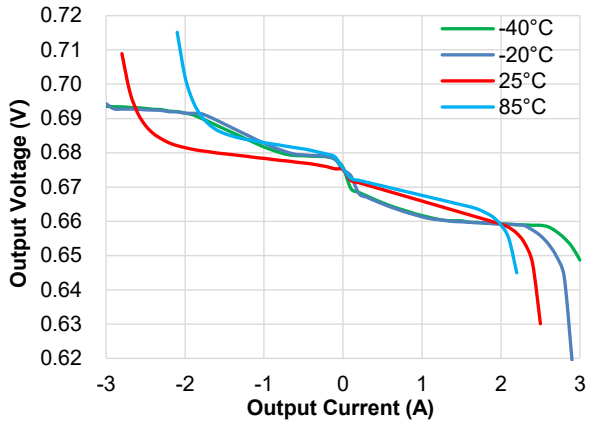

Load Regulation VIN=2.5V DDR4



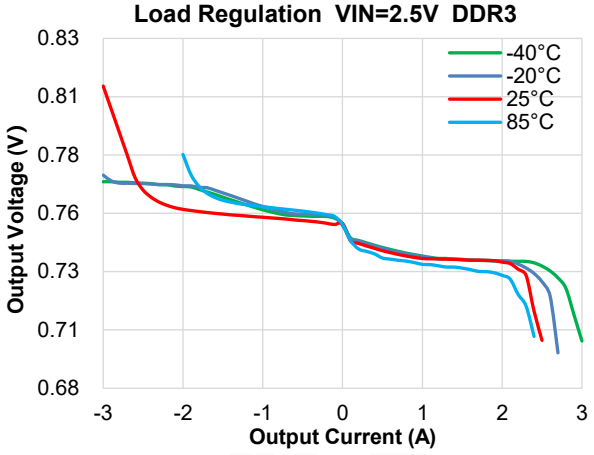
## TYPICAL CHARACTERISTICS (continued)

**$V_{IN}$ = 3.3V, $V_{EN}$ = $V_{VIN}$, $C_{OUT}$ = 3x10μF, $T_A$ = 25°C, and unless otherwise noted.**

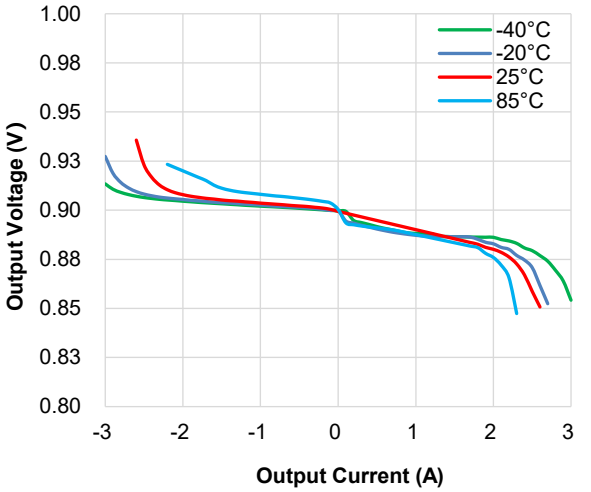
Load Regulation VIN=2.5V DDR3L



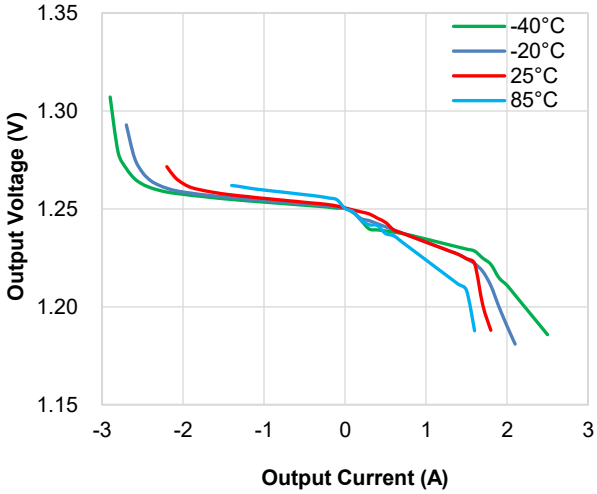

Load Regulation VIN=2.5V DDR3



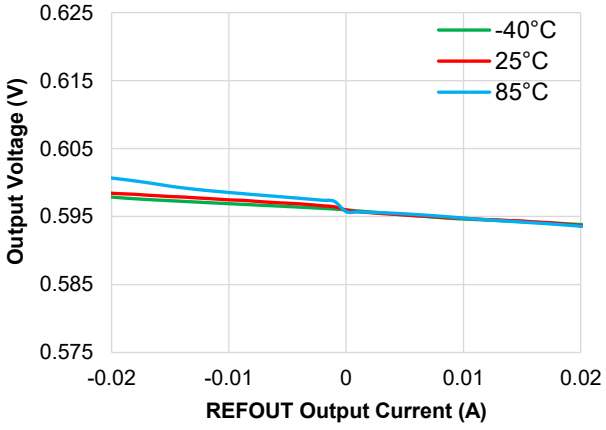

Load Regulation VIN=2.5V DDR2



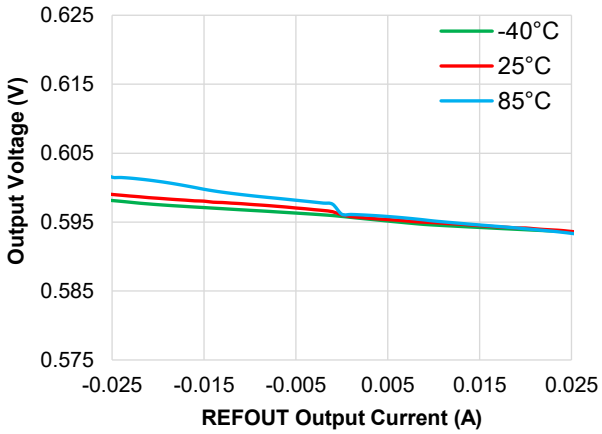

Load Regulation VIN=2.5V DDR




REFOUT Load Regulation VIN=2.5V DDR4



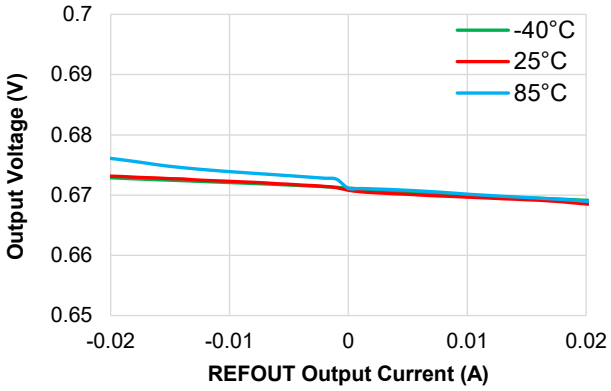

REFOUT Load Regulation VIN=3.3V DDR4



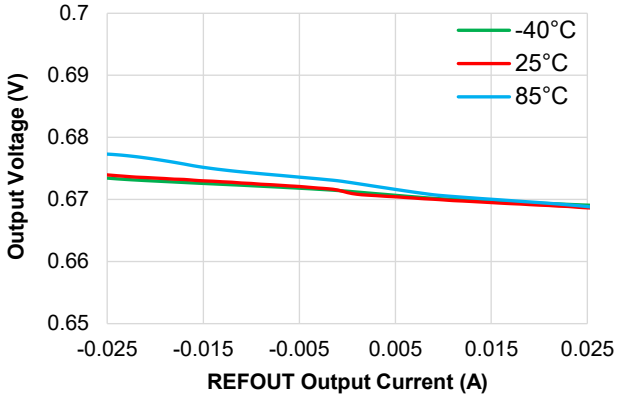
## TYPICAL CHARACTERISTICS (continued)

**$V_{IN}$ = 3.3V, $V_{EN}$ = $V_{VIN}$, $C_{OUT}$ = 3x10μF, $T_A$ = 25°C, and unless otherwise noted.**

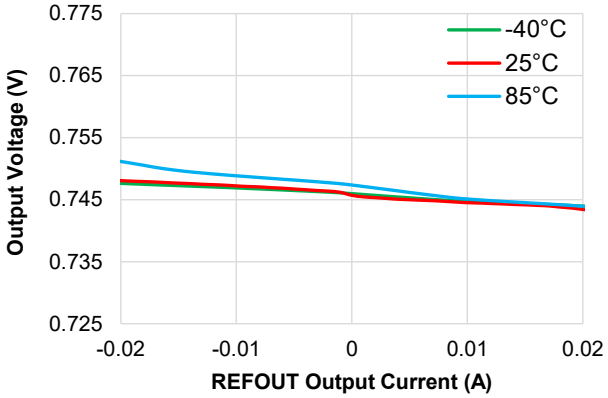
REFOUT Load Regulation VIN=2.5 VDDRL3



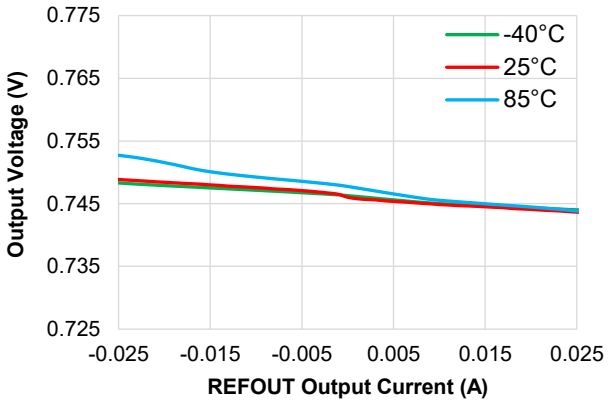

REFOUT Load Regulation VIN=3.3 VDDRL3



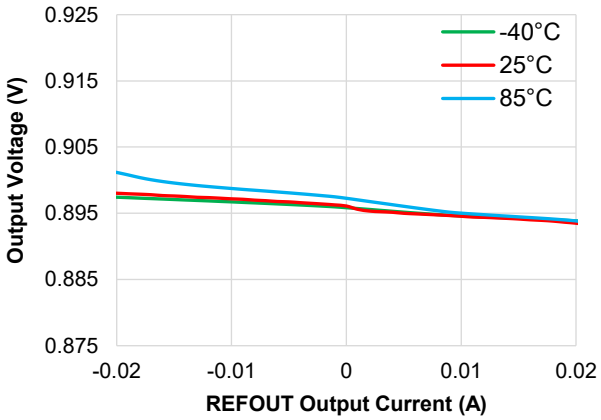

REFOUT Load Regulation VIN=2.5V DDR3



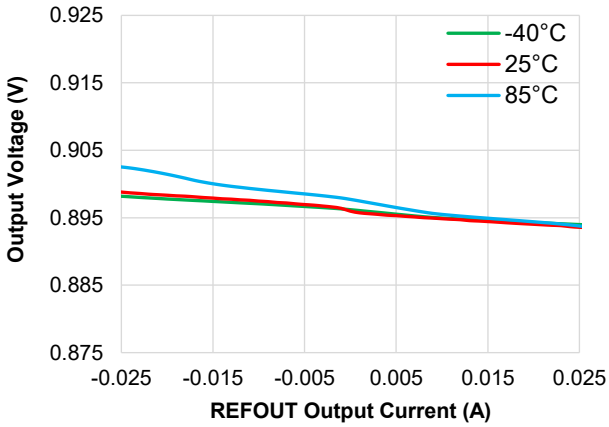

REFOUT Load Regulation VIN=3.3V DDR3




REFOUT Load Regulation VIN=2.5V DDR2



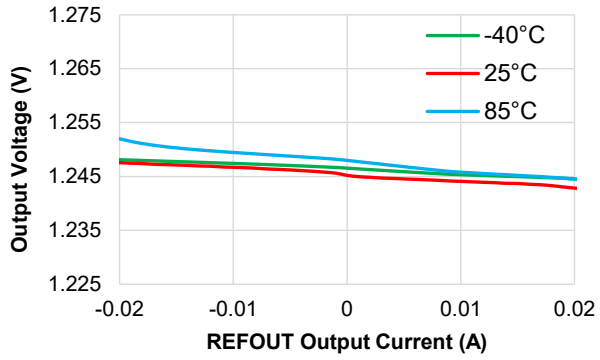

REFOUT Load Regulation VIN=3.3V DDR2



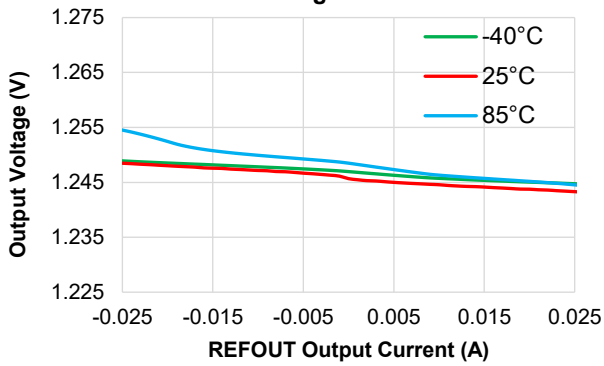
## TYPICAL CHARACTERISTICS (continued)

**$V_{IN}$ = 3.3V, $V_{EN}$ = $V_{VIN}$, $C_{OUT}$ = 3x10μF, $T_A$ = 25°C, and unless otherwise noted.**

REFOUT Load Regulation VIN=2.5V DDR

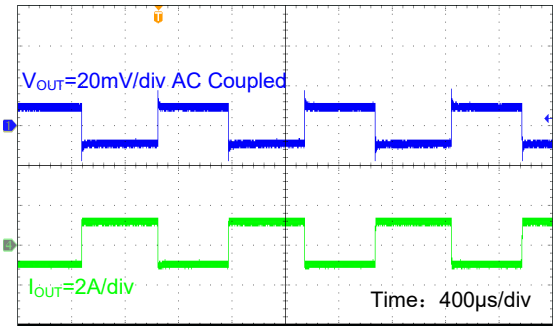



REFOUT Load Regulation VIN=3.3V DDR



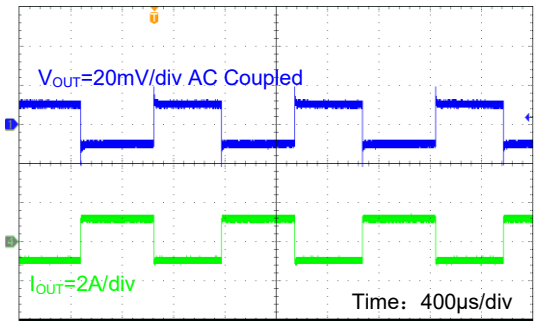

Load Transient

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.35V, $V_{VLDOIN}$=1.35V



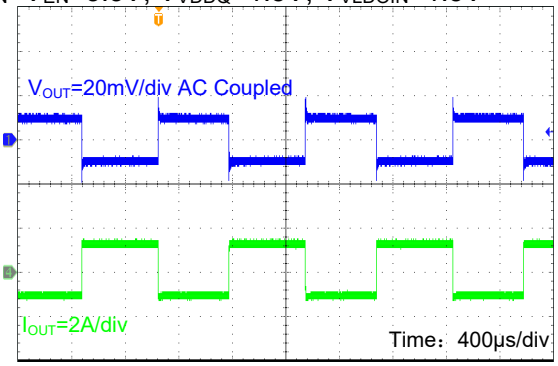

Load Transient

$V_{IN}$=$V_{EN}$=2.5V, $V_{VDDQ}$=1.35V, $V_{VLDOIN}$=1.35V,



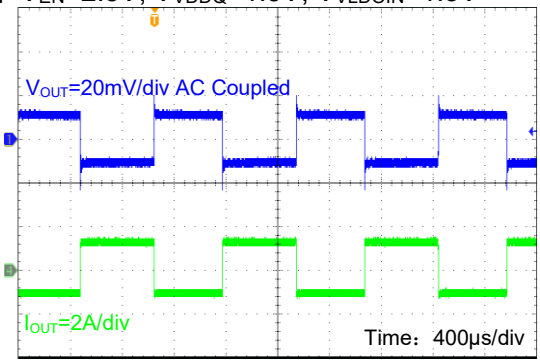

Load Transient

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.5V, $V_{VLDOIN}$=1.5V



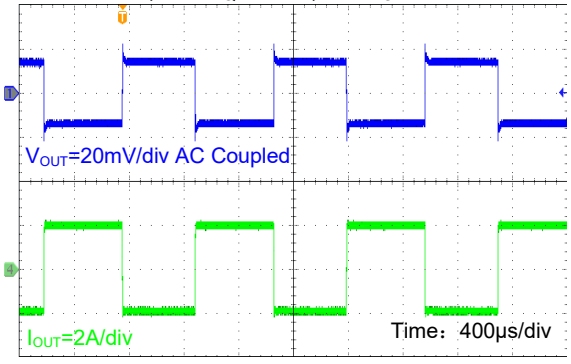

Load Transient

$V_{IN}$=$V_{EN}$=2.5V, $V_{VDDQ}$=1.5V, $V_{VLDOIN}$=1.5V



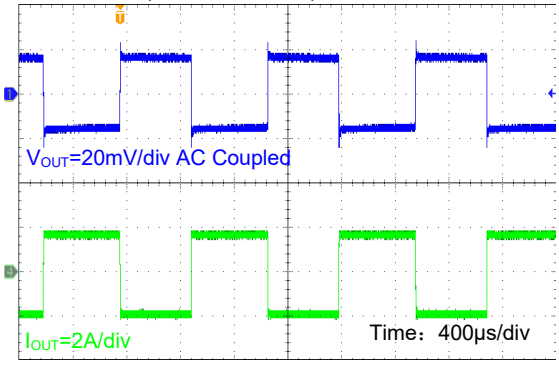

Load Transient

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.8V, $V_{VLDOIN}$=1.8V




Load Transient

$V_{IN}$=$V_{EN}$=2.5V, $V_{VDDQ}$=1.8V, $V_{VLDOIN}$=1.8V

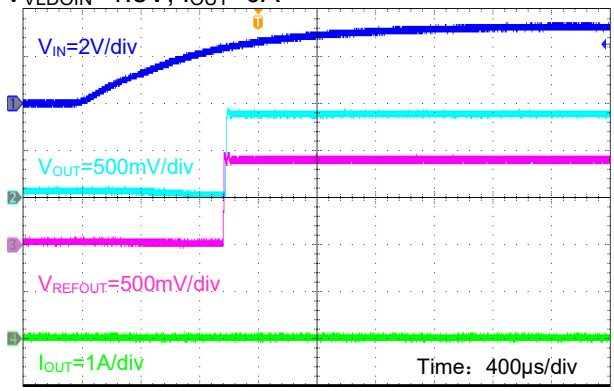


## TYPICAL CHARACTERISTICS (continued)

**$V_{VIN}$ = 3.3V, $V_{VLDOIN}$ = 1.8V, $V_{REFIN}$ = 0.9V, $V_{VOSNS}$ = 0.9V, $V_{EN}$ = $V_{VIN}$, $C_{OUT}$ = 3x10μF, $T_A$ = 25°C**

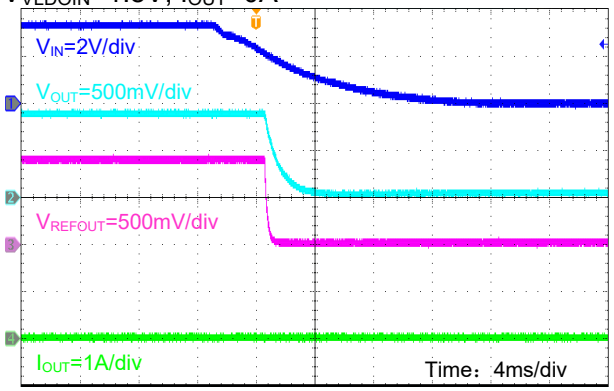
**Input Power On**

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.8V
$V_{VLDOIN}$=1.8V, $I_{OUT}$=0A



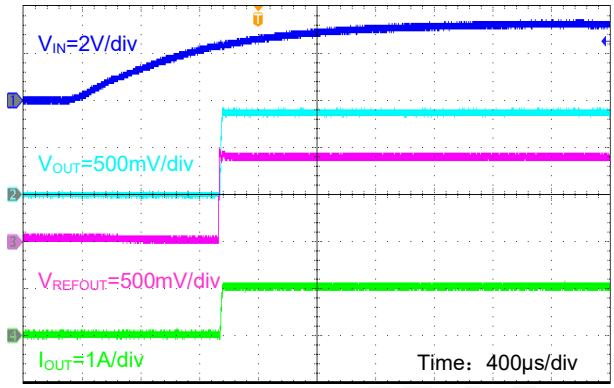

**Input Power Down**

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.8V
$V_{VLDOIN}$=1.8V, $I_{OUT}$=0A



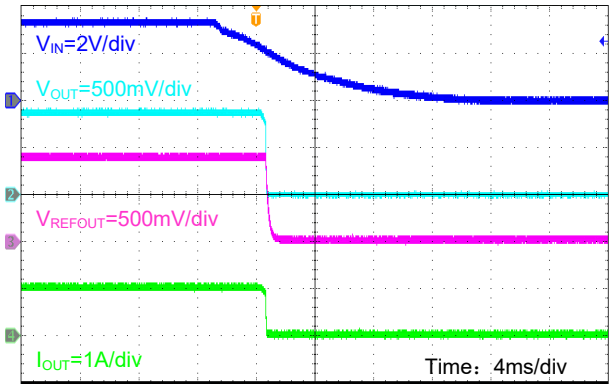

**Input Power On**

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.8V
$V_{VLDOIN}$=1.8V, $I_{OUT}$=1A



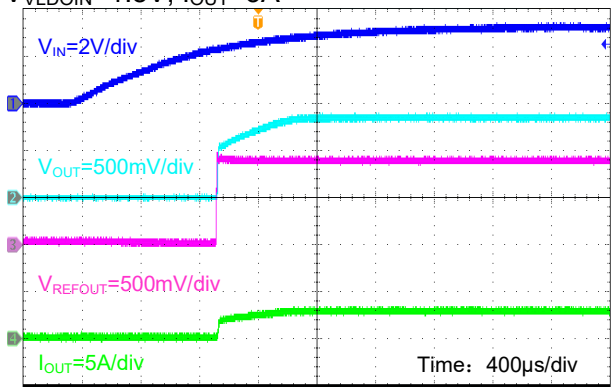

**Input Power Down**

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.8V
$V_{VLDOIN}$=1.8V, $I_{OUT}$=1A



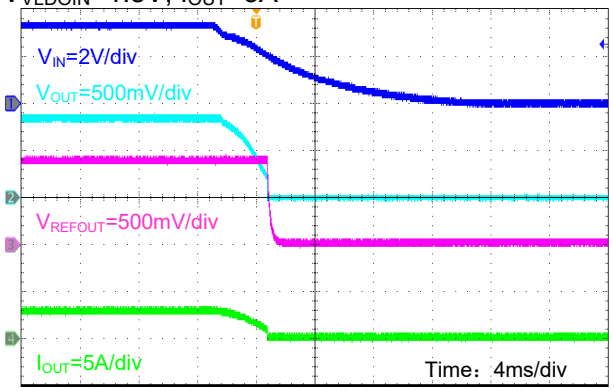

**Input Power On**

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.8V
$V_{VLDOIN}$=1.8V, $I_{OUT}$=3A




**Input Power Down**

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.8V
$V_{VLDOIN}$=1.8V, $I_{OUT}$=3A

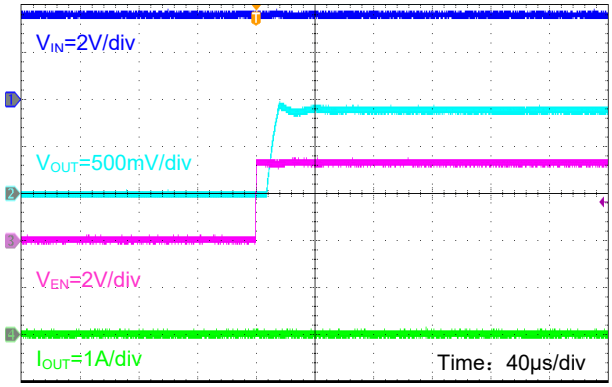


## TYPICAL CHARACTERISTICS (continued)

**$V_{VIN}$ = 3.3V, $V_{VLDOIN}$ = 1.8V, $V_{REFIN}$ = 0.9V, $V_{VOSNS}$ = 0.9V, $V_{EN}$ = $V_{VIN}$, $C_{OUT}$ = 3x10μF, $T_A$ = 25°C**

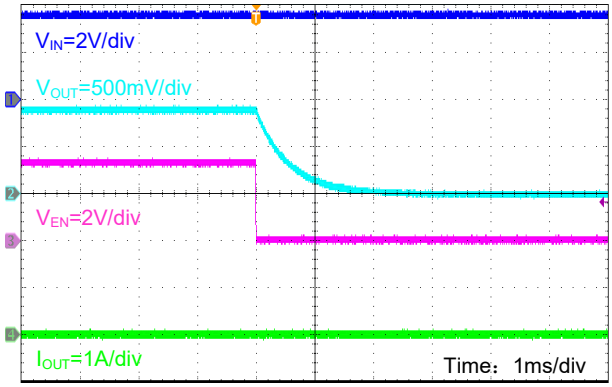
**EN Enable Power On**

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.8V
$V_{VLDOIN}$=1.8V, $I_{OUT}$=0A



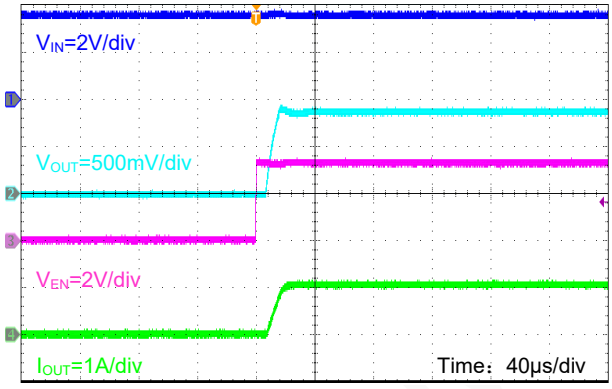

**EN Enable Power Down**

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.8V
$V_{VLDOIN}$=1.8V, $I_{OUT}$=0A



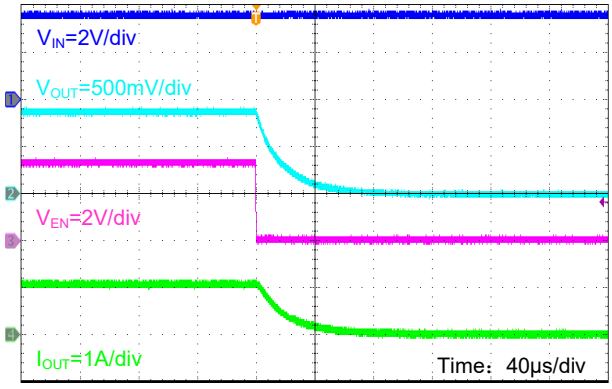

**EN Enable Power On**

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.8V
$V_{VLDOIN}$=1.8V, $I_{OUT}$=1A



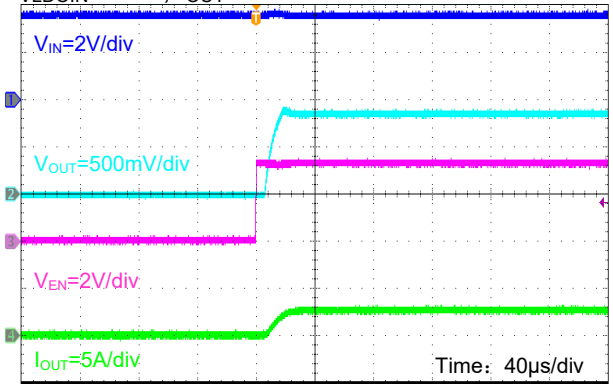

**EN Enable Power Down**

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.8V
$V_{VLDOIN}$=1.8V, $I_{OUT}$=1A



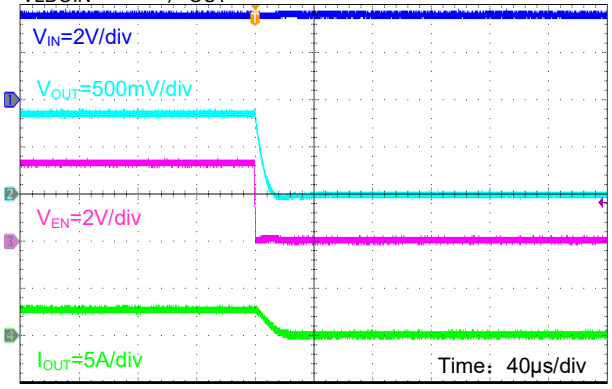

**EN Enable Power On**

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.8V
$V_{VLDOIN}$=1.8V, $I_{OUT}$=3A




**EN Enable Power Down**

$V_{IN}$=$V_{EN}$=3.3V, $V_{VDDQ}$=1.8V
$V_{VLDOIN}$=1.8V, $I_{OUT}$=3A



# Operation Description

## Overview

The TMI62033 is a 3A sink and source double data rate (DDR) termination regulator. it supports a remote sensing function and all power requirements for DDR, DDR2, DDR3, DDR3L, Low-Power DDR3 and DDR4 VTT bus termination.
The device maintains a fast transient response and requires a minimum output capacitance of only 20μF for low-cost, low-noise systems where space is a key consideration.

## VO Pin (Sink and Source)

The TMI62033 is a 3A sink and source tracking DDR termination regulator specifically designed. The device integrates a high-performance, low-dropout (LDO) linear regulator that is capable of both sourcing and sinking current. The LDO regulator employs a fast feedback loop so that small ceramic capacitors can be used to support the fast load transient response. To get tight regulation with minimum effect of trace resistance, connect a remote sensing terminal, VOSNS, to the positive terminal of each output capacitor as a separate trace from the high current path from VO.

## REFIN Pin

The output voltage, VO is regulated to REFOUT. When REFIN is configured for standard DDR termination applications, REFIN can be set by an external equivalent ratio voltage divider connected to the memory supply bus (VDDQ). The TMI62033 device supports REFIN voltages from 0.5V to 1.8V, for many types of low-power LDO applications.

## REFOUT Pin

When it is configured for DDR termination applications, REFOUT generates the DDR VTT reference voltage for the memory application. It is capable of supporting both a sourcing and sinking load of 25mA. When the REFIN voltage is higher than rising UVLO threshold of REFIN and IN voltage is ready, there is voltage regulated at the REFOUT pin, which the REFOUT pin is independent with EN status.

## EN Pin

When EN is driven high, the VO regulator begins normal operation. When the device drives EN low, VO discharges to GND through an internal MOSFET. REFOUT remains on when the device drives EN low. Ensure that the EN pin voltage remains lower than or equal to VIN at all times.

## Soft-Start

A current clamp implements the soft-start function of the VO pin. The current clamp allows the output capacitors to be charged with low and constant current, providing a linear ramp-up of the output voltage. When VO is outside of the power good window, the current clamp level is one-half of the full overcurrent limit (OCL) level. When VO rises or falls within the PGOOD window, the current clamp level switches to the full OCL level. The soft-start function is completely symmetrical and the

overcurrent limit works for both directions. The soft-start function works not only from GND to the REFOUT voltage, but also from VLDOIN to the REFOUT voltage.

### PGOOD Pin

The TMI62033 device provides an open-drain PGOOD output that goes high when the VO output is within ±20% of REFOUT. When output voltage enters the power-good window, the PG pin turns to high output impedance, and PG is pulled up to high-voltage level after 2ms delay to indicate the output voltage is ready.

A pull-up resistor is recommended with a value between 1kΩ and 100kΩ, placed between PGOOD and a stable active supply voltage rail is required.

### UVLO Protection of VIN

The TMI62033 monitors VIN voltage. When the VIN voltage is lower than the UVLO threshold voltage, both the VO and REFOUT regulators are powered off. This shutdown is a non-latch protection.

### Over Current Limit (OCL)

The LDO has a constant overcurrent limit (OCL). The OCL level reduces by one-half when the output voltage is not within the power good window. This reduction is a non-latch protection.

### Thermal Shutdown

The TMI62033 monitors junction temperature. If the device junction temperature exceeds the threshold value, (typically 155°C), the VO and REFOUT regulators both shut off, discharged by the internal discharge MOSFETs. This shutdown is a non-latch protection.

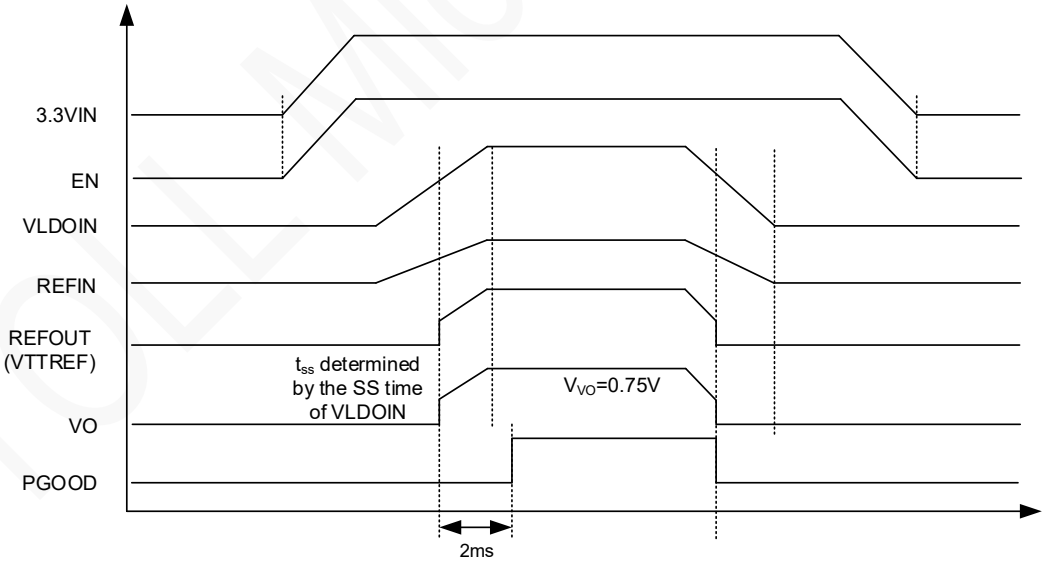



**Figure 3. Typical Timing Diagram of Tracking Start-up and Shutdown**

### Tracking Start-up and Shutdown

The TMI62033 also supports tracking start-up and shutdown when the EN pin is tied directly to the system bus and not used to turn on or turn off the device. During tracking start-up, VO follows REFOUT once REFIN voltage is greater than 0.39V. REFIN follows the rise of VDDQ rail through a voltage divider. The typical soft-start time ($t_{SS}$) for the VDDQ rail is approximately 3ms, however it may vary depending on the system configuration. The soft-start time of the VO output no longer depends on the OCL setting, but it is a function of the soft-start time of the VDDQ rail. PGOOD is asserted 2ms after $V_{VO}$ is within ±20% of REFOUT. During tracking shutdown, the VO pin voltage falls following REFOUT until REFOUT reaches 0.33 V. When REFOUT falls below 0.33 V, the internal discharge MOSFETs turn on and quickly discharge both REFOUT and VO to GND. PGOOD is deasserted when VO is beyond the ±20% range of REFOUT. Figure 3 shows the typical timing diagram for an application that uses tracking start-up and shutdown.

## Layout

### Layout Guidelines

Consider the following points before starting the TMI62033 device layout design.

- Place the input capacitors as close to VDLOIN pin as possible with short and wide connection. Place the output capacitor as close to VO pin as possible with short and wide connection. Place a ceramic capacitor with a value of at least 20μF as close to VO pin if the rest of output capacitors need to be placed on the load side.
- Connect the VOSNS pin to the positive node of output capacitors as a separate trace. In DDR VTT application, connect the VO sense trace to DIMM side to ensure the VTT voltage at DIMM side is well regulated.
- Consider adding low-pass filter at VOSNS if the VO sense trace is very long. Connect the GND pin and PGND pin to the thermal pad directly.
- TMI62033 uses its thermal pad to dissipate heat. In order to effectively remove heat from TMI62033 package, place numerous ground vias on the thermal pad. Use large ground copper plane, especially the copper plane on surface layer, to pour over those vias on thermal pad.

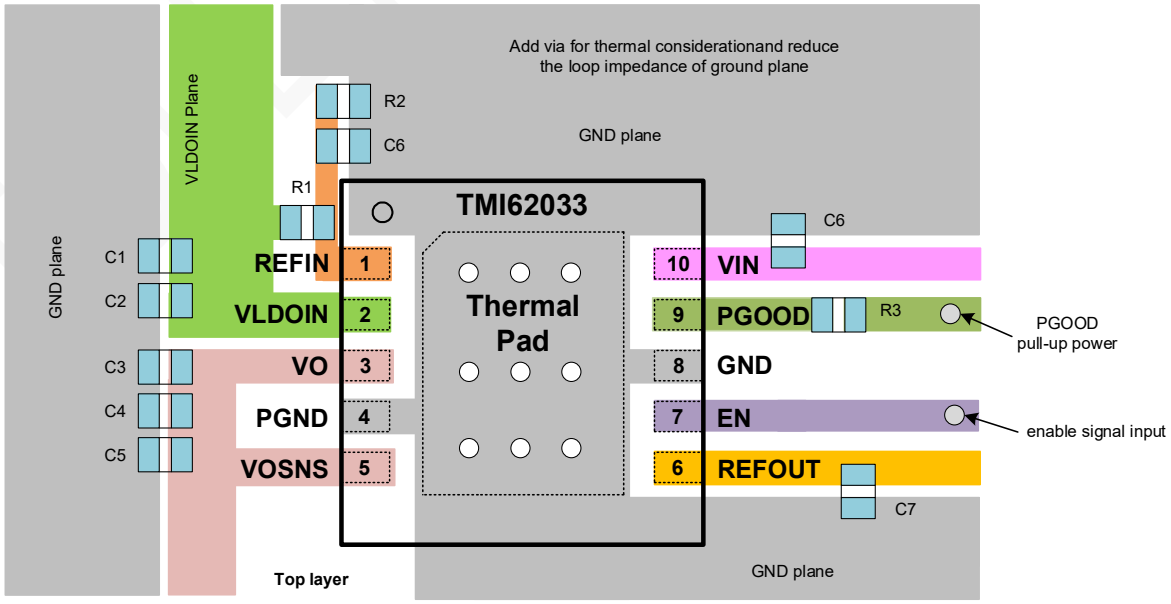
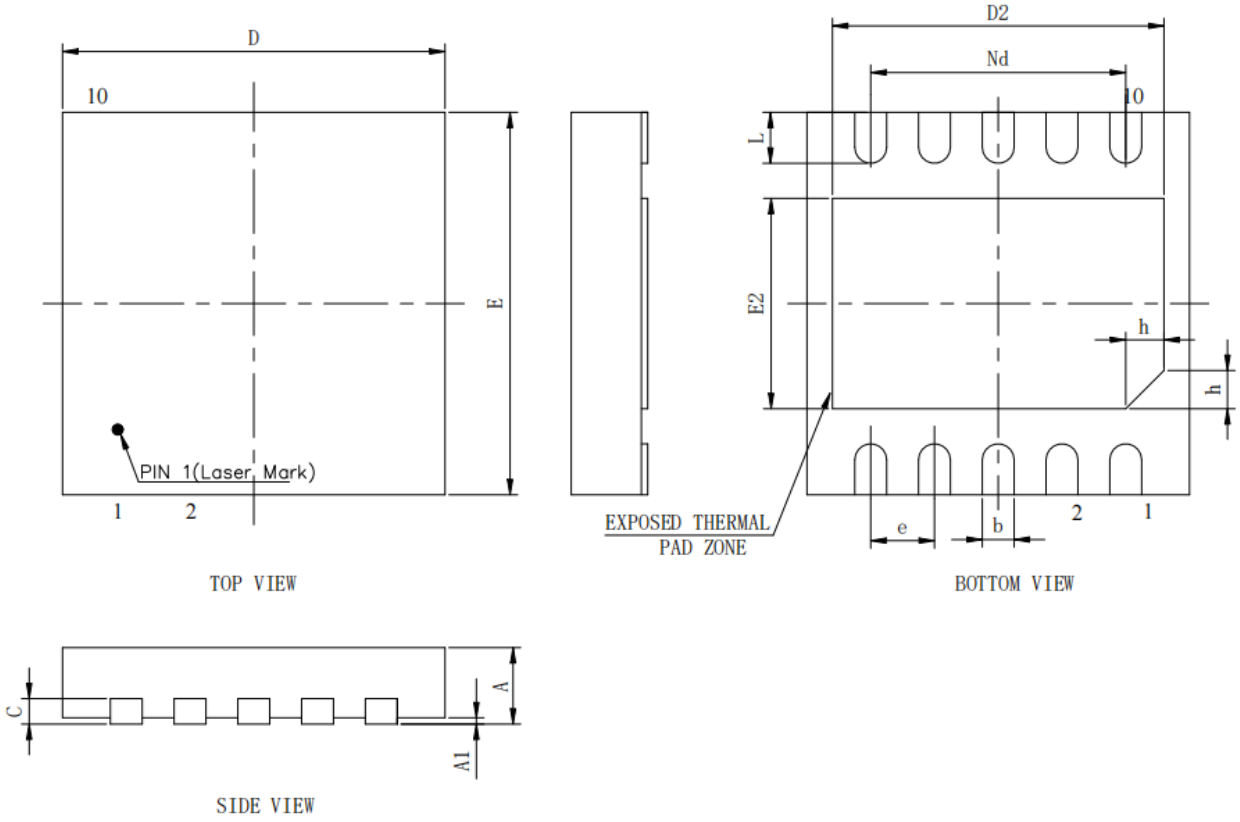



**Figure 4. Layout Recommendation**

## Package Information

### DFN3x3-10




Unit: mm

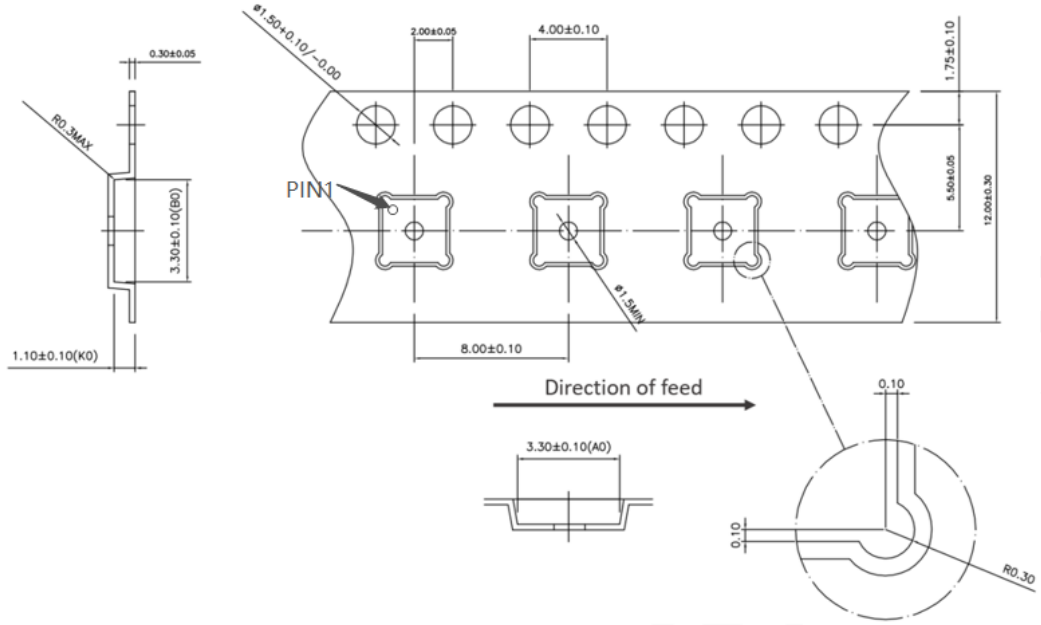
| Symbol | Dimensions In Millimeters | | | Symbol | Dimensions In Millimeters | | |
|---|---|---|---|---|---|---|---|
| | Min | Nom | Max | | Min | Nom | Max |
| A | 0.85 | 0.90 | 0.95 | L | 0.30 | 0.40 | 0.50 |
| A1 | 0 | 0.02 | 0.05 | h | 0.20 | 0.25 | 0.30 |
| b | 0.20 | 0.25 | 0.30 | e | 0.50BSC | | |
| D | 2.90 | 3.00 | 3.10 | Nd | 2.00BSC | | |
| E | 2.90 | 3.00 | 3.10 | c | 0.20REF | | |
| D2 | 2.40 | 2.50 | 2.60 | | | | |
| E2 | 1.45 | 1.55 | 1.65 | | | | |

**Note:**

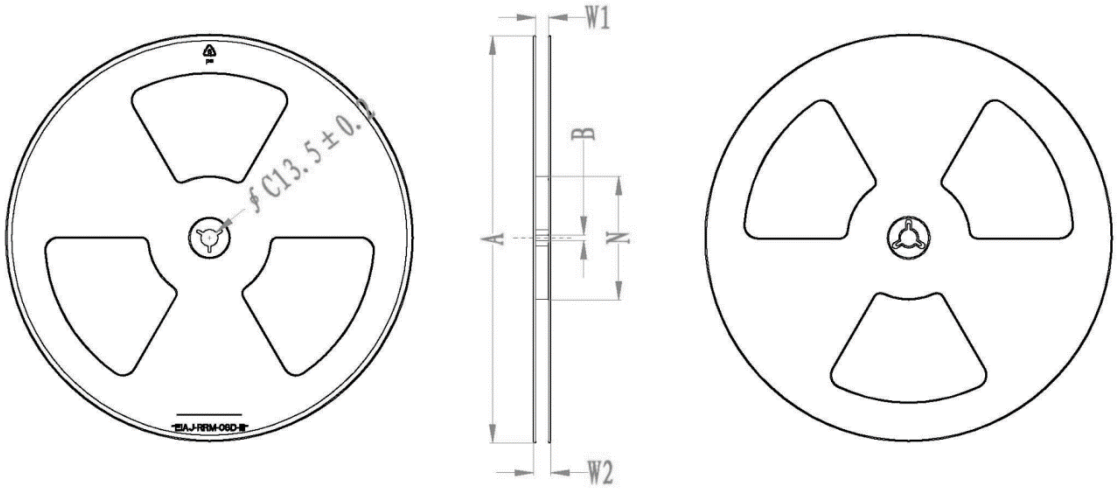
All dimensions are in millimeters.

# TAPE AND REEL INFORMATION

## TAPE DIMENSIONS:




## REEL DIMENSIONS:




Unit: mm

| Ø A | Ø C | B | W1 | W2 | N |
|---|---|---|---|---|---|
| 330±1.0 | 13.5±0.2 | 4.7±0.5 | 13.4±0.5 | 17.4±0.5 | 100±0.5 |

**Note:**

All Dimensions are in Millimeter

Quantity of Units per Reel is 5000

MSL level is level 3.

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