

# Low Quiescent Current, Programmable Delay Time, Supervisory Circuit

## NCP308, NCV308

The NCP308 series is one of the ON Semiconductor Supervisory circuit IC families. It is optimized to monitor system voltages from 0.405 V to 5.5 V, asserting an active low open-drain  $\overline{\text{RESET}}$  output, together with Manual Reset ( $\overline{\text{MR}}$ ) Input. The part comes with both fixed and externally adjustable versions.

### Features

- Wide Supply Voltage Range 1.6 to 5.5 V
- Very Low Quiescent Current 1.6  $\mu\text{A}$
- Fixed Threshold Voltage Versions for Standard Voltage Rails Including 0.9 V, 1.2 V, 1.25 V, 1.5 V, 1.8 V, 1.9 V, 2.5 V, 2.8 V, 3.0 V, 3.3 V, 5.0 V
- Adjustable Version with Low Threshold Voltage 0.405 V (min)
- High Threshold Voltage Accuracy: 0.31% typ
- Support Manual Reset Input ( $\overline{\text{MR}}$ )
- Open-Drain  $\overline{\text{RESET}}$  Output (Push-pull Output upon Request)
- Flexible Delay Time Programmability: 1.25 ms to 10 s
- Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Small TSOP-6 and WDFN6 2 x 2 mm, Pb-Free packages
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These are Pb-Free Devices

### Typical Applications

- DSP or Microcontroller Applications
- Notebook/Desktop Computers
- PDAs/Hand-Held Products
- Portable/Battery-Powered Products
- FPGA/ASIC Applications

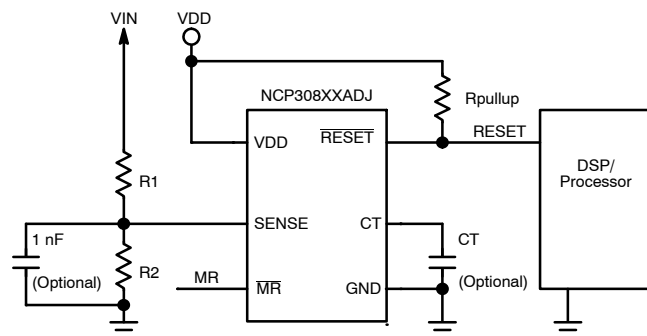


Figure 1. Typical Application Circuit for Adjustable Versions

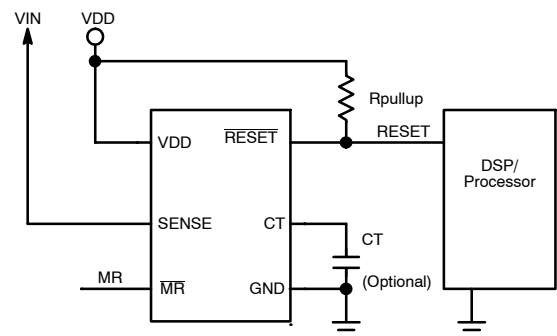
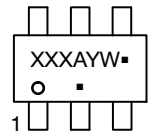


Figure 2. Typical Application Circuit for Fixed Versions

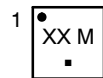
### MARKING DIAGRAMS



TSOP-6  
CASE 318G



WDFN6  
CASE 511BR



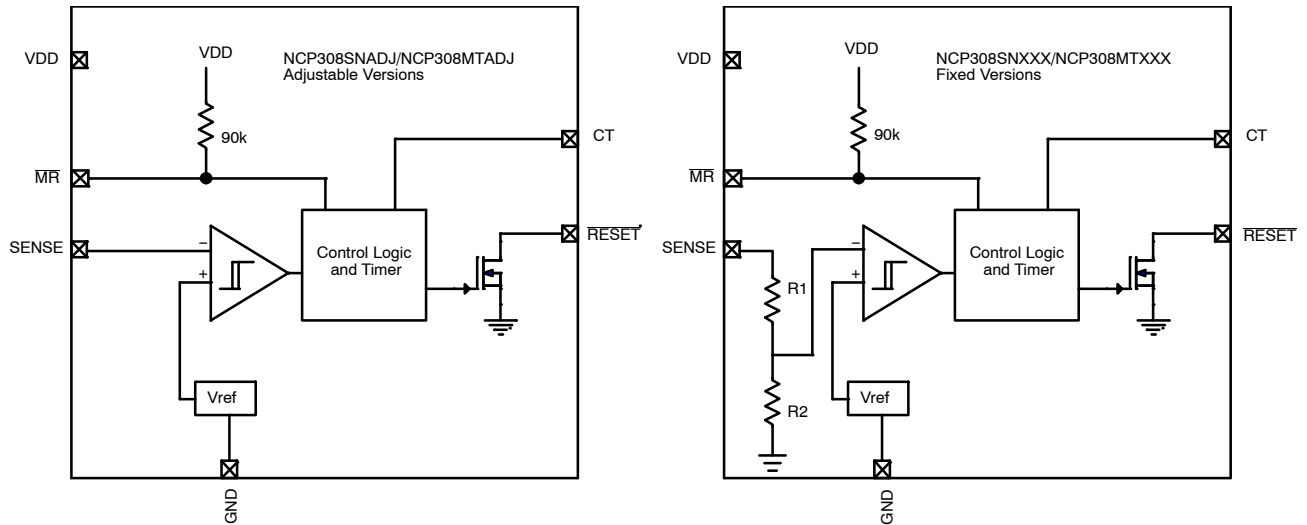
XXX, XX= Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
M = Date Code  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

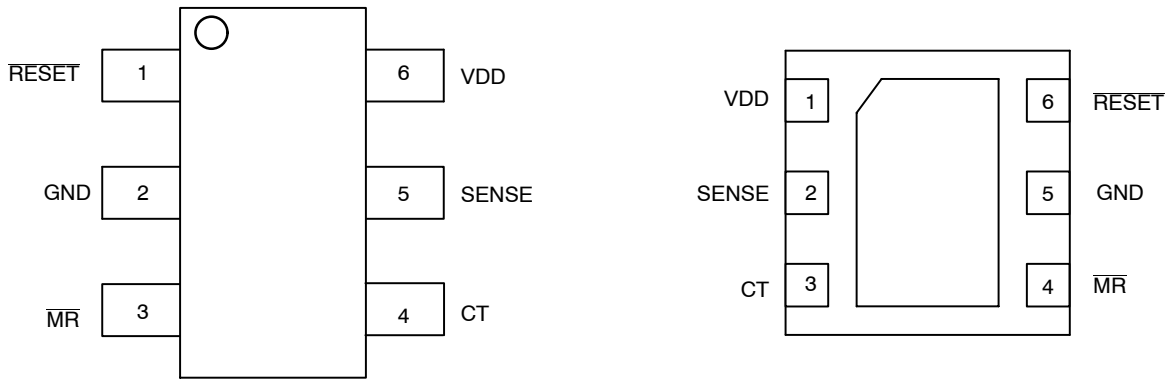
### ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 9 of this data sheet.

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**Figure 3. Functional Block Diagrams of Adjustable and Fixed Versions**



**Figure 4. Pin Connections Diagram (Top View)**

**Table 1. PIN OUT DESCRIPTION**

Name	Pin Number		Description
	TSOP-6	WDFN6	
VDD	6	1	<b>Supply Voltage.</b> A 0.1uF ceramic capacitor placed close to this pin is helpful for transient and parasitic.
SENSE	5	2	<b>Sense Input,</b> this is the voltage to be monitored. If the voltage at this terminal drops below the threshold voltage $V_{IT}$ , then RESET is asserted. SENSE does not necessary monitor VDD, it can monitor any voltage lower than VDD.
CT	4	3	<b>Reset Delay Time Setting Pin.</b> Connecting this pin to VDD through a 40 kΩ to 200 kΩ resistor or leaving it open results in fixed reset delay times. Connecting this pin to a ground referenced capacitor ( $\geq 100$ pF) gives a user-programmable reset delay time. See the <i>Setting Reset Delay Time</i> section for more information.
MR	3	4	<b>Manual Reset input,</b> MR low asserts RESET. MR is internally tied to VDD by a 90 kΩ pull-up Resistor.
RESET	1	6	<b>RESET Output,</b> is an Active low open drain N-Channel MOSFET output, it is driven to a low impedance state when RESET is asserted (either the SENSE input is lower than the threshold voltage ( $V_{IT}$ ) or the MR pin is set to a logic low). RESET will keep low (asserted) for the reset delay time after both SENSE is above $V_{IT}$ and MR is set to a logic high. A pull-up resistor from 10kΩ to 1MΩ should be used on this pin. See Figure 5 for behavior of RESET depends on VDD, SENSE and MR conditions.
GND	2	5	<b>Ground terminal.</b> Should be connected to PCB ground reference
EXP PAD	–	Exposed Pad	<b>Exposed pad,</b> under WDFN6 package, connect it to ground plane for better thermal dissipation.

# NCP308, NCV308

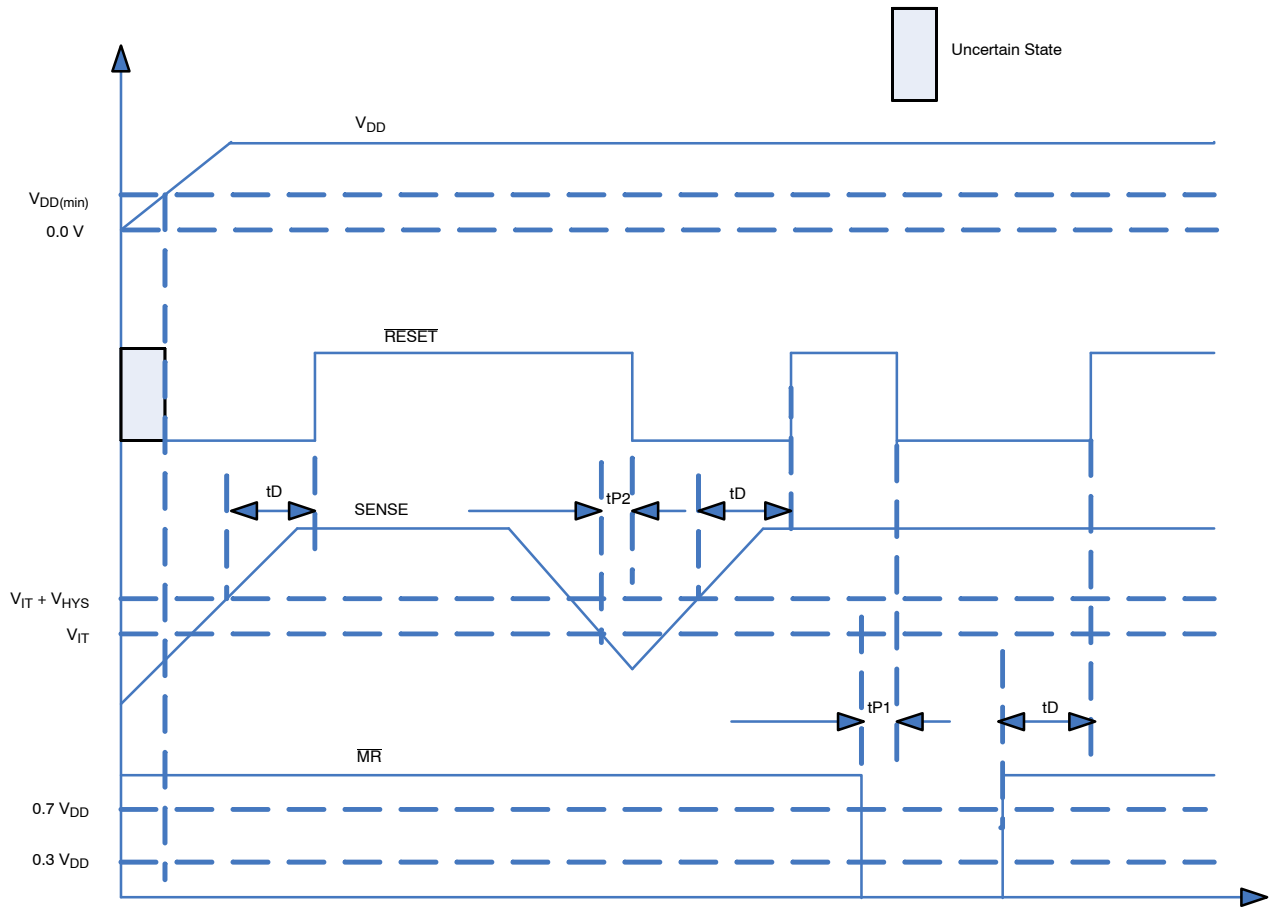


Figure 5. Timing Diagram Showing  $\overline{MR}$  and SENSE Reset Timing

Table 2. TRUTH TABLE

$\overline{MR}$	$SENSE > V_{IT}$	$\overline{RESET}$
L	N	L
L	Y	L
H	N	L
H	Y	H

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**Table 3. MAXIMUM RATINGS**

Rating	Symbol	Value	Unit
Input voltage range, $V_{DD}$	$V_{DD}$	-0.3 to + 6.0	V
CT voltage range $V_{CT}$ , RESET, MR Current through CT pin	$I_{CT}$	-0.3 to $V_{DD} + 0.3 \leq 6.0$ 10	V mA
SENSE pin voltage		-0.3 to + 8.0	V
RESET pin current		5	mA
Thermal Resistance Junction-to-Air TSOP-6 WDFN6	$R_{\theta JA}$	305 220	°C/W
Human Body Model (HBM) ESD Rating (Note 1)	ESD HBM	2000	V
Machine Model (MM) ESD Rating (Note 1)	ESD MM	100	V
Charged Device Model (CDM) ESD Rating (Note 1)	ESD CDM	500	V
Latch up Current: (Note 2) All pins, except digital pins Digital pins (MR)	$I_{LU}$	$\pm 100$ $\pm 10$	mA
Storage Temperature Range	$T_{STG}$	-65 to + 150	°C
Maximum Junction Temperature	$T_J$	-40 to +150	°C
Moisture Sensitivity (Note 3)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and passes the following tests:  
Human Body Model (HBM) +/-2.0 kV per JEDEC standard: JESD22-A114  
Machine Model (MM) +/-100 V per JEDEC standard: JESD22-A115  
Charged Device Model (CDM) 500 V per JEDEC standard: JESD22-C101.
2. Latch up Current per JEDEC standard: JESD78 class II.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020A.

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**Table 4. ELECTRICAL CHARACTERISTICS**  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $R_{pullup} = 100\text{ k}\Omega$ ,  $C_{LRESET} = 50\text{ pF}$ , over operating temperature range ( $T_J = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ), unless otherwise specified. Typical values are at  $T_J = +25^\circ\text{C}$ .

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
$V_{DD}$	Supply Voltage Range		$-40^\circ\text{C} < T_J < +125^\circ\text{C}$	1.6		5.5	V
$V_{DD(min)}$	Minimum $V_{DD}$ Guaranteed RESET Output Valid (Note 4)				0.5	0.8	V
$I_{DD}$	Supply Current (Current into VDD pin)		$V_{DD} = 3.3\text{V}$ , RESET not asserted MR, RESET, CT open		1.6	5.0	$\mu\text{A}$
			$V_{DD} = 5.5\text{V}$ , RESET not asserted MR, RESET, CT open		1.6	6.0	
$V_{OL}$	Low-level output voltage of RESET		$1.3\text{V} \leq V_{DD} < 1.6\text{V}$ , $I_{OL} = 0.4\text{ mA}$			0.3	V
			$1.6\text{V} \leq V_{DD} \leq 5.5\text{V}$ , $I_{OL} = 1.0\text{ mA}$			0.4	
$V_{IT\%}$	Negative going SENSE threshold voltage accuracy			-1.75	$\pm 0.75$	+1.75	%
			$T_J = +25^\circ\text{C}$	-0.31	-	0.31	
			$-20^\circ\text{C} < T_J < +85^\circ\text{C}$	-1.0	$\pm 0.5$	+1.0	
$V_{HYS}$	Hysteresis on $V_{IT}$	$1.6\text{V} \leq V_{DD} \leq 4.2\text{V}$			1.0	3.0	% $V_{IT}$
		$4.2\text{V} \leq V_{DD} \leq 5.5\text{V}$			1.75	3.75	
$R_{MR}$	MR Internal pull-up resistance				90		$\text{k}\Omega$
$I_{SENSE}$	Input current at SENSE pin	NCP308XXADJ	$V_{SENSE} = V_{IT}$		10		nA
		Fixed versions	$V_{SENSE} = 5.5\text{ V}$		110		
$I_{OH}$	RESET leakage Current		$V_{RESET} = 5.5\text{ V}$ , RESET not asserted			300	nA
$C_{IN}$	Input capacitance, any pin	CT pin	$V_{IN} = 0\text{ V to } V_{DD}$		5		pF
		Other pins	$V_{IN} = 0\text{ V to } 5.5\text{ V}$		5		
$V_{IL}$	MR logic low input			0		$0.3 V_{DD}$	V
$V_{IH}$	MR logic high input			$0.7 V_{DD}$		$V_{DD}$	V
$t_w$	Input pulse width to assert RESET	SENSE	$V_{IH} = 1.05 V_{IT}$ , $V_{IL} = 0.95 V_{IT}$		20		$\mu\text{s}$
		MR	$V_{IH} = 0.7 V_{DD}$ , $V_{IL} = 0.3 V_{DD}$		150		
$t_D$	Reset delay time	$C_T = \text{Open}$ $C_T = V_{DD}$ $C_T = 100\text{ pF}$ $C_T = 180\text{ nF}$	(Guaranteed by design and characterization)		20 300 1.25 1200		ms
$t_{P1}$	Propagation delay from MR	MR to RESET	$V_{IH} = 0.7 V_{DD}$ , $V_{IL} = 0.3 V_{DD}$		150		ns
$t_{P2}$	Propagation delay from SENSE	SENSE to RESET	$V_{IH} = 1.05 V_{IT}$ , $V_{IL} = 0.95 V_{IT}$		20		$\mu\text{s}$

4. The lowest supply voltage ( $V_{DD}$ ) at which RESET becomes active.

5. NCP308XX: XX = MT (WDFN6 package) or SN (TSOP-6 package).

TYPICAL OPERATING CHARACTERISTICS

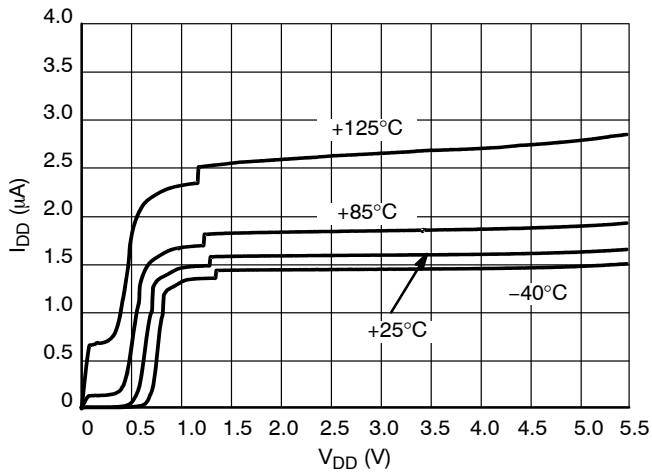


Figure 6. Supply Current vs. Input Voltage

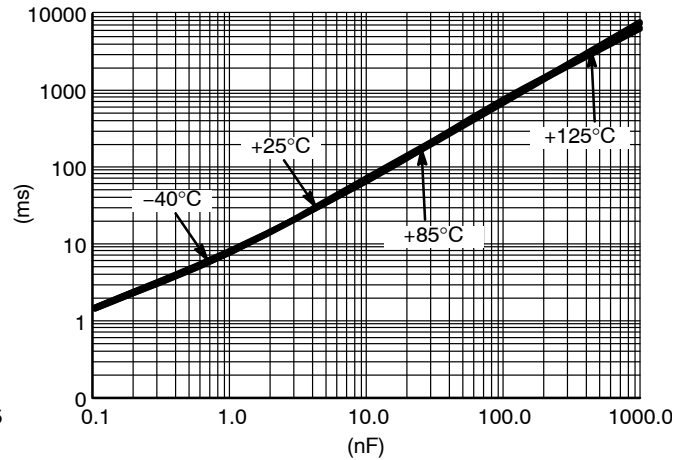


Figure 7. RESET Timeout Period vs. CT

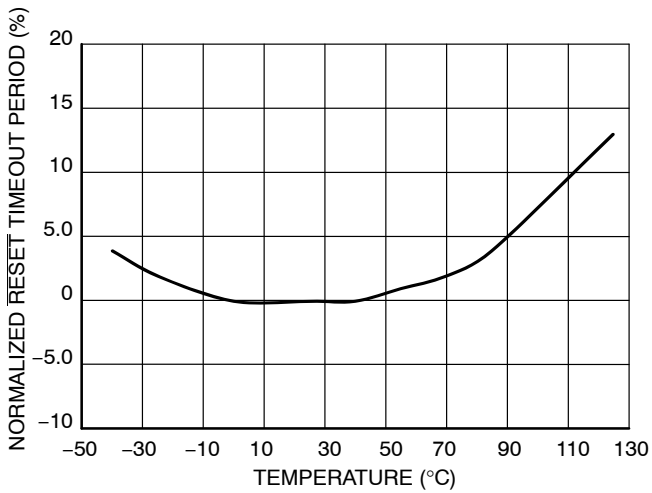


Figure 8. Normalized RESET Timeout Period vs. Temperature

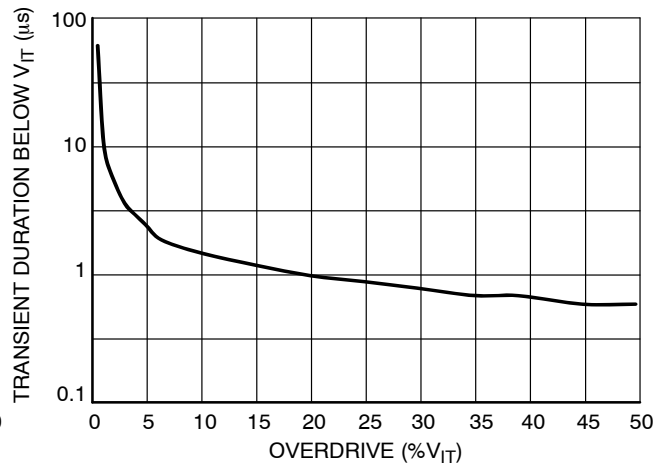


Figure 9. Maximum Transient Duration at Sense vs. Sense Threshold Overdrive Voltage

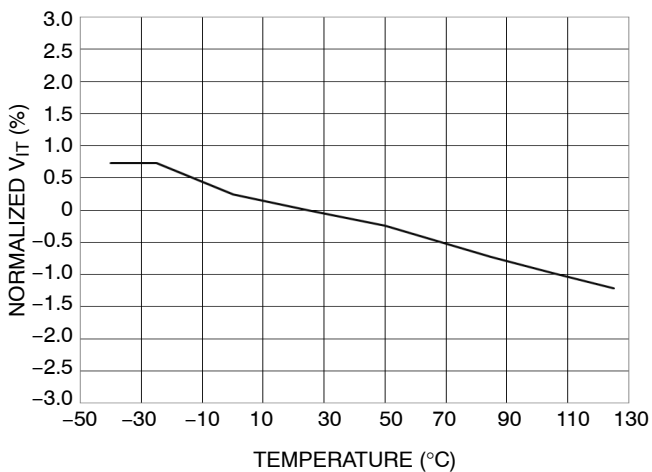


Figure 10. Normalized Sense Threshold Voltage ( $V_{IT}$ ) vs. Temperature

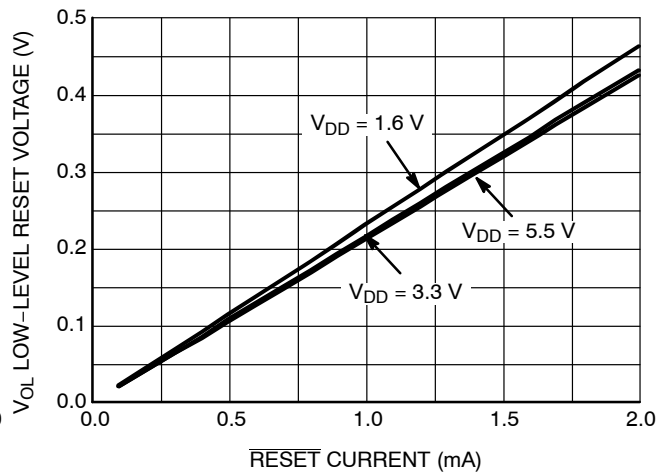


Figure 11. Low-Level RESET Voltage vs. RESET Current

## DETAILED DESCRIPTION

The NCP308 microprocessor supervisory product family is designed to assert a  $\overline{\text{RESET}}$  signal when either the SENSE pin voltage drops below  $V_{IT}$  or the Manual Reset input ( $\overline{\text{MR}}$ ) is driven low. The  $\overline{\text{RESET}}$  output remains asserted for a programmable delay time after both  $\overline{\text{MR}}$  and SENSE voltages return above the respective thresholds. A broad range of voltage threshold and reset delay time options are available, allowing NCP308 series to be used in a wide range of applications.

Reset threshold voltages can be factory-set from 0.82 V to 3.3 V or from 4.4 V to 5.0 V, while the NCP308XXADJ can be used for any voltage above 0.405 V using an external resistor divider.

Flexible delay time can be easily got with CT pin according to Table 5:

**Table 5. DELAY TIME SETTING TABLE**

CT pin Configuration	Delay Time (tD)
CT = VDD	300 ms (fixed)
CT = Open	20 ms (fixed)
Connecting a capacitor between pin CT and GND (Capacitor CT value > 100 pF)	1.25 ms ~ 10 s, depends on capacitor value (Refer to the Setting Reset Delay Time Section)

### Output

The  $\overline{\text{RESET}}$  output is typically connected to the  $\overline{\text{RESET}}$  control pin of a microprocessor. For Open-Drain output versions, a pull-up resistor must be used to hold this line high when  $\overline{\text{RESET}}$  is not asserted. The  $\overline{\text{RESET}}$  output is active once  $V_{DD}$  is over  $V_{DD}(\text{min})$ , this voltage is much lower than most microprocessors' functional voltage range.  $\overline{\text{RESET}}$  remains high as long as SENSE is above its threshold ( $V_{IT}$ ) and the Manual Reset input ( $\overline{\text{MR}}$ ) is logic high. If either SENSE falls below  $V_{IT}$  or  $\overline{\text{MR}}$  is driven low,  $\overline{\text{RESET}}$  is asserted.

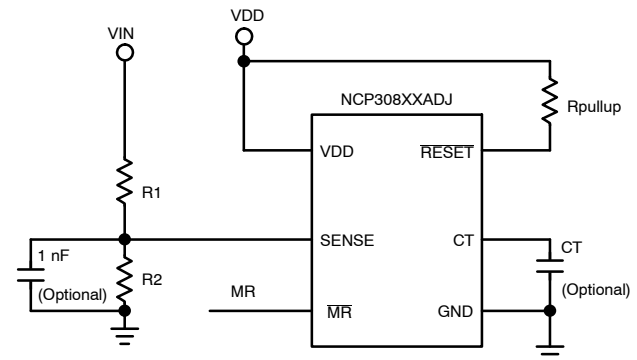
Once  $\overline{\text{MR}}$  is again logic high and SENSE is above ( $V_{IT} + V_{HYS}$ ), the  $\overline{\text{RESET}}$  pin goes to a high impedance state after delay time (tD). The open-drain structure of  $\overline{\text{RESET}}$  is capable to allow the reset signal for the microprocessor to have a voltage higher than  $V_{DD}$  (up to 5.5 V). The pull-up resistor should be no smaller than 10 k $\Omega$  as a result of the finite impedance of the  $\overline{\text{RESET}}$  line.

### SENSE Input

The SENSE input should be connected to the monitored voltage directly. If the voltage on this pin drops below  $V_{IT}$ , then  $\overline{\text{RESET}}$  is asserted. The comparator has a built-in hysteresis to prevent erratic reset operation. It is good practice to put a 1 nF to 10 nF bypass capacitor on the SENSE input to reduce its sensitivity to transients and layout parasitic.

The NCP308XXADJ can be used to monitor any voltage rail down to 0.405 V by the circuit shown in Figure 12. The new  $V_{IT}'$  can be derived from resistor divider network of R1 and R2 by:

$$V_{IT}' = \left( \frac{R1}{R2} + 1 \right) \times V_{IT} \quad (\text{eq. 1})$$



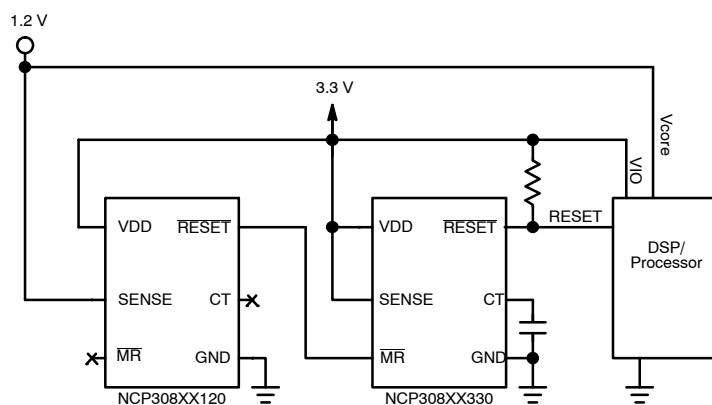
**Figure 12. Using NCP308XXADJ to Monitor a User-Defined Threshold Voltage**

### Manual Reset Input ( $\overline{\text{MR}}$ )

The Manual Reset input ( $\overline{\text{MR}}$ ) allows a processor or other logic circuits to initiate a reset. A logic low on  $\overline{\text{MR}}$  causes  $\overline{\text{RESET}}$  to assert. After  $\overline{\text{MR}}$  returns to a logic high and SENSE is above its reset threshold,  $\overline{\text{RESET}}$  is de-asserted after the delay time set by CT pin.  $\overline{\text{MR}}$  is internally tied to  $V_{DD}$  by a 90 k $\Omega$  resistor so this pin can be left unconnected if  $\overline{\text{MR}}$  will not be used.

Figure 13 shows how  $\overline{\text{MR}}$  can be used to monitor multiple system voltages (e.g. I/O supply voltage of some DSP/processors should be setup before core voltage, and DSP/processor can only start after both I/O and core voltages setup).

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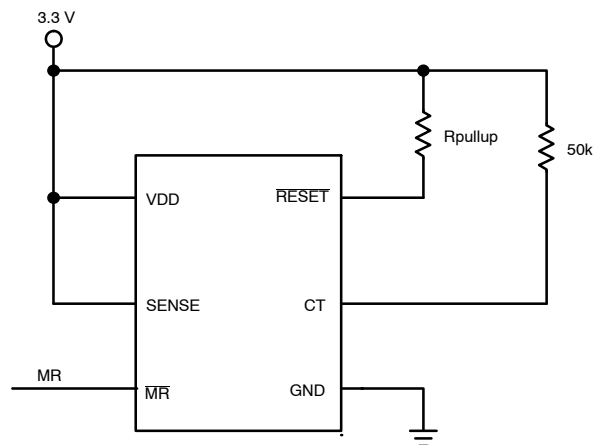


**Figure 13. Using  $\overline{\text{MR}}$  to Monitor Multiple System Voltages**

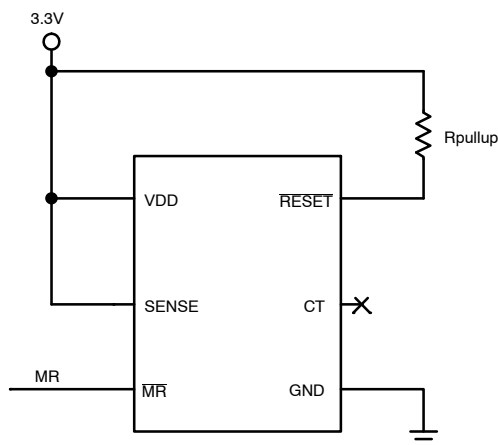
### Setting Reset Delay Time

The NCP308 has three options for setting the reset delay time as shown in Table 5. Figure 14 shows the configuration for a fixed 300 ms typical delay time by tying CT to  $\text{V}_{\text{DD}}$ ; a resistor from 40 k $\Omega$  to 200 k $\Omega$  must be used. Figure 15 shows a fixed 20 ms delay time by leaving the CT pin unconnected.

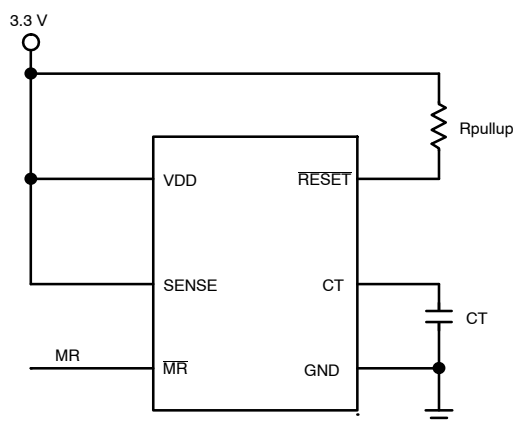
Figure 16 shows a user-defined program time between 1.25 ms and 10 s by connecting a capacitor between CT pin and ground.



**Figure 14. Delay Time Fixed to 300 ms when CT Connected to  $\text{V}_{\text{DD}}$  by Resistor**



**Figure 15. Delay Time Fixed to 20 ms when CT is Open**



**Figure 16. Delay Time Set by Capacitor**

The capacitor CT should be  $\geq 100$  pF for NCP308 to recognize that the capacitor is present. The capacitor value for a given delay time can be calculated using the following equation:



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$$CT(nF) = (tD(s) - 0.5 \times 10^{-3}(s)) \times 175 \quad (\text{eq. 2})$$

Parasitic capacitances of CT pin should be considered to avoid reset delay time deviation or error.

threshold overdrive, as shown in the Maximum Transient Duration at Sense vs. Sense Threshold Overdrive Voltage graph (Figure 9) in Typical Operating Characteristics section.

### Immunity to Sense Pin Voltage Transients

NCP308 is relatively immune to short negative transients on SENSE pin. Sensitivity to transients is dependent on

### ORDERING INFORMATION

Device	Status (Note 6)	Threshold Voltage (V <sub>IT</sub> )	Nominal Monitored Voltage	Marking	Package	Shipping <sup>†</sup>
NCP308SNADJT1G	Active	0.405 V	Adjustable Version	ADJ	TSOP-6 (Pb-Free)	3000 / Tape & Reel
NCV308SNADJT1G*	Active	0.405 V		VDJ		
NCP308SN090T1G	Active	0.84 V	0.9 V	090		
NCP308SN120T1G	Active	1.12 V	1.2 V	120		
NCP308SN125T1G	Active	1.16 V	1.25 V	125		
NCP308SN150T1G	Active	1.40 V	1.5 V	150		
NCP308SN180T1G	Active	1.67 V	1.8 V	180		
NCP308SN190T1G	Active	1.77 V	1.9 V	190		
NCP308SN250T1G	Active	2.33 V	2.5 V	250		
NCP308SN280T1G	Active	2.61 V	2.8 V	280		
NCP308SN300T1G	Active	2.79 V	3.0 V	300		
NCP308SN330T1G	Active	3.07 V	3.3 V	330		
NCV308SN330T1G*	Active	3.07 V	3.3 V	33A		
NCP308SN500T1G	Active	4.65 V	5.0 V	500		
NCP308MTADJTBG	Active	0.405 V	Adjustable Version	AA	WDFN6 (Pb-Free)	
NCP308MT090TBG	Active	0.84 V	0.9 V	AC		
NCP308MT120TBG	Active	1.12 V	1.2 V	AD		
NCP308MT125TBG	Active	1.16 V	1.25 V	AE		
NCP308MT150TBG	Active	1.40 V	1.5 V	AF		
NCP308MT180TBG	Active	1.67 V	1.8 V	AG		
NCP308MT190TBG	Active	1.77 V	1.9 V	AH		
NCP308MT250TBG	Active	2.33 V	2.5 V	AJ		
NCP308MT280TBG	Active	2.61 V	2.8 V	AK		
NCP308MT300TBG	Active	2.79 V	3.0 V	AL		
NCP308MT330TBG	Active	3.07 V	3.3 V	AM		
NCP308MT500TBG	Active	4.65 V	5.0 V	AN		

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

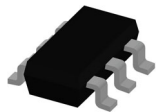
\*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

6. The marketing status are defined as below:

Active: Products in production and recommended for new designs;

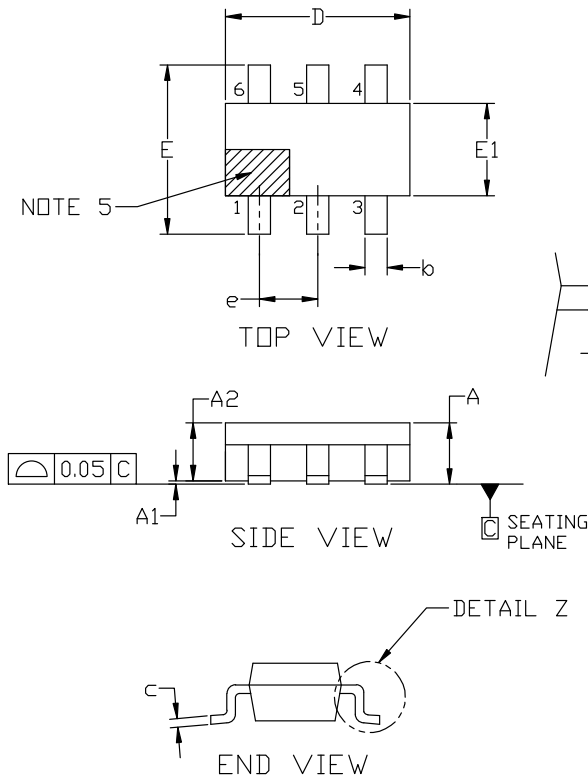
Under Request: Device has been announced but is not in production. Samples may or may not be available.

**MECHANICAL CASE OUTLINE**  
**PACKAGE DIMENSIONS**

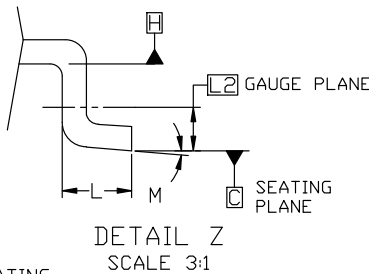


**TSOP-6 3.00x1.50x0.90, 0.95P**  
**CASE 318G**  
**ISSUE W**

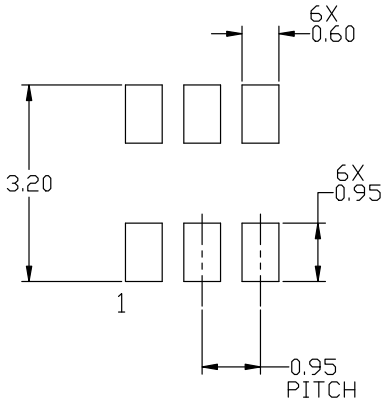
**DATE 26 FEB 2024**



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
  2. CONTROLLING DIMENSION: MILLIMETERS.
  3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
  4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
  5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



**RECOMMENDED MOUNTING FOOTPRINT**

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98ASB14888C</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TSOP-6 3.00x1.50x0.90, 0.95P</b>	<b>PAGE 1 OF 2</b>

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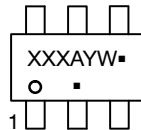
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

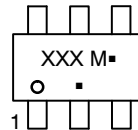
TSOP-6 3.00x1.50x0.90, 0.95P  
CASE 318G  
ISSUE W

DATE 26 FEB 2024

### GENERIC MARKING DIAGRAM\*



IC



STANDARD

XXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

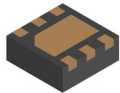
STYLE 1: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN	STYLE 2: PIN 1. EMITTER 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. BASE 2 6. COLLECTOR 2	STYLE 3: PIN 1. ENABLE 2. N/C 3. R BOOST 4. Vz 5. V in 6. V out	STYLE 4: PIN 1. N/C 2. V in 3. NOT USED 4. GROUND 5. ENABLE 6. LOAD	STYLE 5: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2	STYLE 6: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR
STYLE 7: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. N/C 5. COLLECTOR 6. EMITTER	STYLE 8: PIN 1. Vbus 2. D(in) 3. D(in)+ 4. D(out)+ 5. D(out) 6. GND	STYLE 9: PIN 1. LOW VOLTAGE GATE 2. DRAIN 3. SOURCE 4. DRAIN 5. DRAIN 6. HIGH VOLTAGE GATE	STYLE 10: PIN 1. D(OUT)+ 2. GND 3. D(OUT)- 4. D(IN)- 5. VBUS 6. D(IN)+	STYLE 11: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1/GATE 2	STYLE 12: PIN 1. I/O 2. GROUND 3. I/O 4. I/O 5. VCC 6. I/O
STYLE 13: PIN 1. GATE 1 2. SOURCE 2 3. GATE 2 4. DRAIN 2 5. SOURCE 1 6. DRAIN 1	STYLE 14: PIN 1. ANODE 2. SOURCE 3. GATE 4. CATHODE/DRAIN 5. CATHODE/DRAIN 6. CATHODE/DRAIN	STYLE 15: PIN 1. ANODE 2. SOURCE 3. GATE 4. DRAIN 5. N/C 6. CATHODE	STYLE 16: PIN 1. ANODE/CATHODE 2. BASE 3. EMITTER 4. COLLECTOR 5. ANODE 6. CATHODE	STYLE 17: PIN 1. EMITTER 2. BASE 3. ANODE/CATHODE 4. ANODE 5. CATHODE 6. COLLECTOR	

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DESCRIPTION:	TSOP-6 3.00x1.50x0.90, 0.95P	PAGE 2 OF 2

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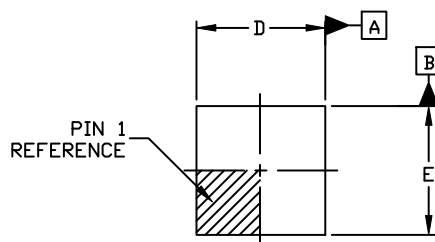
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

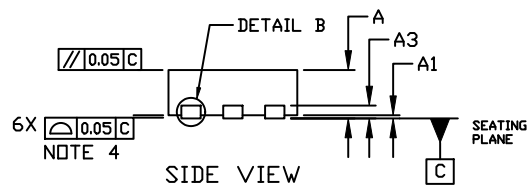


**WDFN6 2x2, 0.65P**  
CASE 511BR  
ISSUE C

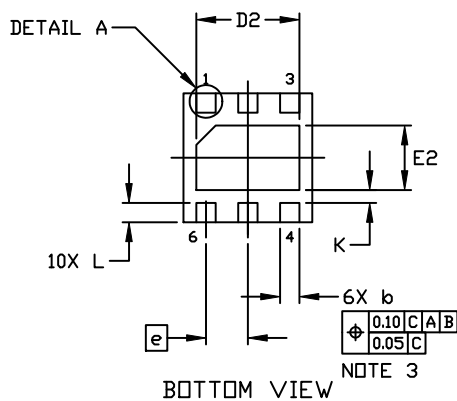
DATE 01 DEC 2021



TOP VIEW



SIDE VIEW



BOTTOM VIEW

### GENERIC MARKING DIAGRAM\*

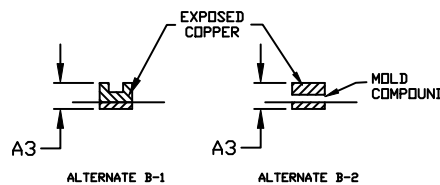


XX = Specific Device Code  
M = Date Code

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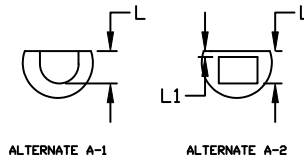
### NOTES:

1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



DETAIL B

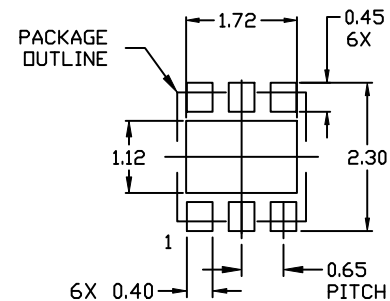
ALTERNATE CONSTRUCTION



DETAIL A

ALTERNATE CONSTRUCTIONS

DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e	0.65 BSC		
K	0.20 REF		
L	0.20	0.30	0.40
L1	---	---	0.15



### RECOMMENDED MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>WDFN6 2X2, 0.65P</b>	<b>PAGE 1 OF 1</b>

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