TMUX1247 5-V Bidirectional, 2:1 (SPDT) General Purpose Switch

1 Features

- Rail to rail operation
- Bidirectional signal path
- 1.8 V Logic compatible
- Fail-safe logic
- Low on-resistance: 3 Ω
- Wide supply range: 1.08 V to 5.5 V
- -40°C to +125°C Operating temperature
- Low supply current: 4 nA
- Transition time: 14 ns
- Break-before-make switching
- ESD protection HBM: 2000 V

2 Applications

- Analog and Digital Switching
- I2C and SPI bus Multiplexing
- Remote radio units
- Active antenna system mMIMO (AAS)
- Barcode scanner
- Motor drives
- Building automation
- Analog input module
- Power delivery
- Video surveillance
- Electronic point of sale
- Appliances
- Consumer audio

3 Description

The TMUX1247 is a general purpose complementary metal-oxide semiconductor (CMOS) single-pole double-throw (SPDT) switch. The TMUX1247 switches between two source inputs based on the state of the SEL pin. Wide operating supply of 1.08 V to 5.5 V allows for use in a broad array of applications from personal electronics to building automation. The device supports bidirectional analog and digital signals on the source (Sx) and drain (D) pins ranging from GND to V_{DD}. A low supply current of 4 nA enables use in portable applications.

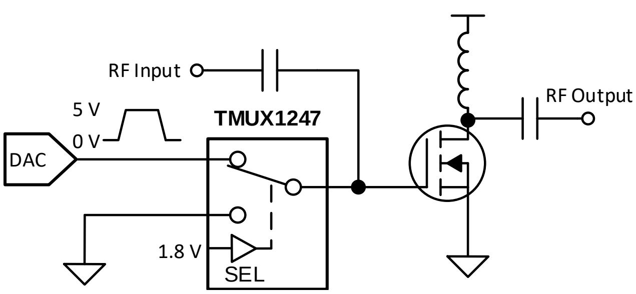
All logic inputs have 1.8 V logic compatible thresholds, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range. Fail-Safe Logic circuitry allows voltages on the control pins to be applied before the supply pin, protecting the device from potential damage.

Device Information(1)

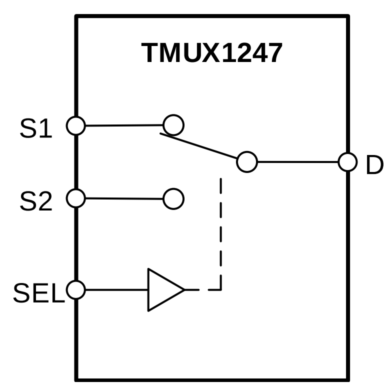
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMUX1247	SC70 (6)	2.00 mm × 1.25 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Application Example



TMUX1247 Block Diagram



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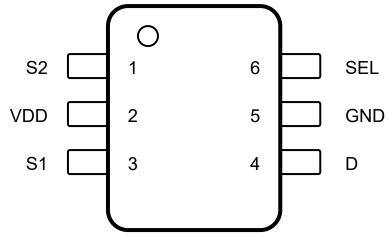
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2019	*	Initial release.

5 Pin Configuration and Functions

DCK Package
6-Pin SC70
Top View



Not to scale

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
S2	1	I/O	Source pin 2. Can be an input or output.
V_{DD}	2	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
S1	3	I/O	Source pin 1. Can be an input or output.
D	4	I/O	Drain pin. Can be an input or output.
GND	5	P	Ground (0 V) reference
SEL	6	I	Select pin: controls state of the switch according to Table 1. (Logic Low = S1 to D, Logic High = S2 to D)

(1) I = input, O = output, I/O = input and output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)(2)(3)]

		MIN	MAX	UNIT
V_{DD}	Supply voltage	–0.5	6	V
V_{SEL} or V_{EN}	Logic control input pin voltage (SEL)	–0.5	6	V
I_{SEL} or I_{EN}	Logic control input pin current (SEL)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	–0.5	V_{DD}+0.5	V
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx, D)	–50	50	mA
I_K	Diode clamp current[(4)]	–30	30	mA
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature		150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	1.08		5.5	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)	0		V_{DD}	V
V_{SEL}	Logic control input pin voltage (SEL)	0		5.5	V
T_A	Ambient temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[(1)]		TMUX1247 DCK (SC70) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	243.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	180.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	106.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	89.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	106.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics (V_{DD} = 5 V ±10 %), GND = 0 V unless otherwise specified.

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		3		Ω
			–40°C to +85°C			5	Ω
			–40°C to +125°C			6	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.15		Ω
			–40°C to +85°C			1	Ω
			–40°C to +125°C			1	Ω
R_{ON} FLAT	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		1.5		Ω
			–40°C to +85°C		2		Ω
			–40°C to +125°C		3		Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 5 V Switch Off V_D = 4.5 V / 1.5 V V_S = 1.5 V / 4.5 V Refer to Off-Leakage Current	25°C		±75		nA
			–40°C to +85°C	–150		150	nA
			–40°C to +125°C	–175		175	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 5 V Switch On V_D = V_S = 4.5 V / 1 V Refer to On-Leakage Current	25°C		±200		nA
			–40°C to +85°C	–500		500	nA
			–40°C to +125°C	–750		750	nA
LOGIC INPUTS							
V_{IH}	Input logic high		-40°C to 125°C	1.42		5.5	V
V_{IL}	Input logic low		-40°C to 125°C	0		0.87	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Digital input capacitance		25°C		1		pF
C_{IN}	Digital input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Digital Inputs = 0 V or 5.5 V	25°C		0.007		µA
			–40°C to +125°C			1.5	µA

(1) When V_S is 4.5 V, V_D is 1.5 V or when V_S is 1.5 V, V_D is 4.5 V.

Electrical Characteristics (V_{DD} = 5 V ±10 %), GND = 0 V unless otherwise specified. (continued)

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Switching time between channels	V_S = 3 V R_L = 200 Ω, C_L = 15 pF	25°C		12		ns
			–40°C to +85°C			18	ns
			–40°C to +125°C			19	ns
t_{OPEN} (BBM)	Break before make time	V_S = 3 V R_L = 200 Ω, C_L = 15 pF	25°C		8		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_S = V_{DD} /2 R_S = 0 Ω, C_L = 1 nF	25°C		–10		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz	25°C		–45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF	25°C		250		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		23		pF

6.6 Electrical Characteristics (V_{DD} = 3.3 V ±10 %), GND = 0 V unless otherwise specified.

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		4.5		Ω
			–40°C to +85°C			12.5	Ω
			–40°C to +125°C			13	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.15		Ω
			–40°C to +85°C			1	Ω
			–40°C to +125°C			1	Ω
R_{ON} FLAT	On-resistance flatness	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		3.5		Ω
			–40°C to +85°C		4		Ω
			–40°C to +125°C		5		Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 3.3 V Switch Off V_D = 3 V / 1 V V_S = 1 V / 3 V Refer to Off-Leakage Current	25°C		±75		nA
			–40°C to +85°C	–150		150	nA
			–40°C to +125°C	–175		175	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 3.3 V Switch On V_D = V_S = 3 V / 1 V Refer to On-Leakage Current	25°C		±200		nA
			–40°C to +85°C	–500		500	nA
			–40°C to +125°C	–750		750	nA
LOGIC INPUTS							
V_{IH}	Input logic high		-40°C to 125°C	1.35		5.5	V
V_{IL}	Input logic low		-40°C to 125°C	0		0.8	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Digital Inputs = 0 V or 5.5 V	25°C		0.004		µA
			–40°C to +125°C			0.8	µA

(1) When V_S is 3 V, V_D is 1 V or when V_S is 1 V, V_D is 3 V.

Electrical Characteristics (V_{DD} = 3.3 V ±10 %), GND = 0 V unless otherwise specified. (continued)

at T_A = 25°C, V_{DD} = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Switching time between channels	V_S = 2 V R_L = 200 Ω, C_L = 15 pF	25°C		14		ns
			–40°C to +85°C			20	ns
			–40°C to +125°C			22	ns
t_{OPEN} (BBM)	Break before make time	V_S = 2 V R_L = 200 Ω, C_L = 15 pF	25°C		8		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_S = V_{DD}/2 R_S = 0 Ω, C_L = 1 nF	25°C		–6		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF Refer to Bandwidth	25°C		250		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		23		pF

6.7 Electrical Characteristics (V_{DD} = 1.8 V ±10 %), GND = 0 V unless otherwise specified.

at T_A = 25°C, V_{DD} = 1.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		40		Ω
			–40°C to +85°C			80	Ω
			–40°C to +125°C			80	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{SD} = 10 mA Refer to On-Resistance	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current[1]	V_{DD} = 1.98 V Switch Off V_D = 1.8 V / 1 V V_S = 1 V / 1.8 V Refer to Off-Leakage Current	25°C		±75		nA
			–40°C to +85°C	–150		150	nA
			–40°C to +125°C	–175		175	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.98 V Switch On V_D = V_S = 1.62 V / 1 V	25°C		±200		nA
			–40°C to +85°C	–500		500	nA
			–40°C to +125°C	–750		750	nA
DIGITAL INPUTS							
V_{IH}	Input logic high		–40°C to +125°C	1.07		5.5	V
V_{IL}	Input logic low		–40°C to +125°C	0		0.68	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.05	µA
C_{IN}	Logic input capacitance		25°C		1		pF
C_{IN}	Logic input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Logic Inputs = 0 V or 5.5 V	25°C		0.002		µA
			–40°C to +125°C			0.52	µA

(1) When V_S is 1.8 V, V_D is 1 V or when V_S is 1 V, V_D is 1.8 V.

Electrical Characteristics (V_{DD} = 1.8 V ±10 %), GND = 0 V unless otherwise specified. (continued)

at T_A = 25°C, V_{DD} = 1.8 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
LOGIC INPUTS							
t_{TRAN}	Switching time between channels	V_S = 1 V R_L = 200 Ω, C_L = 15 pF	25°C		24		ns
			–40°C to +85°C			44	ns
			–40°C to +125°C			45	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF	25°C		16		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_S = V_{DD}/2 R_S = 0 Ω, C_L = 1 nF	25°C		–3		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Off Isolation	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Off Isolation	25°C		–45		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz Refer to Crosstalk	25°C		–65		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz Refer to Crosstalk	25°C		–45		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF	25°C		250		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		23		pF

6.8 Electrical Characteristics (V_{DD} = 1.2 V ±10 %), GND = 0 V unless otherwise specified.

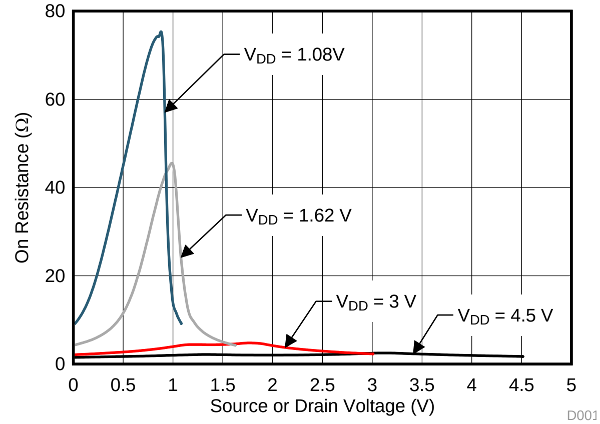
at T_A = 25°C, V_{DD} = 1.2 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TA	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to V_{DD} I_{DS} = 10 mA	25°C		70		Ω
			–40°C to +85°C			105	Ω
			–40°C to +125°C			105	Ω
ΔR_{ON}	On-resistance matching between channels	V_S = 0 V to V_{DD} I_{DS} = 10 mA	25°C		0.4		Ω
			–40°C to +85°C			1.5	Ω
			–40°C to +125°C			1.5	Ω
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 1.32 V Switch Off V_D = 1.2 V / 1 V V_S = 1 V / 1.2 V	25°C		±75		nA
			–40°C to +85°C	–150		150	nA
			–40°C to +125°C	–175		175	nA
$I_{D(ON)}$ $I_{S(ON)}$	Channel on leakage current	V_{DD} = 1.32 V Switch On V_D = V_S = 1 V / 0.8 V	25°C		±200		nA
			–40°C to +85°C	–500		500	nA
			–40°C to +125°C	–750		750	nA
DIGITAL INPUTS							
V_{IH}	Input logic high		–40°C to +125°C	0.96			V
V_{IL}	Input logic low		–40°C to +125°C			0.36	V
I_{IH} I_{IL}	Input leakage current		25°C		±0.005		µA
I_{IH} I_{IL}	Input leakage current		–40°C to +125°C			±0.10	µA
C_{IN}	Digital input capacitance		25°C		1		pF
C_{IN}	Digital input capacitance		–40°C to +125°C			2	pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	Digital Inputs = 0 V or 5.5 V	25°C		0.0015		µA
			–40°C to +125°C			0.45	µA
DYNAMIC CHARACTERISTICS							
t_{TRAN}	Switching time between channels	V_{IN} = V_{DD} V_S = 1 V R_L = 200 Ω, C_L = 15 pF	25°C		40		ns
			–40°C to +85°C			175	ns
			–40°C to +125°C			175	ns
t_{OPEN} (BBM)	Break before make time	V_S = 1 V R_L = 200 Ω, C_L = 15 pF	25°C		27		ns
			–40°C to +85°C	1			ns
			–40°C to +125°C	1			ns
Q_C	Charge Injection	V_S = (V_{DD} + V_{SS})/2 R_S = 0 Ω, C_L = 1 nF	25°C		±5		pC
O_{ISO}	Off Isolation	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	25°C		-64		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz	25°C		-44		dB
X_{TALK}	Crosstalk	R_L = 50 Ω, C_L = 5 pF f = 1 MHz	25°C		-64		dB
		R_L = 50 Ω, C_L = 5 pF f = 10 MHz	25°C		-44		dB
BW	Bandwidth	R_L = 50 Ω, C_L = 5 pF	25°C		250		MHz
C_{SOFF}	Source off capacitance	f = 1 MHz	25°C		7		pF
C_{SON} C_{DON}	On capacitance	f = 1 MHz	25°C		23		pF

(1) When V_S is 1 V, V_D is 1.2 V or when V_S is 1.2 V, V_D is 1 V.

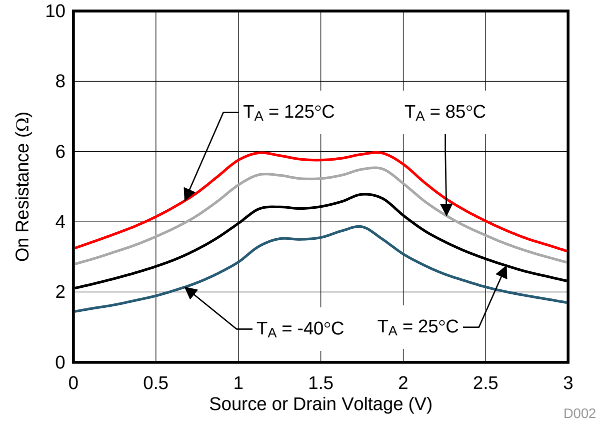
6.9 Typical Characteristics

at T_A = 25°C, V_{DD} = 5 V (unless otherwise noted)



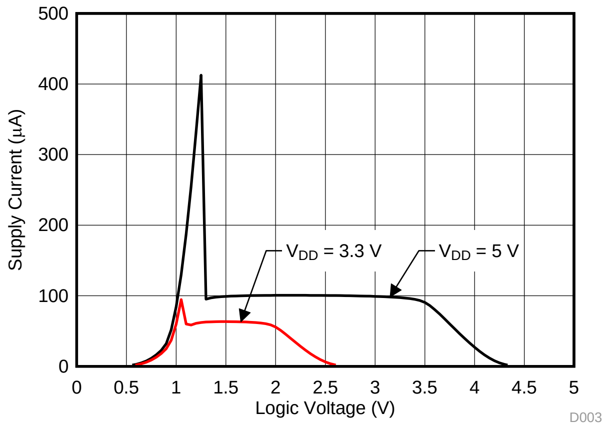
T_A = 25°C

Figure 1. On-Resistance vs Source or Drain Voltage



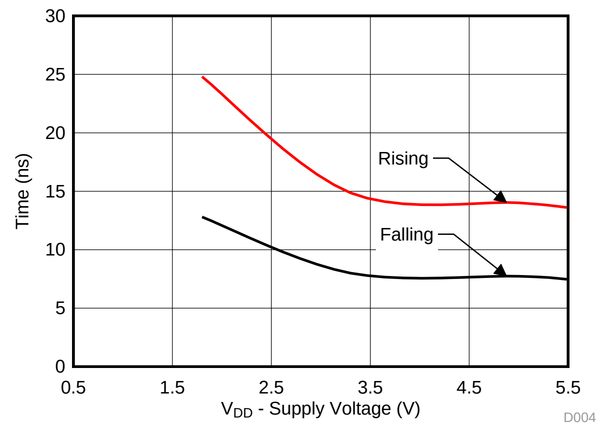
V_{DD} = 3 V

Figure 2. On-Resistance vs Source or Drain Voltage



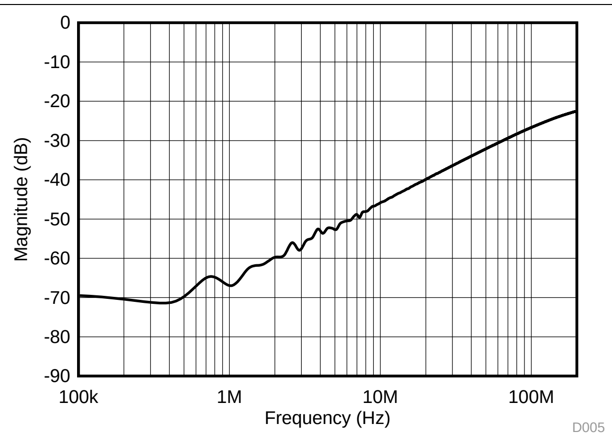
T_A = 25°C

Figure 3. Supply Current vs Logic Voltage



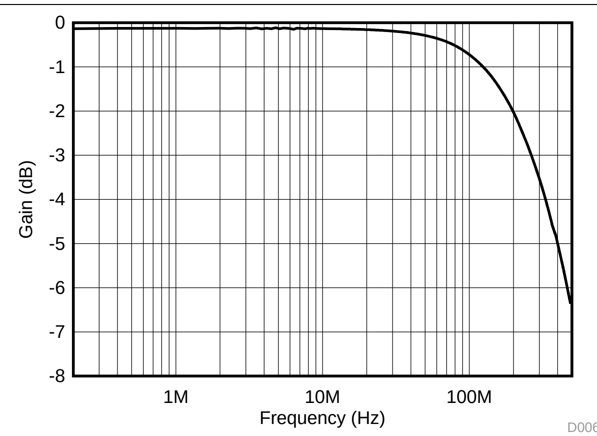
T_A = 25°C

Figure 4. $T_{transition}$ vs Supply Voltage



T_A = 25°C

Figure 5. Crosstalk and Off-Isolation vs Frequency



T_A = 25°C

Figure 6. Frequency Response

7 Parameter Measurement Information

7.1 On-Resistance

The on-resistance of a device is the ohmic resistance between the source (Sx) and drain (D) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in Figure 7. Voltage (V) and current (I_{SD}) are measured using this setup, and R_{ON} is computed with $R_{ON} = V / I_{SD}$:

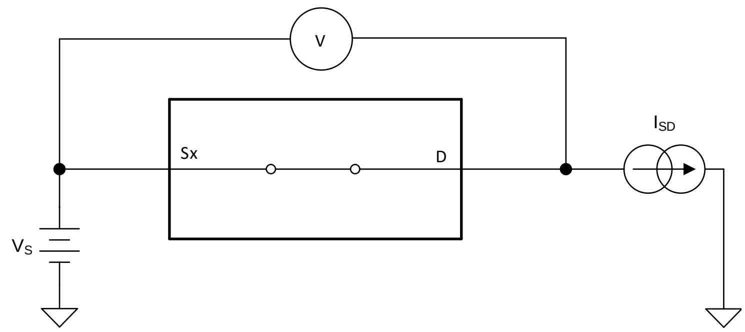


Figure 7. On-Resistance Measurement Setup

7.2 Off-Leakage Current

Source leakage current is defined as the leakage current flowing into or out of the source pin when the switch is off. This current is denoted by the symbol $I_{S(OFF)}$.

The setup used to measure off-leakage current is shown in Figure 8.

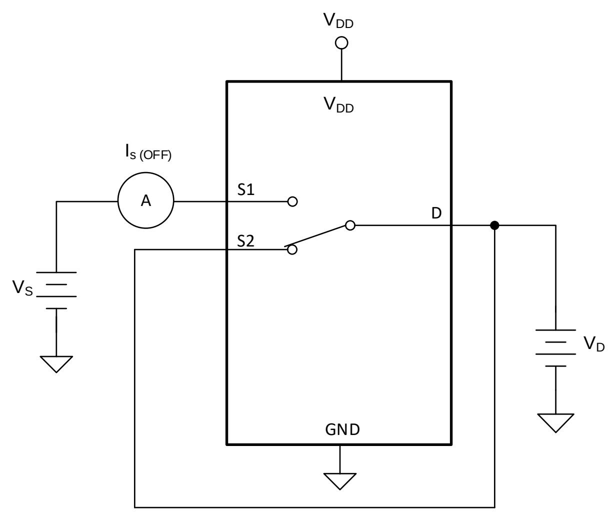


Figure 8. Off-Leakage Measurement Setup

7.3 On-Leakage Current

Source on-leakage current is defined as the leakage current flowing into or out of the source pin when the switch is on. This current is denoted by the symbol $I_{S(ON)}$.

Drain on-leakage current is defined as the leakage current flowing into or out of the drain pin when the switch is on. This current is denoted by the symbol $I_{D(ON)}$.

Either the source pin or drain pin is left floating during the measurement. Figure 9 shows the circuit used for measuring the on-leakage current, denoted by $I_{S(ON)}$ or $I_{D(ON)}$.

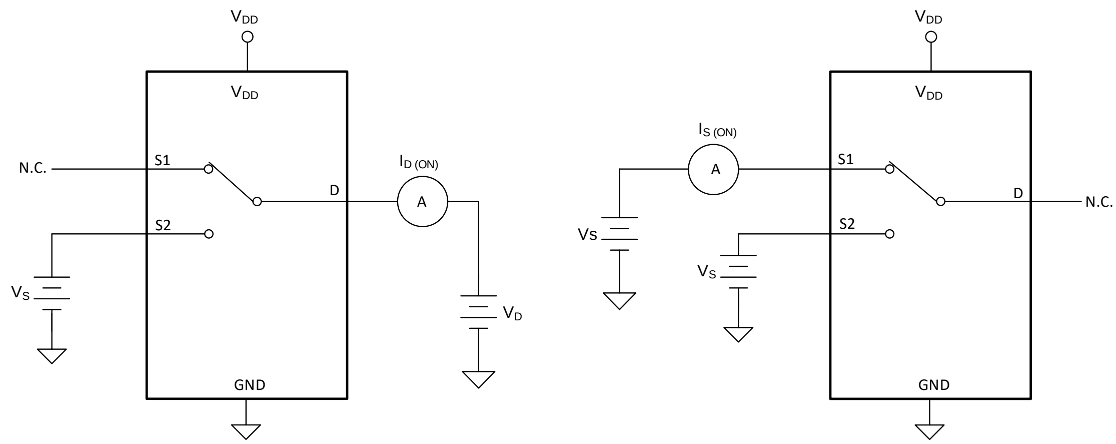


Figure 9. On-Leakage Measurement Setup

7.4 Transition Time

Transition time is defined as the time taken by the output of the device to rise or fall 10% after the logic control signal has risen or fallen past the logic threshold. The 10% transition measurement is utilized to provide the timing of the device. System level timing can then account for the time constant added from the load resistance and load capacitance. Figure 10 shows the setup used to measure transition time, denoted by the symbol $t_{TRANSITION}$.

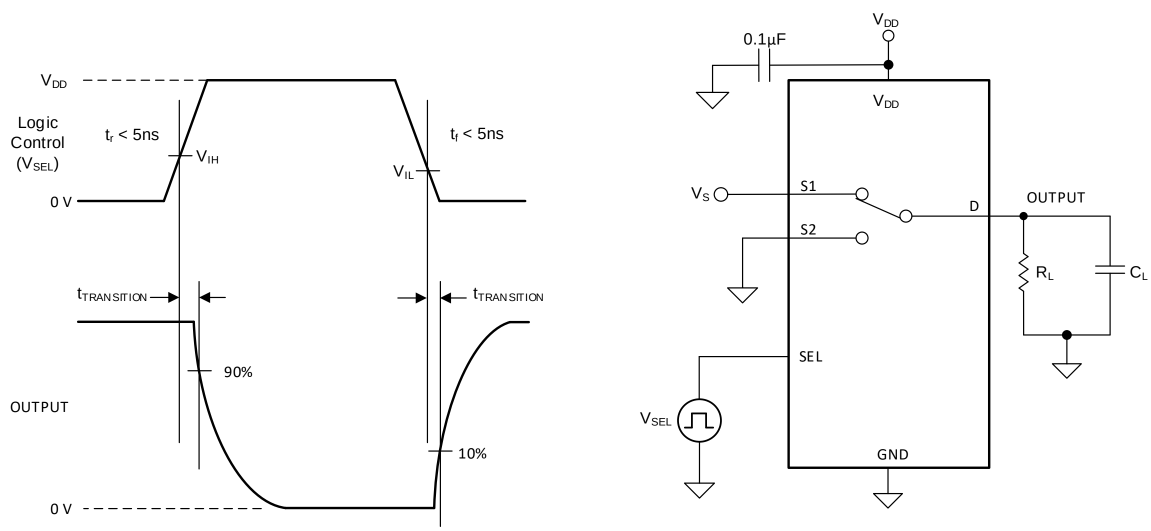


Figure 10. Transition-Time Measurement Setup

7.5 Break-Before-Make

Break-before-make delay is a safety feature that prevents two inputs from connecting when the device is switching. The output first breaks from the on-state switch before making the connection with the next on-state switch. The time delay between the *break* and the *make* is known as break-before-make delay. Figure 11 shows the setup used to measure break-before-make delay, denoted by the symbol $t_{OPEN(BBM)}$.

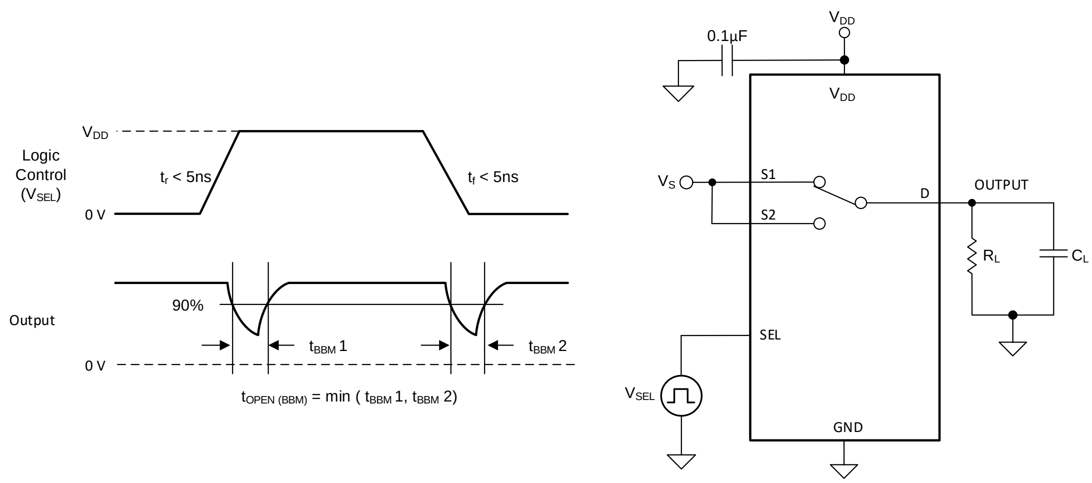


Figure 11. Break-Before-Make Delay Measurement Setup

7.6 Charge Injection

The TMUX1247 has a transmission-gate topology. Any mismatch in capacitance between the NMOS and PMOS transistors results in a charge injected into the drain or source during the falling or rising edge of the gate signal. The amount of charge injected into the source or drain of the device is known as charge injection, and is denoted by the symbol Q_C. Figure 12 shows the setup used to measure charge injection from Drain (D) to Source (Sx).

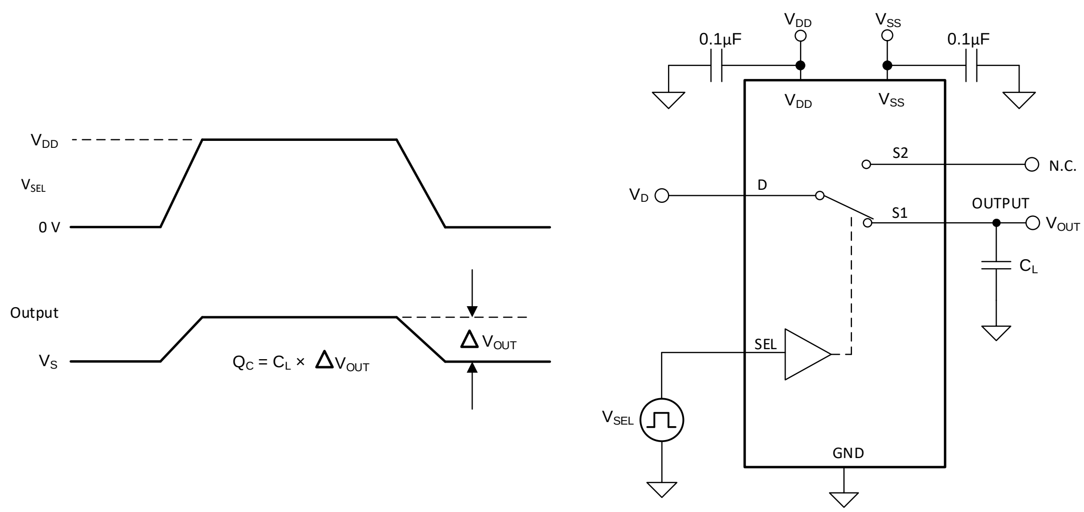


Figure 12. Charge-Injection Measurement Setup

7.7 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (D) of the device when a signal is applied to the source pin (Sx) of an off-channel. Figure 13 shows the setup used to measure, and the equation used to calculate off isolation.

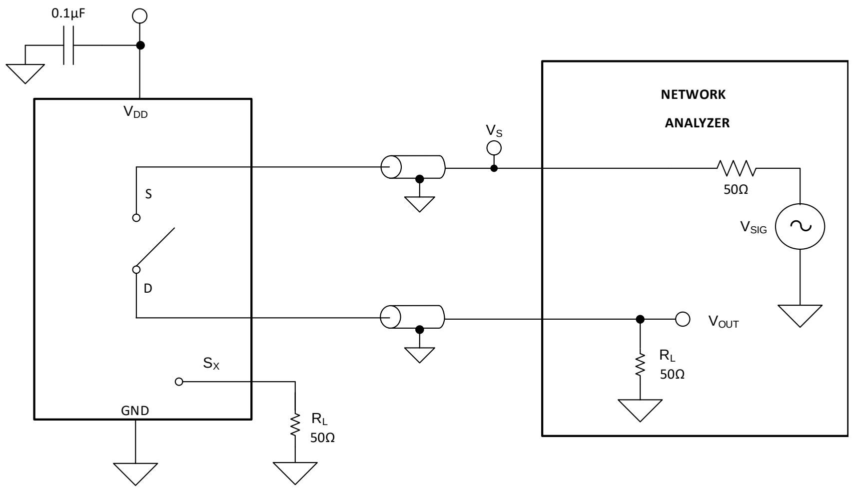


Figure 13. Off Isolation Measurement Setup

$$\text{Off Isolation} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (1)$$

7.8 Crosstalk

Crosstalk is defined as the ratio of the signal at the drain pin (D) of a different channel, when a signal is applied at the source pin (Sx) of an on-channel. Figure 14 shows the setup used to measure, and the equation used to calculate crosstalk.

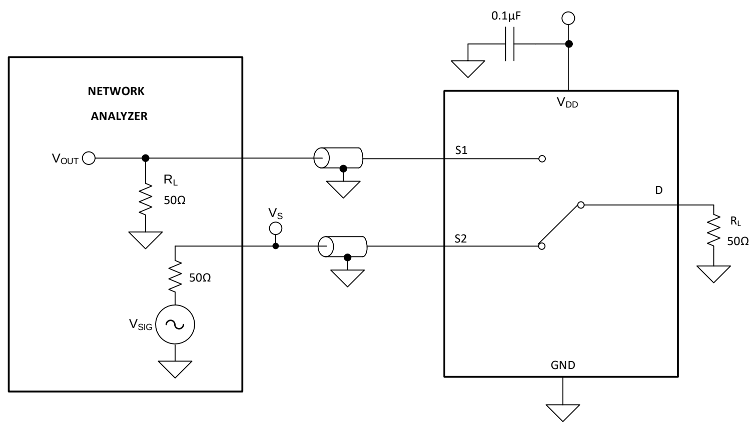


Figure 14. Crosstalk Measurement Setup

$$\text{Channel-to-Channel Crosstalk} = 20 \cdot \text{Log}\left(\frac{V_{OUT}}{V_S}\right) \quad (2)$$

7.9 Bandwidth

Bandwidth is defined as the range of frequencies that are attenuated by less than 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the drain pin (D) of the device. Figure 15 shows the setup used to measure bandwidth.

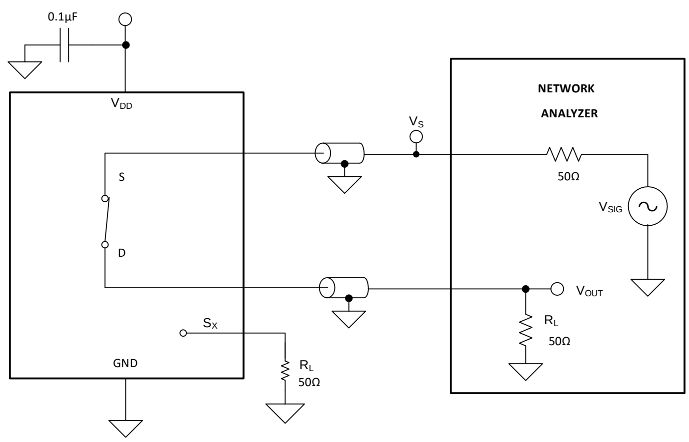


Figure 15. Bandwidth Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX1247 is an 2:1 (SPDT), 1-channel switch where the input is controlled with a single select (SEL) control pin.

8.2 Functional Block Diagram

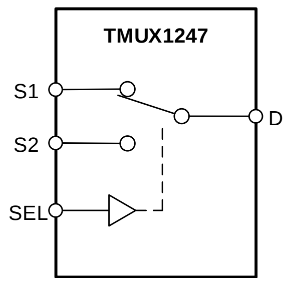


Figure 16. TMUX1247 Functional Block Diagram

8.3 Feature Description

8.3.1 Bidirectional Operation

The TMUX1247 conducts equally well from source (Sx) to drain (D) or from drain (D) to source (Sx). The device has very similar characteristics in both directions and supports both analog and digital signals.

8.3.2 Rail to Rail Operation

The valid signal path input/output voltage for TMUX1247 ranges from GND to V_{DD}.

8.3.3 1.8 V Logic Compatible Inputs

The TMUX1247 has 1.8-V logic compatible control for the logic control input (SEL). The logic input threshold scales with supply but still provides 1.8-V logic control when operating at 5.5 V supply voltage. 1.8-V logic level inputs allow the TMUX1247 to interface with processors that have lower logic I/O rails and eliminates the need for an external translator, which saves both space and BOM cost. For more information on 1.8 V logic implementations refer to *Simplifying Design with 1.8 V logic Muxes and Switches*

8.3.4 Fail-Safe Logic

The TMUX1247 supports Fail-Safe Logic on the control input pin (SEL) allowing for operation up to 5.5 V, regardless of the state of the supply pin. This feature allows voltages on the control pin to be applied before the supply pin, protecting the device from potential damage. Fail-Safe Logic minimizes system complexity by removing the need for power supply sequencing on the logic control pins. For example, the Fail-Safe Logic feature allows the select pin of the TMUX1247 to be ramped to 5.5 V while V_{DD} = 0 V. Additionally, the feature enables operation of the TMUX1247 with V_{DD} = 1.2 V while allowing the select pin to interface with a logic level of another device up to 5.5 V.

8.4 Device Functional Modes

The select (SEL) pin of the TMUX1247 controls which switch is connected to the drain of the device. When a given input is not selected, that source pin is in high impedance mode (HI-Z). The control pins can be as high as 5.5 V.

The TMUX1247 can be operated without any external components except for the supply decoupling capacitors. Unused logic control pins should be tied to GND or V_{DD} in order to ensure the device does not consume additional current as highlighted in *Implications of Slow or Floating CMOS Inputs*. Unused signal path inputs (Sx or D) should be connected to GND.

8.5 Truth Tables

Table 1. TMUX1247 Truth Table

CONTROL LOGIC (SEL)	Selected Source (Sx) Connected To Drain (D) Pin
0	S1
1	S2

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX12xx family offers good system performance across a wide operating supply (1.08V to 5.5V). These devices include 1.8V logic compatible control input pins that enable operation in systems with 1.8V I/O rails. Additionally, the control input pin supports Fail-Safe Logic which allows for operation up to 5.5V, regardless of the state of the supply pin. This protection stops the logic pins from back-powering the supply rail. These features of the TMUX12xx, a family of general purpose multiplexers and switches, reduce system complexity, board size, and overall system cost.

9.2 Typical Application

9.2.1 Input Control for Power Amplifier

One application of the TMUX1247 is for input control of a power amplifier. Utilizing a switch allows a system to control when the DAC is connected to the power amplifier, and can stop biasing the power amplifier by switching the gate to GND. Figure 17 shows the TMUX1247 configured for control of the power amplifier.

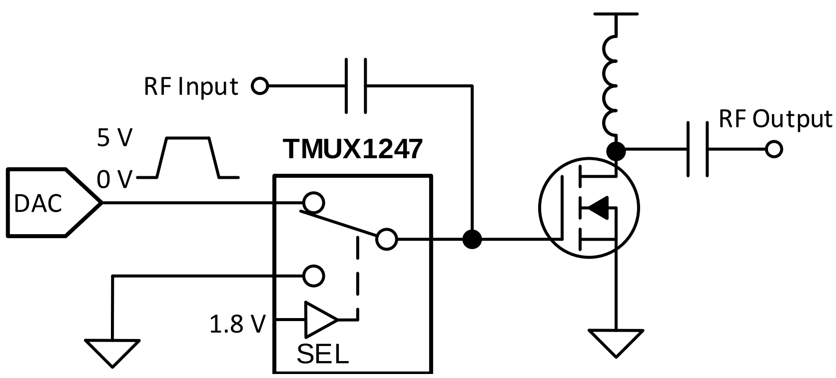


Figure 17. Input Control of Power Amplifier

Typical Application (continued)

9.2.1.1 Design Requirements

This design example uses the parameters listed in Table 3.

Table 2. Design Parameters

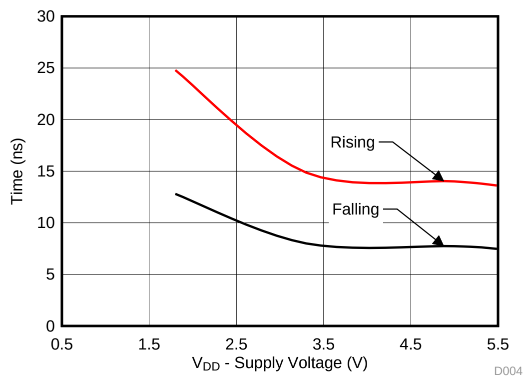
PARAMETERS	VALUES
Supply (V_{DD})	5 V
Mux I/O signal range	0 V to V_{DD} (Rail to Rail)
Control logic thresholds	1.8 V compatible (up to 5.5V)

9.2.1.2 Detailed Design Procedure

The application shown in Figure 17 demonstrates how to toggle between the DAC output and GND for control of a power amplifier using a single control input. The DAC output is utilized to bias the gate of the power amplifier and can be disconnected from the circuit using the select pin of the switch. The TMUX1247 can support 1.8-V logic signals on the control input, allowing the device to interface with low logic controls of an FPGA or MCU. The TMUX1247 can be operated without any external components except for the supply decoupling capacitors. The select pin is recommended to have a weak pull-down or pull-up resistor to ensure the input is in a known state. All inputs to the switch must fall within the recommend operating conditions of the TMUX1247 including signal range and continuous current. For this design with a supply of 5 V the signal range can be 0 V to 5 V and the max continuous current can be 30 mA.

9.2.1.3 Application Curve

A key parameter for this application is the transition time of the device. Faster transition time allows the system to toggle between input sources at a faster rate and allows the output to settle to the final value. The TMUX1247 has a transition time that varies with supply voltage and is shown in Figure 18



T_A = 25°C

Figure 18. $T_{transition}$ vs Supply Voltage

9.2.2 Switchable Operational Amplifier Gain Setting

Another example application of the TMUX1247 is to change an Op Amp from unity gain setting to an inverting amplifier configuration. Utilizing a switch allows a system to have a configurable gain and allows the same architecture to be utilized across the board for various inputs to the system. Figure 19 shows the TMUX1247 configured for gain setting application.

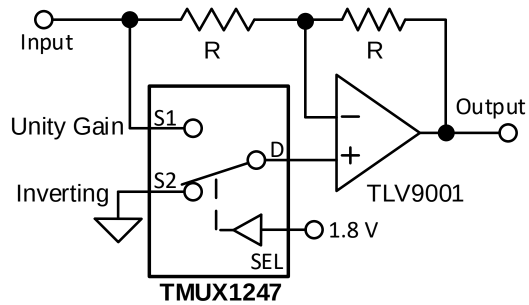


Figure 19. Switchable Op Amp Gain Setting

9.2.2.1 Design Requirements

This design example uses the parameters listed in Table 3.

Table 3. Design Parameters

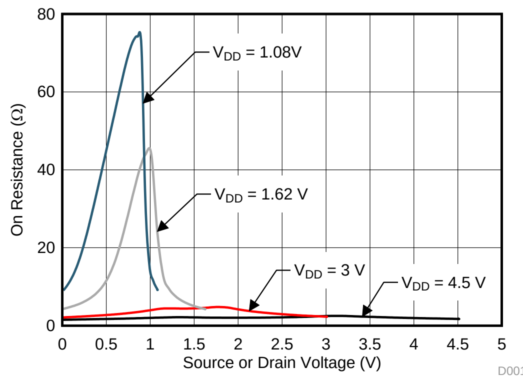
PARAMETERS	VALUES
Input Signal	0 V to 2.75 V
Mux Supply (V_{DD})	2.75 V
Op Amp Supply (V_+/ V_-)	±2.75 V
Mux I/O signal range	0 V to V_{DD} (Rail to Rail)
Control logic thresholds	1.8 V compatible (up to 5.5V)

9.2.2.2 Detailed Design Procedure

The application shown in Figure 19 demonstrates how to use a single control input and toggle between gain settings of -1 and +1. If switching between inverting and unity gain is not required, the TMUX1247 can be utilized in the feedback path to select different feedback resistors and provide scalable gain settings for configurable signal conditioning.

The TMUX1247 can be operated without any external components except for the supply decoupling capacitors. The select pin is recommended to have a weak pull-down or pull-up resistor to ensure the input is in a known state. All inputs to the switch must fall within the recommend operating conditions of the TMUX1247 including signal range and continuous current. For this design with a supply of 2.75 V the signal range can be 0 V to 2.75 V and the max continuous current can be 30 mA.

9.2.2.3 Application Curve



T_A = 25°C

Figure 20. On-Resistance vs Source or Drain Voltage

10 Power Supply Recommendations

The TMUX1247 operates across a wide supply range of 1.08 V to 5.5 V. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings can cause permanent damage to the devices.

Power-supply bypassing improves noise margin and prevents switching noise propagation from the V_{DD} supply to other components. Good power-supply decoupling is important to achieve optimum performance. For improved supply noise immunity, use a supply decoupling capacitor ranging from 0.1 µF to 10 µF from V_{DD} to ground. Place the bypass capacitors as close to the power supply pins of the device as possible using low-impedance connections. TI recommends using multi-layer ceramic chip capacitors (MLCCs) that offer low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling purposes. For very sensitive systems, or for systems in harsh noise environments, avoiding the use of vias for connecting the capacitors to the device pins may offer superior noise immunity. The use of multiple vias in parallel lowers the overall inductance and is beneficial for connections to ground planes.

11 Layout

11.1 Layout Guidelines

11.1.1 Layout Information

When a PCB trace turns a corner at a 90° angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self–inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. Figure 21 shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

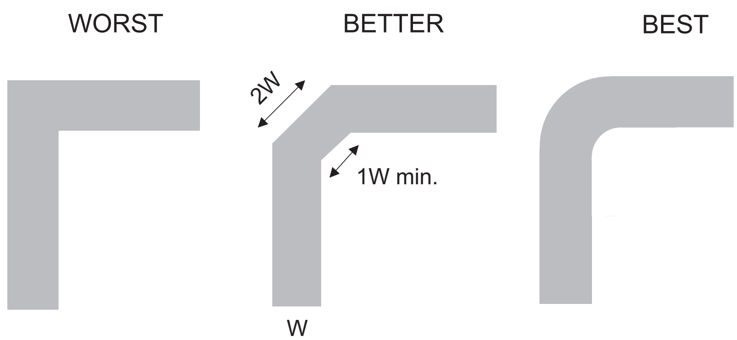


Figure 21. Trace Example

Route high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points, through-hole pins are not recommended at high frequencies.

Figure 22 illustrates an example of a PCB layout with the TMUX1247. Some key considerations are:

- Decouple the V_{DD} pin with a 0.1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the V_{DD} supply.
- Keep the input lines as short as possible.
- Use a solid ground plane to help reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

11.2 Layout Example

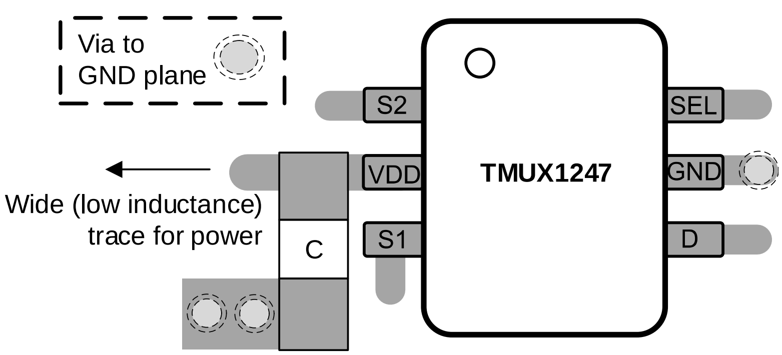


Figure 22. TMUX1247 Layout Example

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

Texas Instruments, *Improve Stability Issues with Low CON Multiplexers*.

Texas Instruments, *Simplifying Design with 1.8 V logic Muxes and Switches*.

Texas Instruments, *Eliminate Power Sequencing with Powered-off Protection Signal Switches*.

Texas Instruments, *System-Level Protection for High-Voltage Analog Multiplexers*.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks

E2E is a trademark of Texas Instruments.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMUX1247DCKR	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	247
TMUX1247DCKR.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	247
TMUX1247DCKRG4	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	247
TMUX1247DCKRG4.A	Active	Production	SC70 (DCK) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	247

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

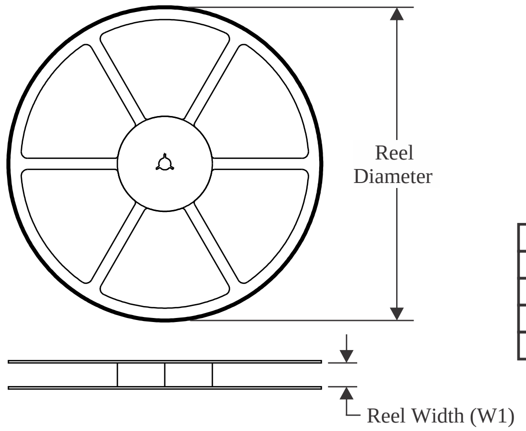
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

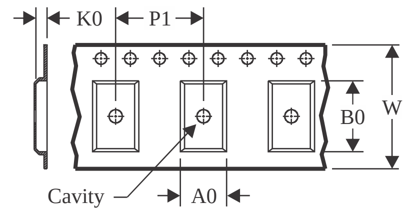
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

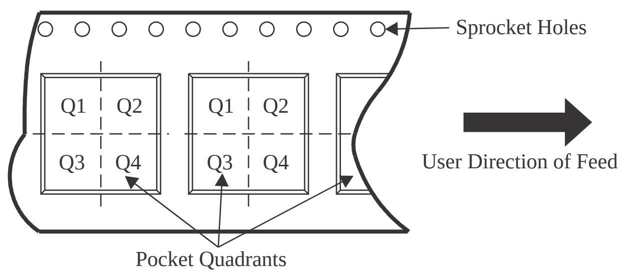


TAPE DIMENSIONS



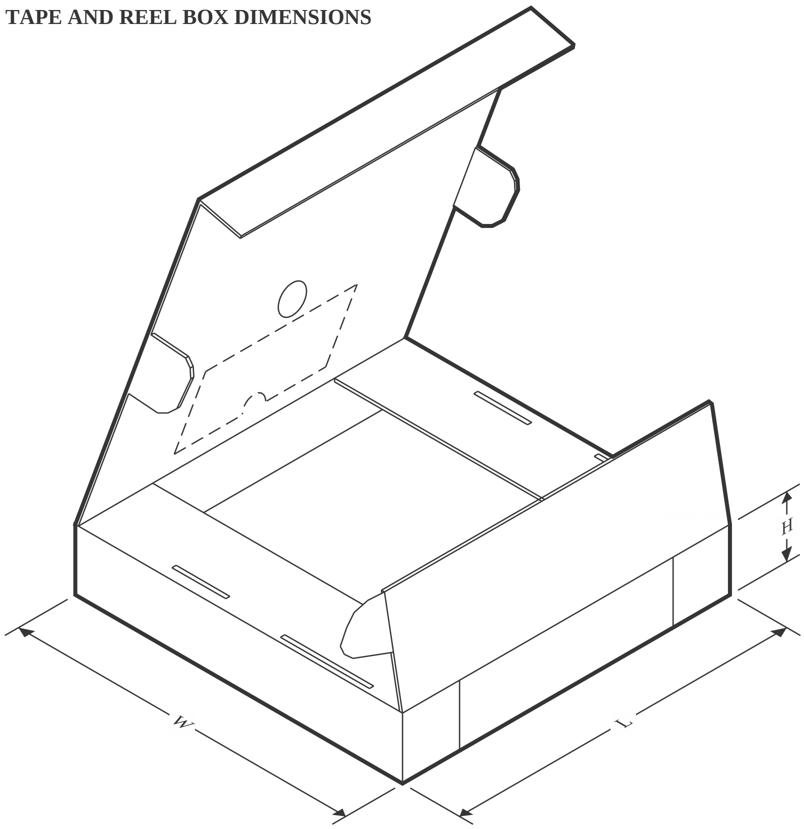
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



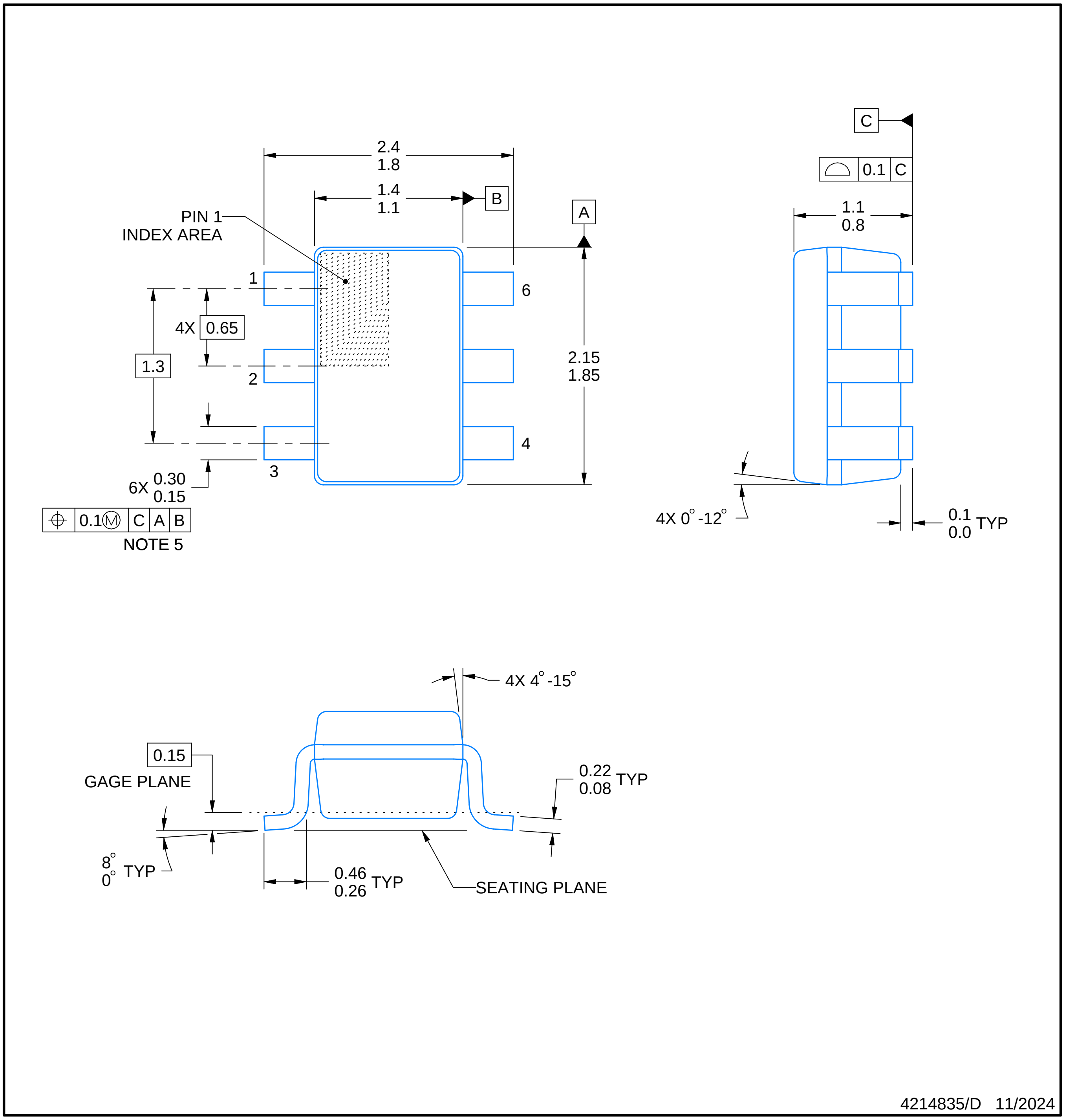
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX1247DCKR	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TMUX1247DCKRG4	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3



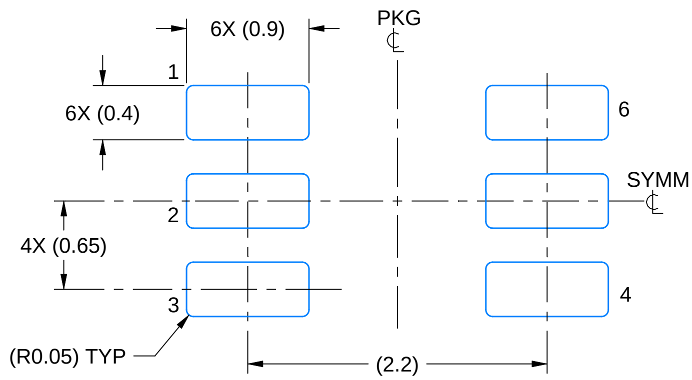
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX1247DCKR	SC70	DCK	6	3000	180.0	180.0	18.0
TMUX1247DCKRG4	SC70	DCK	6	3000	180.0	180.0	18.0

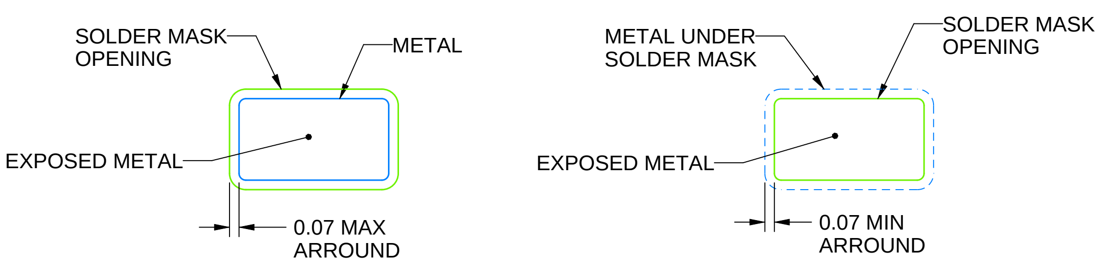


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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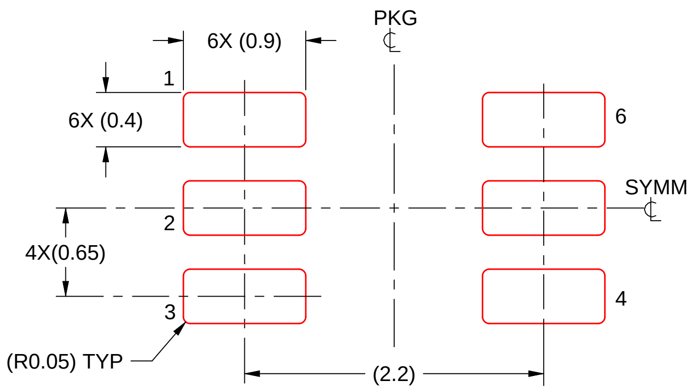
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.