4.1-40V 100-mΩ Single-Channel Smart High-Side Switch

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1: -40°C to 125°C Ambient Operating Temperature Range
- Quad-Channel 100-mΩ Smart High-Side Switch With Full Diagnostics
  - A Version: Open-Drain Digital Output
  - B Version: Current Sense Analog Output
- Wide Operating Voltage: 4.1 V to 40 V
- High accurate current sense: ±15mA @ 500mA, ±3.75mA @ 25mA with B Version
- Adjustable current limit: ±25% when > 250mA, ±20% when > 500mA
- Protection:
  - Short-to-GND Protection by Current Limit (Internal or External)
  - Thermal Shutdown With Latch-Off Option and Thermal Swing
  - Inductive Load Negative Voltage Clamp with Optimized Slew Rate
  - Loss-of-GND and Loss-of-Battery Protection
- Diagnostic:
  - Overcurrent and Short-to-Ground Detection
  - Open Load / Short to Battery Detection During On and Off State
  - Global Fault Report for Fast Hardware Interrupt
- Available in an ESOP-14 Package

APPLICATIONS

- High-Side Relay Drivers
- Power Switch for Sub-Module Power Supply
- Low Wattage Lamp Power Switch
- General Resistive, Inductive, and Capacitive Loads

DESCRIPTION

The SCT41100Q device is fully protected single-channel smart high-side switch with four integrated

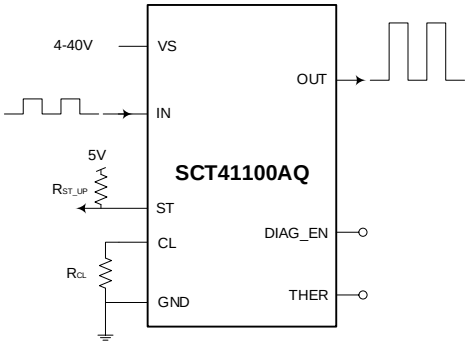
For version A, the device implements the digital fault report with an open-drain structure, Quad channel synchronous setting of current limit value.

For version B, the device achieves high-precision current detection, making diagnosis more accurate, Quad channel synchronous setting of current limit value.

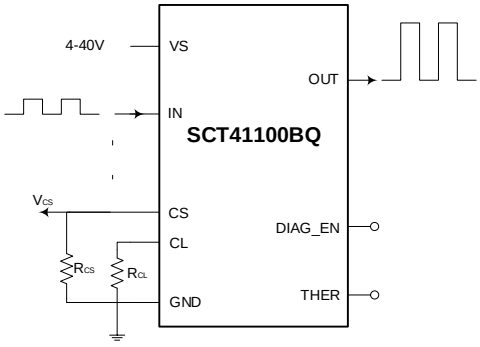
The SCT41100Q provides current limit, thermal shutdown protection. Full diagnostics and high-accuracy current sense enable intelligent control of the load. The device is available in a 28-pin EMSOP-28 package.

代理商 威汉迈 www.wsvie.com 联系电话 138 2526 3270

TYPICAL APPLICATION



Typical Application of Version A



Typical Application of Version B

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REVISION HISTORY

Revision 0.8: Customer Sample

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DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
SCT41100AQMZER	100AQ	ESOP-14
SCT41100BQMZER	100BQ	ESOP-14

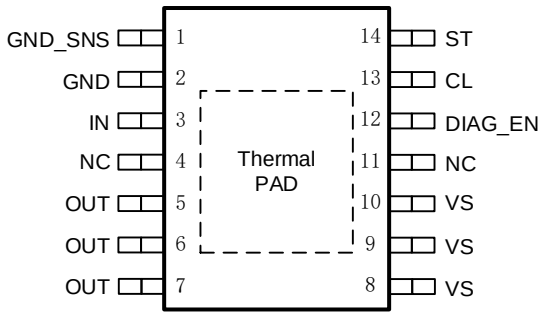
1) For Tape & Reel, Add Suffix R (e.g. SCT41100AQMZER&41100BQMZER)

ABSOLUTE MAXIMUM RATINGS

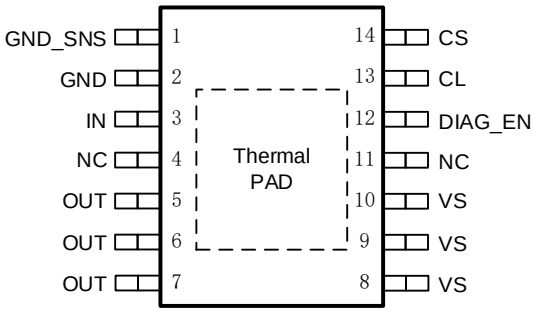
Over operating free-air temperature unless otherwise noted(1)

DESCRIPTION	MIN	MAX	UNIT
VS (t < 400 mS)	-0.3	43	V
OUT (t < 400 mS)	-0.3	43	V
Reverse polarity voltage(2)	-18		V
Current on GND (t < 2 minutes)	-250	20	mA
Voltage on IN, DIAG_EN	-0.3	5.5	V
Current on IN, DIAG_EN	-10		mA
Voltage on ST	-0.3	5.5	V
Current on ST	-30	10	mA
Voltage on CS	--2.7	5.5	V
Current on CS		30	mA
Voltage on CL	-0.3	5.5	V
Current on CL		6	mA
Inductive load switch-off energy dissipation, single pulse, single channel		70	mJ
Operating ambient temperature	-40	125	°C
Operating Junction temperature(3)	-40	150	°C
Storage temperature T_{STG}	-65	150	°C

PIN CONFIGURATION



Top View: Version A ESOP-14



Top View: Version B ESOP-14

(1) Stresses beyond those listed under Absolute Maximum Rating may cause device permanent damage. The device is not guaranteed to function outside of its Recommended Operation Conditions.
(2) Reverse polarity condition: t < 60 s, reverse current < Irev1, GND pin 1-kΩ resistor in parallel with diode
(3) The IC includes thermal shutdown protection to protect the device during overload conditions. Junction temperature will exceed 170°C when thermal shutdown protection is active. Continuous operation above the specified maximum operating junction temperature will reduce lifetime.

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PIN FUNCTIONS

NAME	NO.		I/O(1)	PIN FUNCTION
	A Version	B Version		
GND_SNS	1	1	I	External ground sense.
GND	2	2	G	IC ground pin.
IN	3	3	I	logic input, internal pulldown.
NC	4,11	4,11	-	Not Connection.
OUT	5,6,7	5,6,7	O	Output of high side-switch, connected to the load.
VS	8,9,10	8,9,10	I	Power supply; battery voltage.
DIAG_EN	12	12	I	Enable-disable pin for diagnostics; internal pulldown.
CL	13	13	I	Adjustable current limits.
ST	14	-	O	Open-drain diagnostic status output, external pull-up voltage required.
CS	-	14	O	Current-sense output

(1) G=Ground, I=Input, O=Output

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RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range unless otherwise noted

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{VS}	Input voltage range	4.1	40	V
IN, DIAG_EN	External pull-up voltage range	0	5	V
ST	External pull-up voltage range	0	5	V
Nominal dc load current		0	4	A
T_J	Operating junction temperature	-40	150	°C

ESD RATINGS

PARAMETER	DEFINITION	MIN	MAX	UNIT
V_{ESD}	Human Body Model(HBM), per ANSI-JEDEC-JS-001-2014 specification, all pins(1)	TBD	TBD	kV
	Charged Device Model(CDM), per ANSI-JEDEC-JS-002-2014 specification, all pins(2)	TBD	TBD	kV

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

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THERMAL INFORMATION

PARAMETER	THERMAL METRIC	ESOP-14	UNIT
$R_{\theta JA}$	Junction to ambient thermal resistance(1)	35.85	°C/W
$R_{\theta JC\ (top)}$	Junction to case (top) thermal resistance(1)	48.58	
$R_{\theta JC\ (bot)}$	Junction to case (bottom) thermal resistance(1)	5.72	
$R_{\theta JB}$	Junction to board thermal resistance(1)	16.16	
$R_{\psi JT}$	Junction-to-top characterization parameter	4.49	

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT41100Q is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT41100Q. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

ELECTRICAL CHARACTERISTICS

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 150°C junction temperature range unless otherwise stated. VS = 13.5 V, IN = 5 V unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply						
V_{VS}	Operating input		5		40	V
V_{VS_UVLO}	Input UVLO Threshold	V_{VS} rising		3.8	4	V
	Hysteresis			550		mV
I_{Q_OP}	Operating input current	DIAG_EN=5V,I_{OUT}=0.5A, Current limit=5A		2.3		mA
		DIAG_EN=5V,I_{OUT}=0A, Current limit=5A				
I_{OFF}	Standby current	IN=DIAG_EN=0V, CL=CS=Floating			0.3	uA
		IN=DIAG_EN= 0V, CL=CS=Floating,TJ=125°C			3	uA
$I_{OFF(DIAG)}$	Standby current with diagnostic enabled	IN=0V,DIAG_EN=5V, VS-OUT>V_{OL_OFF}		1	5	mA
$t_{OFF(DIAG)}$	Standby mode deglitch time	IN from high to low, if deglitch time >$T_{OFF(DIAG)}$, the device enters into standby mode.		9		mS
I_{LKG_OUT}	Output leakage current in off-state	IN=DIAG_EN=OUT=0V			3	uA
Power Stage						
R_{DSON}	On-state resistance			75		mΩ
VF	Drain−source diode voltage	IN=0V，IOUT = −0.1 A		0.7		
$I_{CL(INT)}$	Internal current limit	Internal current limit value, CL pin connected to GND	7		14	A
$I_{CL(TSD)}$	Current limit during thermal shutdown	Internal current limit value under thermal shutdown		7.5		A
		External current limit value under thermal shutdown. The percentage of the external current limit setting value		60%		
$V_{DS(clamp)}$	Drain-to-source internal clamp voltage			47V		V

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Logic Input(IN,DIAG_EN)						
V_{IH}	Logic high-level voltage			1.1	1.3	V
V_{IL}	Logic low-level voltage		0.6	0.95		V
$R_{L\_PG\_IN}$	IN-pin pulldown resistor			480		kΩ
$R_{L\_PG\_DIAG}$	DIAG_EN-pin pulldown resistor			480		kΩ
Diagnostics						
I_{LKG_GL}	Output leakage current under GND loss condition			14	100	uA
V_{OL_OFF}	Open-load detection threshold	IN = 0 V, when $V_{VS} - V_{OUTx} < V_{OL\_OFF}$, duration longer than t(ol,off), then open load is detected, off state	1.3	1.8	2.3	V
t_{DOL_OFF}	Open-load detection threshold deglitch time in off-state			30		uS
I_{OL_OFF}	Off-state output sink current	IN=0V,DIAG_EN=5V, $V_{OUT}=V_{VS}$		43		uA
I_{OL_ON}	Open-load detection threshold in on state	IN=5V, when IOUT < I_{OL_ON}, duration longer than I_{OL_ON}. Open load detected. Version A only		5		mA
t_{DOL_ON}	Open-load detection threshold deglitch time in on-state			700		uS
V_{ST}	Status low-output voltage	IST = 2 mA, version A only		0.3		V
t_{CL_DEG}	Deglitch time when current limit occurs	IN= DIAG_EN = 5V, the deglitch time from current limit toggling to ST, CS report.			45	uS
T_{SD}	Thermal shutdown threshold			175		℃
T_{SD_RST}	Thermal shutdown status reset threshold			155		℃
T_{SW}	Thermal swing shutdown threshold			40		℃
T_{HYS}	Hysteresis for resetting the thermal shutdown or thermal swing			10		℃
Current Limit						
K_{CL}	Current-limit ratio			4000		
V_{CL}	Current limit internal threshold			1.233		V
$\Delta K_{CL}/ K_{CL}$	External current limit accuracy	I_{Limit} ≥0.25A 0.5A ≤ I_{Limit} ≤ 7A	30 15		30 15	%
Current Sense (Version B)						
K_{CS}	Current-sense ratio			1000		
$\Delta K_{CS}/ K_{CS}$		I_{OUTx} ≥ 50mA I_{OUTx} ≥ 100mA I_{OUTx} ≥ 500mA	-30 -20 -15		30 20 15	
V_{CS_LIN}	Current-sense voltage linear range	V_{VS} ≥ 6.5V 5V ≤ V_{VS} < 6.5V	0 0		4 V_{VS} -2.5	V
I_{OUT_LIN}	Output-current linear range		0		4	A
V_{CS_H}	Current sense pin output voltage	Fault mode	4.3		5	V

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I_{CS_H}	Current-sense pin output current	V_{CS} =4.3V	10	14.5		mA
I_{CS_LKG}	Current-sense leakage current in disabled mode	DIAG_EN=0V,TJ=125°C			0.5	uA
Switching						
t_{D_ON}	Input to output propagation delay, Rising	DIAG_EN=5V, I_{OUT} =0.5A, IN rising edge to 10% of V_{OUT}		30		uS
t_{D_OFF}	Input to output propagation delay, Falling	DIAG_EN=5V, I_{OUT} =0.5A, IN falling edge to 90% of V_{OUT}		60		uS
$\Delta V/\Delta t_{\_ON}$	Turnon slew rate	DIAG_EN=5V, I_{OUT} =0.5A, V_{OUT} from 10% to 90%		0.4		V/uS
$\Delta V/\Delta t_{\_OFF}$	Turnoff slew rate	DIAG_EN=5V, I_{OUT} =0.5A, V_{OUT} from 90% to 10%		0.4		V/uS
Current Sense timing						
$t_{CS\_ON(EN)}$	CS settling time from DIAG_EN disabled	I_{OUT} =0.5A, DIAG_EN rising edge to V_{CS} rising		2	15	uS
$t_{CS\_OFF(EN)}$	CS settling time from DIAG_EN enabled	I_{OUT} =0.5A, DIAG_EN falling edge to V_{CS} falling		1	15	uS
$t_{CS\_ON(IN)}$	CS settling time from IN rising edge	DIAG_EN=5V, I_{OUT} =0.5A, IN rising edge to V_{CS} rising		60		uS
$t_{CS\_OFF(IN)}$	CS settling time from IN falling edge	DIAG_EN=5V, I_{OUT} =0.5A, IN rising edge to V_{CS} rising		5		uS
t_{CS_CL}	CS settling time from Current limit	DIAG_EN=5V, IN=5V,OUT=0V, Current limit to V_{CS_H}			45	uS

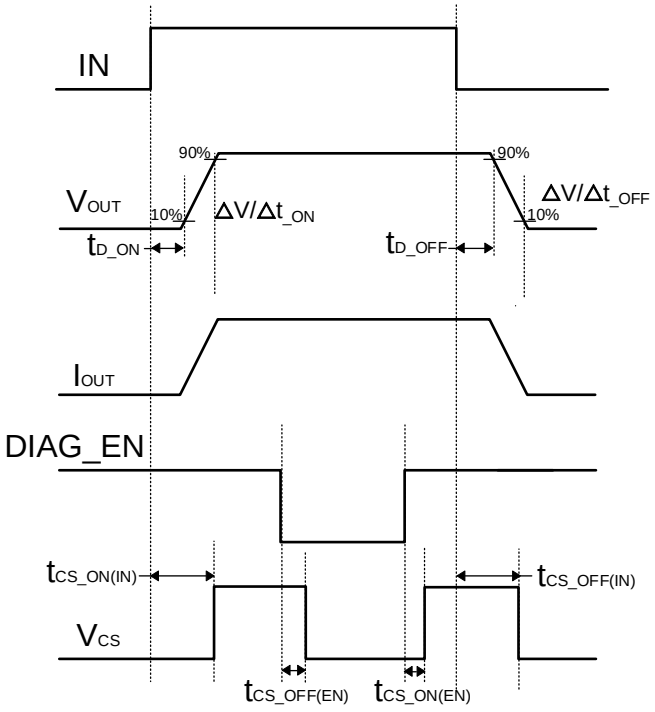

Figure 1. Output And CS Delay Sequential

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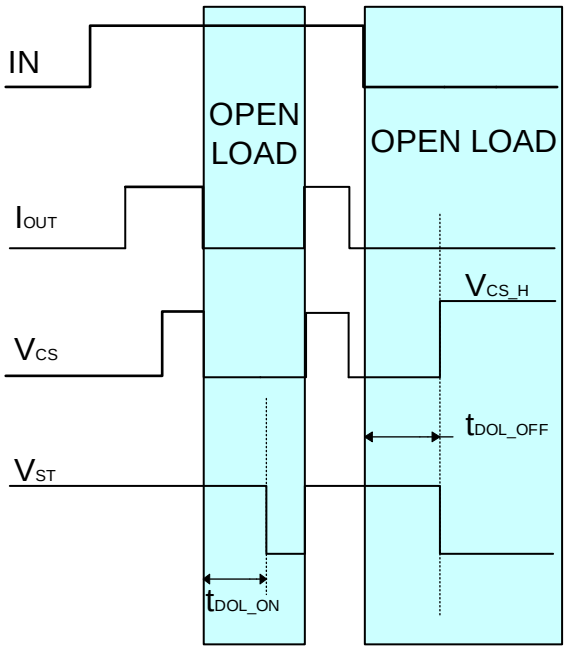

Figure 2. Open Load Delay

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TYPICAL CHARACTERISTICS

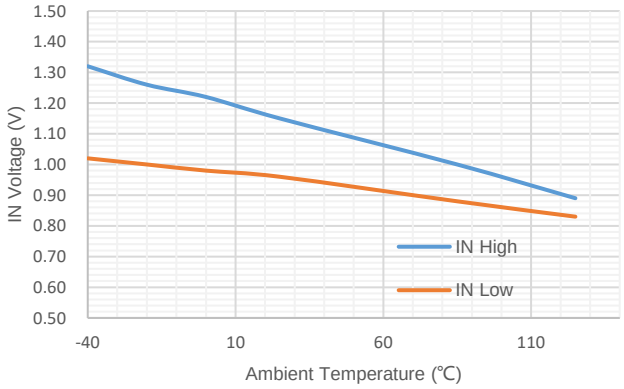

Figure 3. IN Threshold VS Temperature

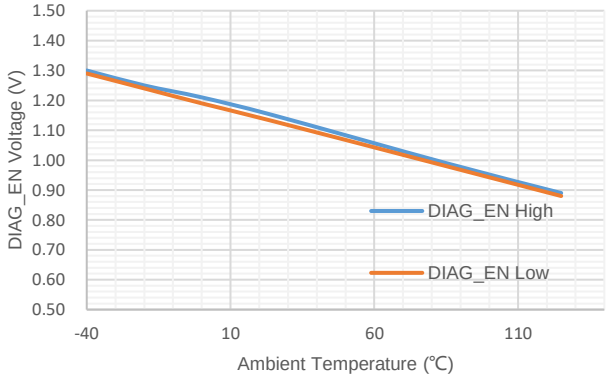

Figure 4. DIAG_EN Threshold VS Temperature

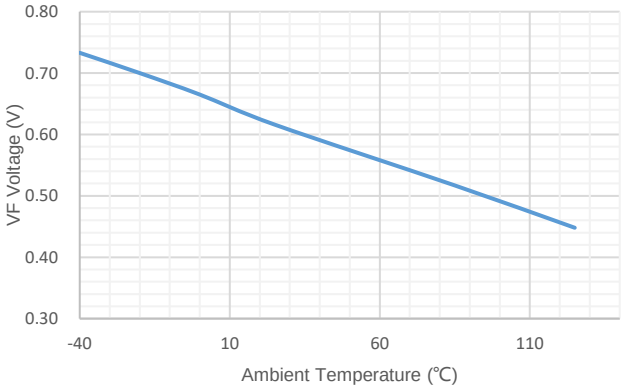

Figure 5. Body-Diode Forward Voltage VS Temperature

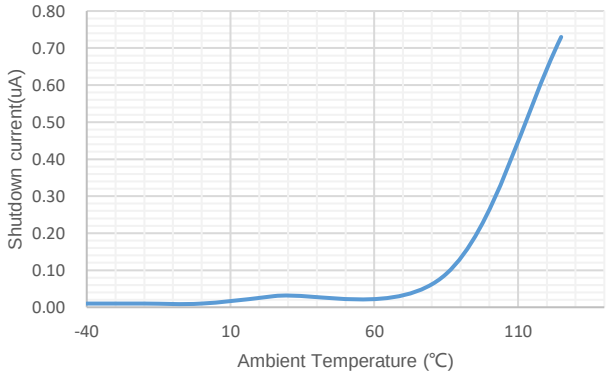

Figure 6. $I_{SHUTDOWN}$ vs Input Voltage

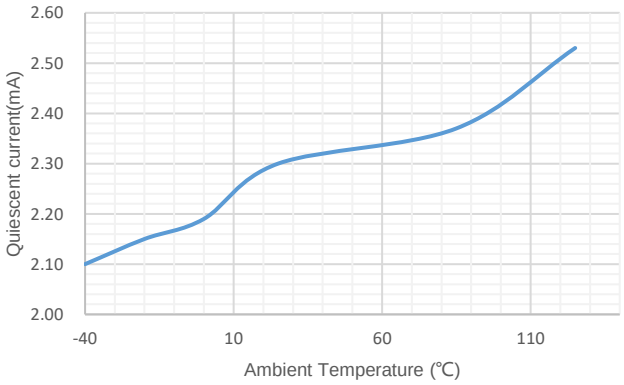

Figure 7. I_Q vs Input Voltage

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FUNCTIONAL BLOCK DIAGRAM

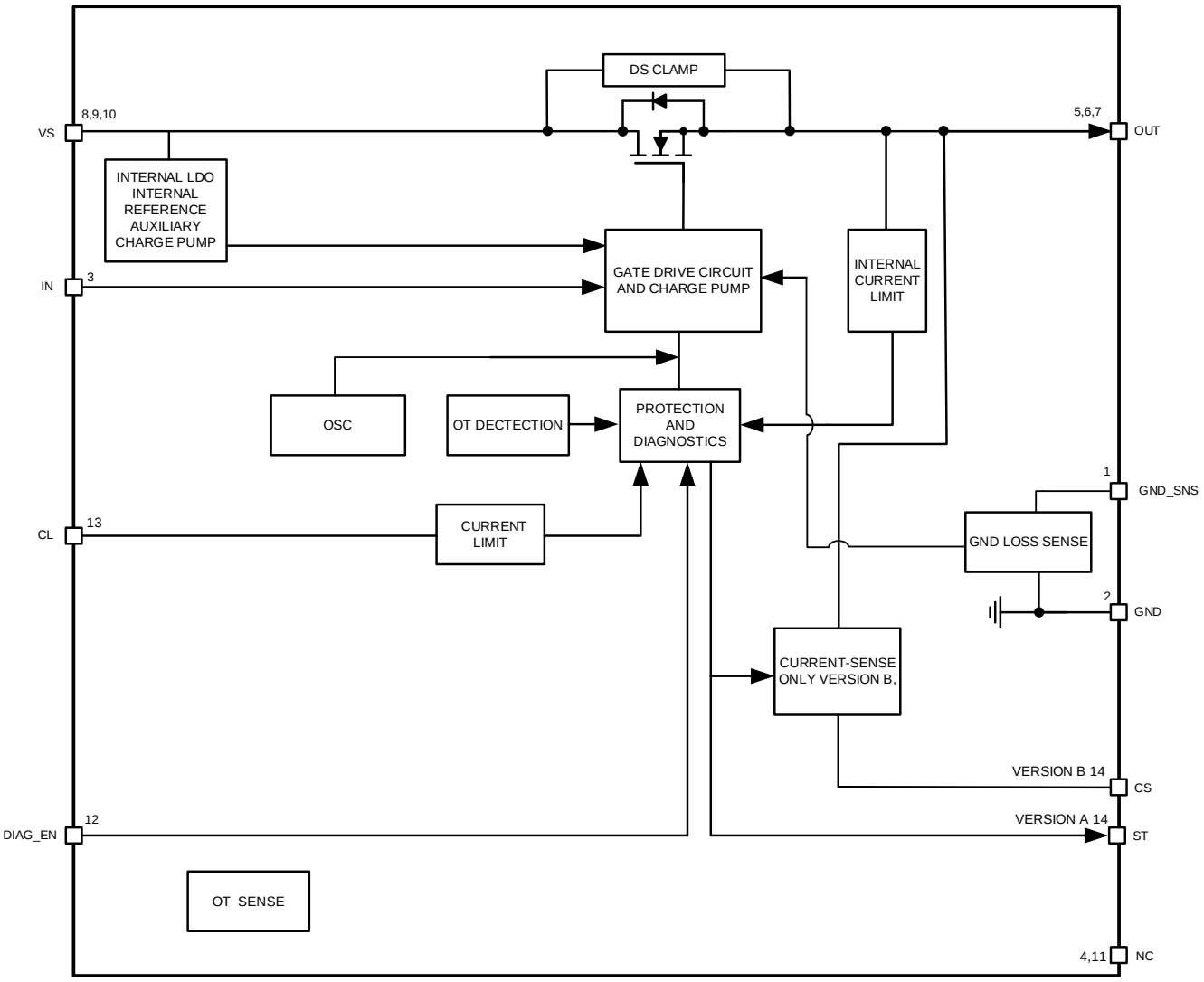

Figure 8. Functional Block Diagram

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OPERATION

Overview

SCT41100Q is a single-channel intelligent high-side switch that internally integrates a charge pump and power N-MOSFETs. SCT41100Q offers external adjustable threshold overcurrent protection functionality, with a typical value of 14A for internal current limiting to enhance design flexibility and system reliability. This device features comprehensive diagnostic functions and high-precision current sensing functions to achieve smart control of the load. Among SCT41100Q's two versions, Version A includes an open-drain digital output diagnostic mode. Version B provides current sensing analog output.

In Version A, an open-drain digital output is utilized, and the diagnostic output pin ST needs to be pulled down to the ground externally by providing a pull-up voltage of 3.3V or 5V to match the MCU. The abnormal status of each channel in version A can be reported separately to help the system quickly locate problematic channels.

Version B has a current sensing analog output, enabling the system to accurately determine the operational status of channel. The integrated current mirror of the device provides a mirror current of 1/KCS load current, which flows through the CS resistor and becomes a voltage signal to achieve analog output of load current.

SCT41100Q has a clamping function between the drain and source electrodes, which can effectively protect itself under inductive load conditions.

SCT41100Q is an intelligent high-side switch suitable for applications where resistance, capacitance, and inductance loads can support most small load currents.

Adjustable Current Limit

SCT41100Q has an adjustable high-precision current limitation mechanism. When the load current reaches the designated threshold, it rapidly internally controls the N-MOSFET gate voltage to clamp the output current to the set value and report faults. When overcurrent occurs, there is high power dissipation in the device. If the device heats up and triggers thermal shutdown, the current limit will be reduced to $I_{CL\ (TSD)}$ to reduce power dissipation on the device and further protect the device.

SCT41100Q has two overcurrent protection thresholds, internal and external.

Internal current limitation, SCT41100Q has a conventional value of 14A for internal integrated current limitation. When the CL pin is connected to the IC GND, the external current limitation becomes inactive, and protection is solely managed by the internal current limitation. This configuration is generally suitable for applications involving low VS voltage transient high current instances. At this point, there is a certain application risk when VS is under high voltage.

External adjustable current limit, SCT41100Q can set the current limit threshold through an external R_{CL} resistor, which needs to be connected between CL and IC GND. Use Equation 1 to calculate the RCL resistance:

$$R_{CL} = \frac{V_{CL} \times K_{CL}}{I_{Limit}} \quad (1)$$

Where

- V_{CL} is an internal reference value with a typical value of 1.233V
- K_{CL} is a typical value of 4000 for the load current sampling ratio

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Accurate Current Sense

Version B have high-precision current detection functions, which can accurately detect the real-time status of each channel, making it convenient for the system to accurately diagnose the status of each channel. Version B internally integrate a current mirror to mirror the load current. The ratio between the load current and the mirror current is KCS: 1, and the mirror current flows through the CS pin and an external ground resistor RCS, generating a voltage signal to achieve load current detection. Refer to Formula (2) for RCS calculation:

$$R_{CS} = \frac{V_{CS} \times K_{CS}}{I_{OUTx\_MAX}} \quad (2)$$

Where

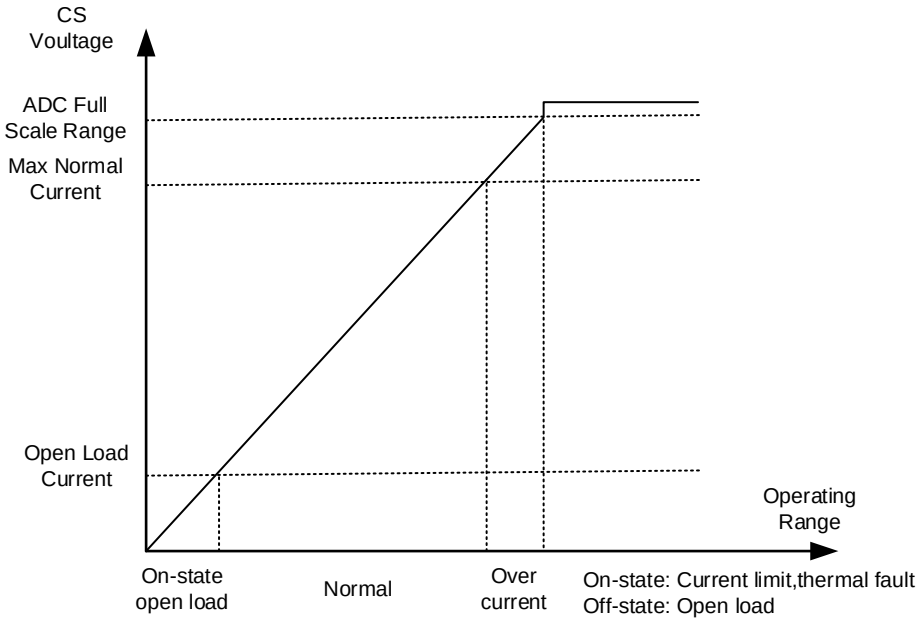
- V_{CS} is the voltage value corresponding to the maximum load current, the values should refer in the EC table to V_{CS_LIN} range
- K_{CS} stands for the load current sampling mirror ratio, typically set to 1000.
- I_{OUT_MAX} represents the maximum load current value for the current channel.

When the system malfunctions, CS will pull up to V_{CS_H} cooperates for fault detection. At this point, in order to make the fault detection judgment effective, there are limitations in equation (3) for the R_{CS}:

$$R_{CS} \geq \frac{V_{CS\_H(MIN)}}{I_{CS\_H(MIN)}} \quad (3)$$

Where

- $V_{CS\_H\ (MIN)}$ is the minimum value of VCS
- $I_{CS\_H\ (MIN)}$ is the minimum value of ICS



- Figure 9.Voltage Indication on the CS Pin

Diagnostic Enable Function

Through DIAG_ EN pin can set the device to enable or disable diagnostic functions. The diagnostic function is enabled when the DIAG_EN is high, and disabled when the DIAG_EN is low. When the diagnostic function is disabled, it will reduce the standby power consumption of the device.

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Diagnostics Reporting

Version A,ST pins for fault reporting. Pulling down the internal ST device to GND, requires the external pull-up, with conventional values of 3.3V and 5V. When a channel malfunctions, the corresponding ST pin will be pulled down to GND, so that the system can quickly detect the faulty channel.

Version B, Diagnose anomalies by checking if the CS pin voltage is VCS_ H .
The fault report is shown in Table 2:

Table 2. Fault Table

Conditions	INx	OUTx	Criterion	STx	CS
Normal	L	L	-	H	0
	H	H	-	H	In linear region
Overlaod, short to ground	H	L	Current limit triggered	L	V_{CS_H}
Open load, short to battery, reverse polarity	H	H	Version A: Output current < I_{OL_ON}	L	Almost 0
	L	H	$V_{VS} – V_{OUT} < V_{OL\_OFF}$	L	V_{CS_H}
Thermal shutdown	H	-	TSD triggered	L	V_{CS_H}

Open-Load Detection

There are two types of load open circuit detection:

1. When IN is low, the channel is turned off, and due to the open circuit of the load, the OUT voltage cannot decrease rapidly. When the OUT voltage and power supply voltage still meet V_{VS} - V_{OUT}<V_{OL_OFF} after t_{DOL_OFF} , then an open load condition is determined, and ST , CS reports the fault. Due to potential leakage currents and external components, it is generally recommended to use a pull-up resistor between VS and OUT to offset leakage current, ensuring a more accurate open load report. The recommended value for pull-up resistance is 10k.
2. When IN is high, the load current of version A is less than I_{OL_ON}, ST diagnosis takes effect. The high-precision current detection function of version B. When the VCS voltage is detected to be too low, it can be considered that the load is open.

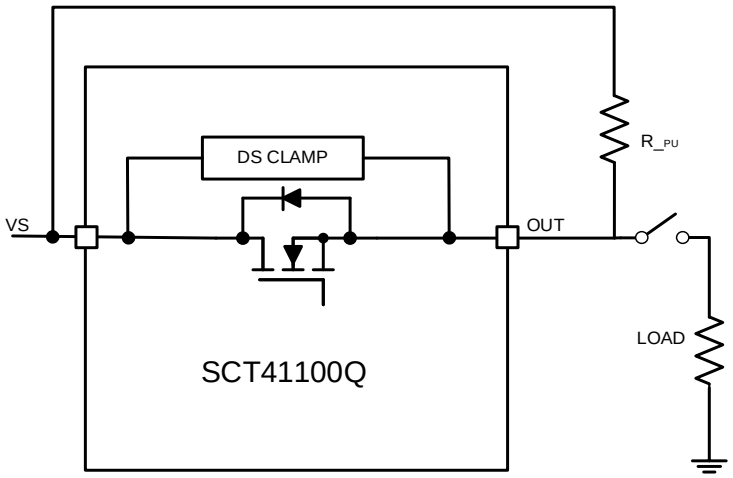

Figure 10. Open-Load Detection

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Loss-of-GND Protection

SCT41100Q features Loss-of-GND protection. By connecting the GND_SNS pin to external ground, in case of a loss of ground, the status is determined by the voltage difference between IC GND and the GND_SNS pin connected to external ground. Regardless of whether IN is high or low, the channels will be deactivated for protection.

Thermal Shutdown

UUnder extreme conditions like overcurrent, the device undergoes substantial power stress and heats up rapidly. SCT41100Q incorporates two types of thermal protection: absolute thermal protection and relative thermal protection. These are designed to prevent rapid overheating of the device without protection.
After triggering the thermal shutdown, when TJ<TSD-THYS, the output will recover, but the current limit threshold will be reduced to 40% of the design value, reducing power stress and enhancing protection. When TJ<TSD_RST or IN pin restart thermal fault signal will be cleared.

Inductive-Load Switching-Off Clamp

When disconnecting the inductive load, the output will be pulled negative due to the influence of the induced electromotive force. At this time, the VS voltage is still positive, and excessive output negative voltage may cause power MOSFET voltage breakdown. To protect the device, the SCT41100Q internally integrates a voltage clamp function, namely $V_{DS\ (clamp)}$. When the output negative voltage is too large, the voltage between V_{VS} and V_{OUT} will be clamped to $V_{DS\ (clamp)}$ to protect the power MOSFET. When the energy of the inductive load is too large, it is recommended to use the method shown in Figure 13 for further protection.

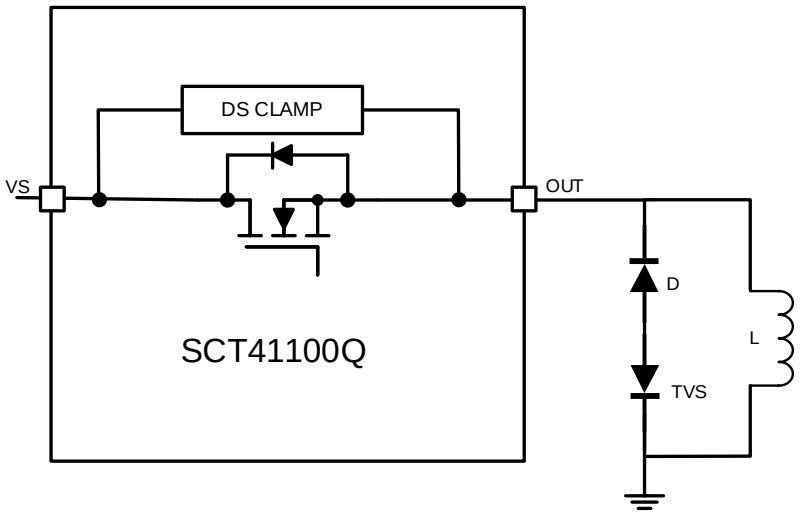

Figure 11. Inductive Load External Protection Circuit

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APPLICATION INFORMATION

Protection for Loss of Power Supply

There is no risk for resistive or capacitive loads when the input power supply suddenly disconnects. However, for inductive loads, sudden changes in inductance current will generate induced electromotive force. It is recommended to add a GND network or external freewheeling diode to prevent excessive energy from damaging the chip. Join GND network GND_SNS cannot be grounded to prevent ground failure error reporting.

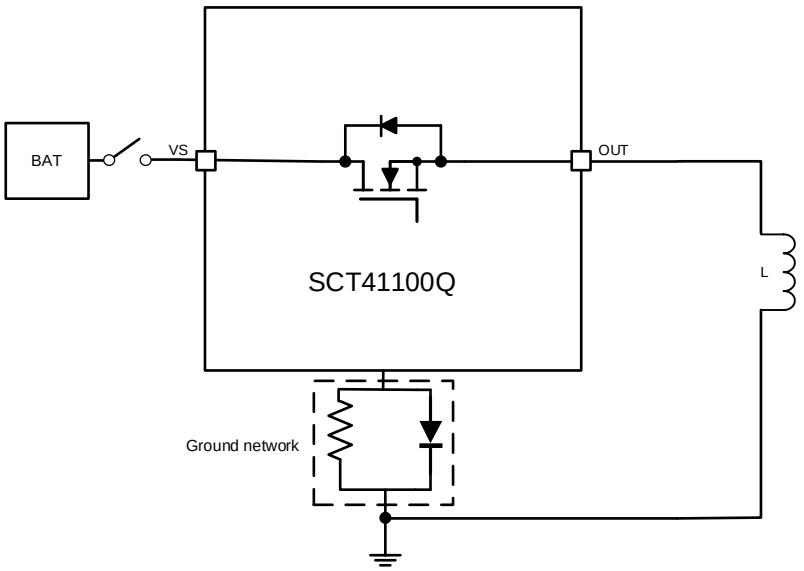

Figure 12. Ground Network Power Loss Protection

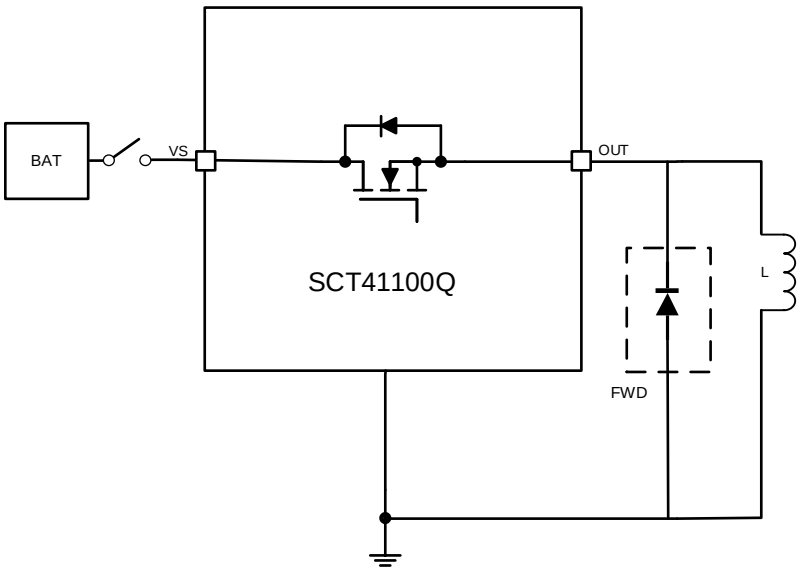

Figure 13. The Freewheeling Diode Power Loss Protection

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Reverse-Current Protection

When there is an input short circuit, the reverse current flows to the input through the body diode, and when the input polarity is reversed, the reverse current flows to the input through GND and the body diode. Since the current-handling capacity of the GND pin is limited, for device protection, it's advisable to include a reverse protection diode at the input or incorporate it into the GND network. When a reverse protection diode is added to the input, both the load and the device are protected.

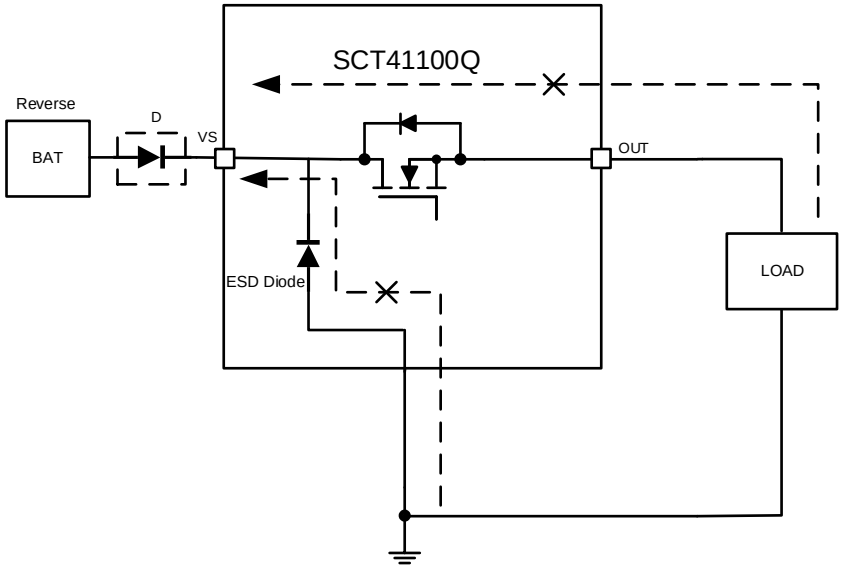

Figure 14. Anti Reverse Diode Power Reverse Protection

By adding to the GND network, the current flowing into IC GND will be limited, thus protecting the device.

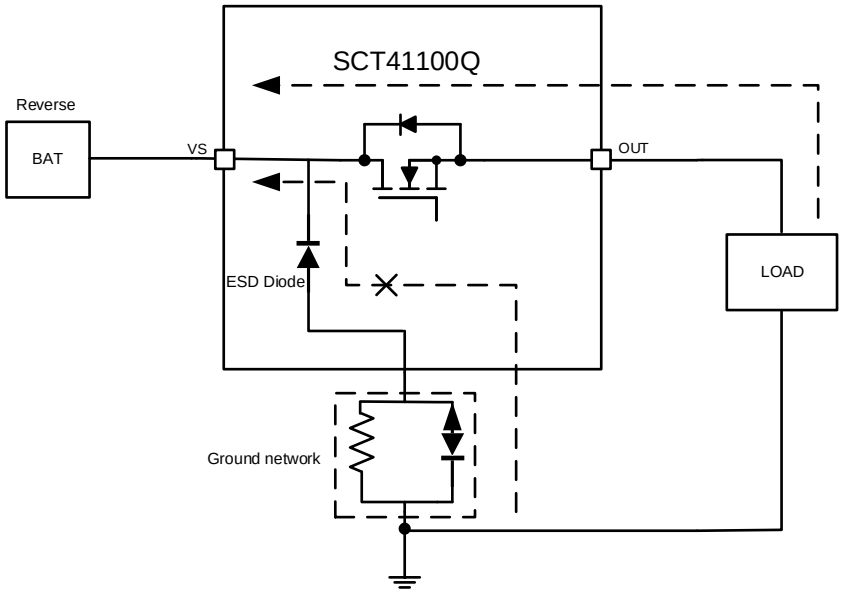

Figure 15. Ground Network Power Reverse Protection

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MCU I/O Protection

In some extreme cases, such as ISO7637-2 testing or inductive load input disconnection, negative voltage pulses may appear in the IC GND relative to the system ground. To protect the MCU and the device, it is recommended to connect a series resistor between the MCU and the SCT41100Q logic control pin.

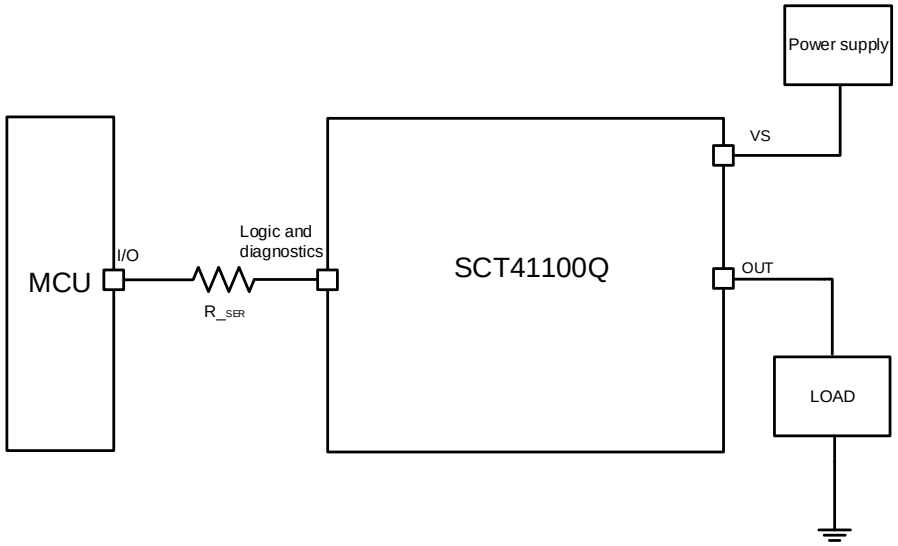

Figure 16. MCU I/O Protection

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Typical Application

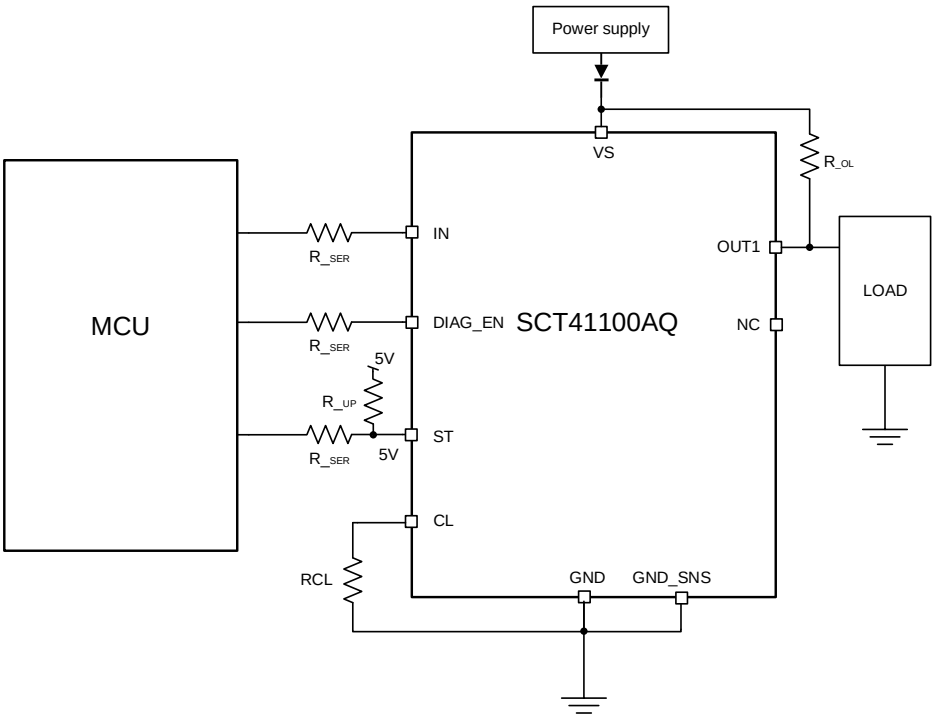

Figure 17. Version A Application Schematic

Design Parameters

Design Parameters	Example Value
Input Voltage	13.5V Normal 8V to 18V
Load Current	Typical 4A
Current Limit	5A
MCU Voltage	5V

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Typical Application (continued)

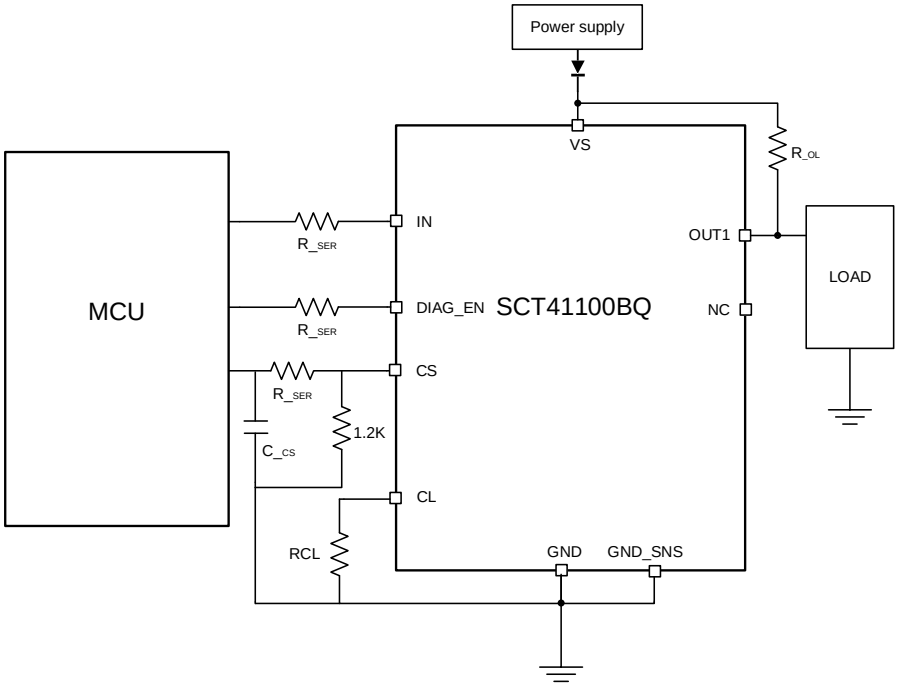

Figure 18. Version B Application Schematic

Design Parameters

Design Parameters	Example Value
Input Voltage	13.5V Normal 8V to 18V
Load Current	Typical 4A
Current Limit	5A
MCU Voltage	5V
Current Sense Range	0-4A

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Application Waveforms

V_{VS}=13.5V, unless otherwise noted

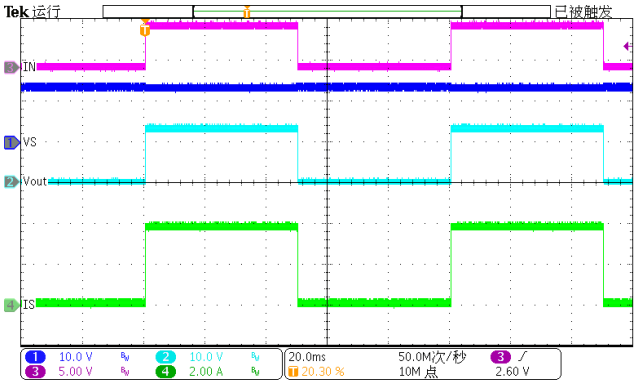

Figure 19. IN Toggle resistive load 4A

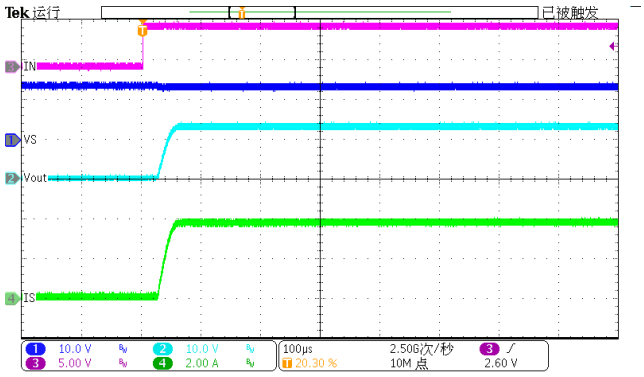

Figure 20. IN On resistive load 4A

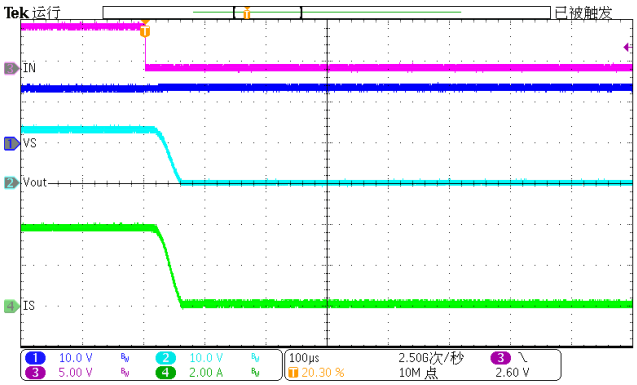

Figure 21. IN Off resistive load 4A

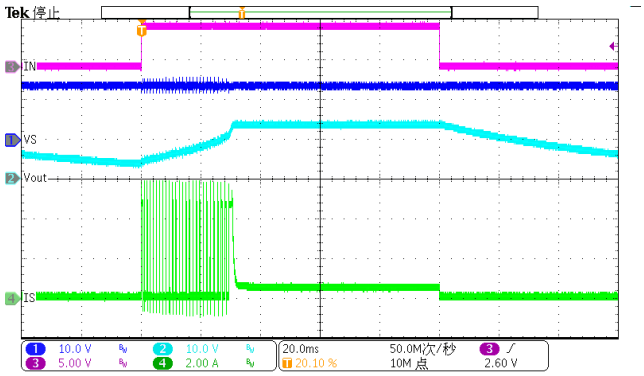

Figure 22. IN Toggle capacitive load C=2.2mF

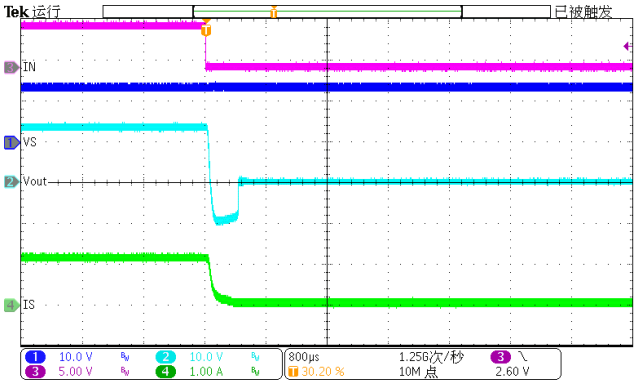

Figure 23. IN Off Inductive load L=8mH series resistor=13.5Ω

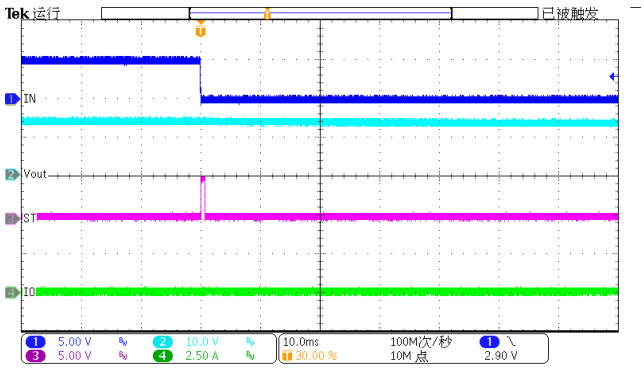

Figure 24. Open-load detection for version A

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Application Waveforms(continued)

V_{VS}=13.5V, unless otherwise noted

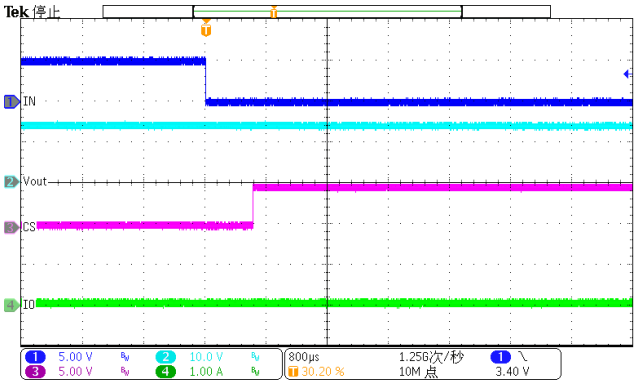

Figure 25. Open-load detection for version B

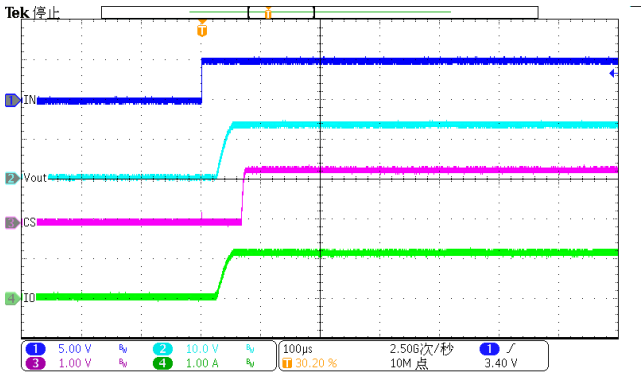

Figure 26. IN On current sense load=0.5A

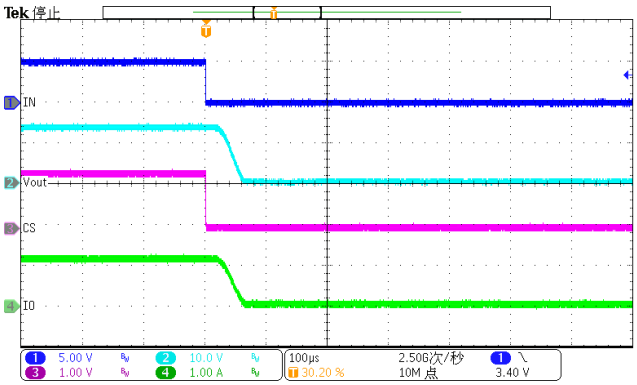

Figure 27. IN Off current sense load=0.5A

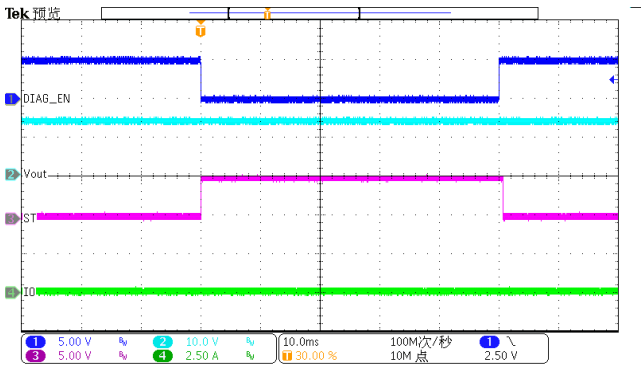

Figure 28. DIAG_EN Toggle for version A

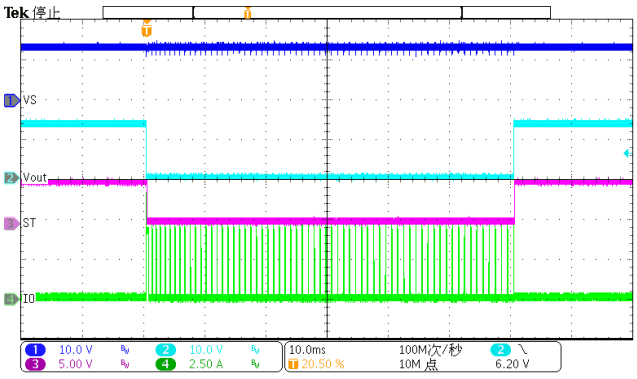

Figure 29. Overcurrent detection for version A

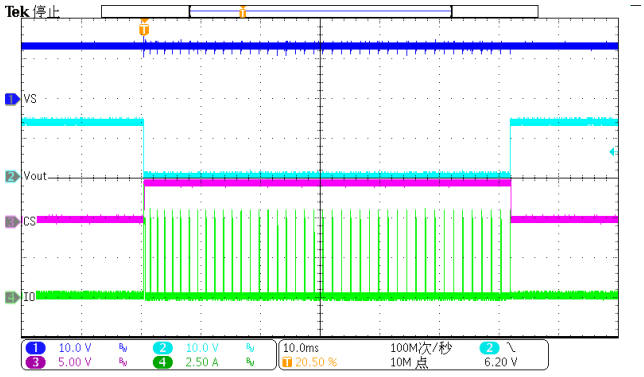

Figure 30. Overcurrent detection for version B

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Layout Guideline

The PCB layout is very important. Good PCB design can optimize heat transfer, which is absolutely essential for the long-term reliability of the device.

1. Maximize the copper coverage on the PCB to increase the thermal conductivity of the board. Maximum copper is extremely important when there are not any heat sinks attached to the PCB on the other side of the package.
2. More vias should be placed below the device Thermal PAD to further improve heat transfer.
3. R_{CL} should be connected to IC GND.

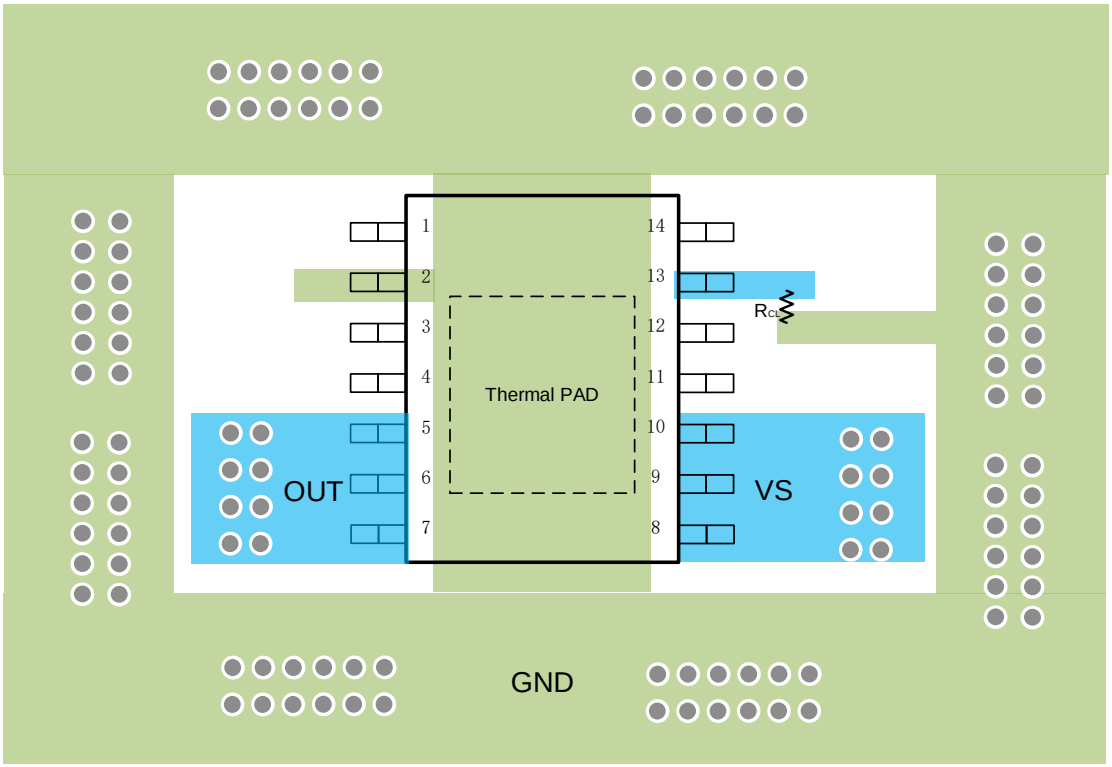

Figure 31. Without a GND Network PCB Layout

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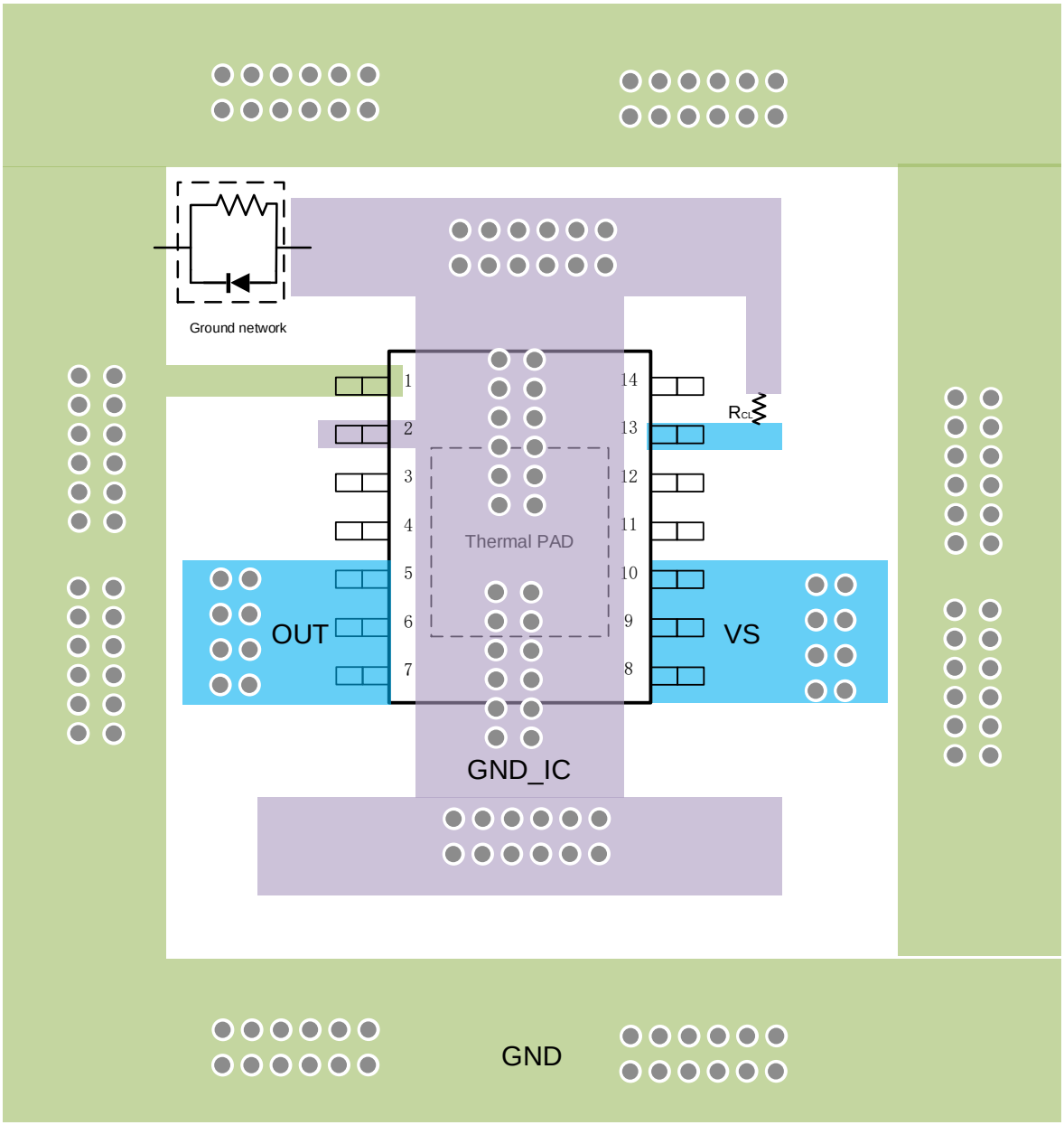

Figure 32. With a GND Network PCB Layout

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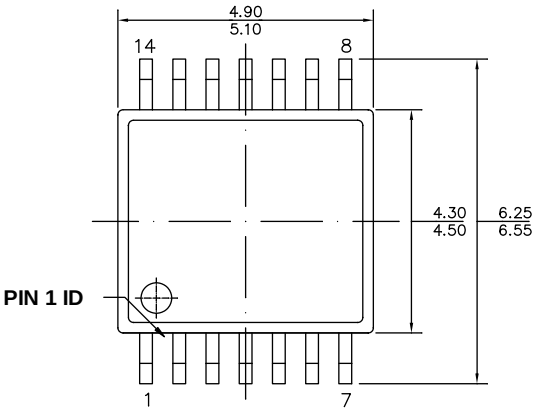
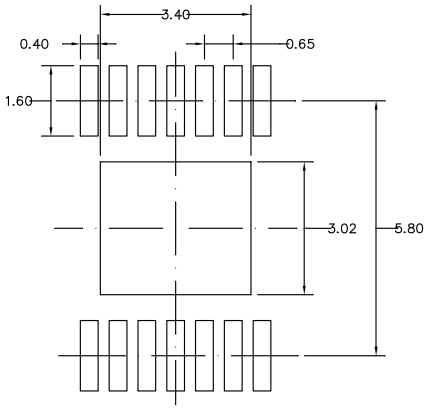
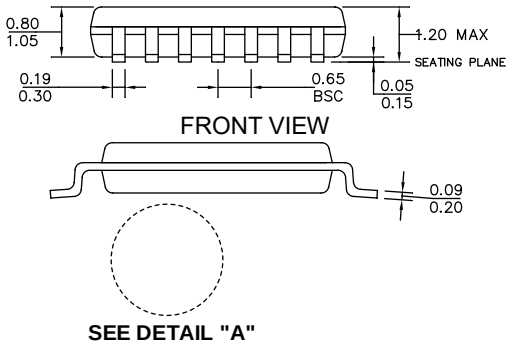
PACKAGE INFORMATION



TOP VIEW

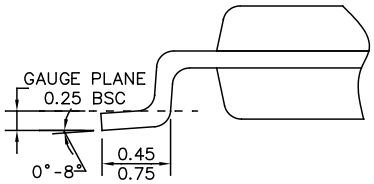


BOTTOM VIEW

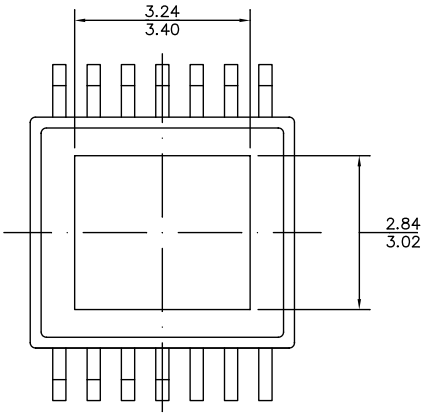


FRONT VIEW

SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS..
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3. PACKAGE WITDH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5. DRAWING CONFORMS TO JEDEC MO-153, VARIATION ABT.
6. DRAWING IS NOT TO SCALE.

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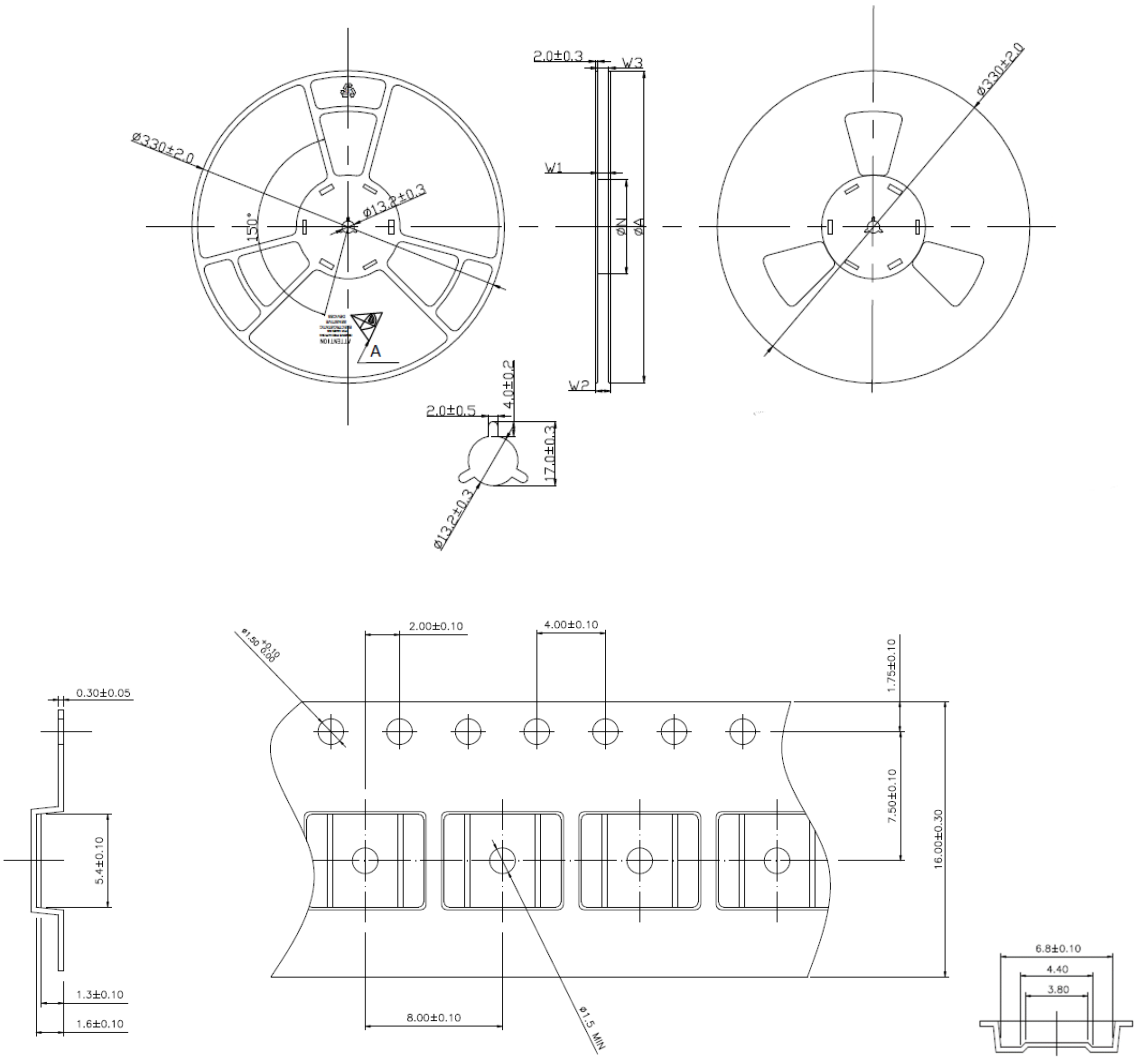
TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT41100AQMZER	ESOP-14	14	4000
SCT41100BQMZER	ESOP-14	14	4000



NOTES:
1. 10 sprocket hole pitch cumulative tolerance ±0.2.
2.Camber not to exceed 1mm in 100mm
3.Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
4.Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier
5. Pocket position relative to sprocket hole measured as true position of pocket not pocket hole.
6.Pocket center and pocket hole center must be same position.

TAPE DIMENSIONS

W (mm)	ΦA (mm)	ΦN (mm)	W1 (mm)	W2(Max) (mm)	W3(Max) (mm)
16	330±2.0	100±1.0	16.4±0.5	22.4	15.9/19.4

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