1MHz, 3A Synchronous Step-Down Converter with Soft Start

DESCRIPTION

The EUP3083 is a constant frequency, current mode, PWM step-down converter. The device integrates a main switch and a synchronous rectifier for high efficiency. The 2.7V to 5.5V input voltage range makes the EUP3083 ideal for powering portable equipment that runs from a single cell Lithium-Ion (Li+) battery or 3-cell NiMH/ NiCd batteries. The output voltage can be regulated as low as 0.6V. The EUP3083 supports up to 3A load current and can also run at 100% duty cycle for low dropout applications, extending battery life in portable systems. Switching frequency is internally set at 1MHz, allowing the use of small surface mount inductors and capacitors.

The EUP3083 is available in TDFN-8L(2×2) Package.

FEATURES

- High Efficiency up to 95%
- Low R_{DSON} for internal switches:
  High-side: 100mΩ
  Low-side: 60mΩ
- 2.7V to 5.5V Input Voltage Range
- 3A Available Load Current
- 30μA Typical Quiescent Current
- 1MHz Constant Switching Frequency
- Adjustable Output Voltage as Low as 0.6V
- 100% Duty Cycle Low Dropout Operation
- Short Circuit and Thermal Protection
- Excellent Line and Load Transient Response
- Soft Start Function
- Power Good
- Available in TDFN-8L(2×2) Package
- RoHS Compliant and Halogen-Free

APPLICATIONS

- Cellular and Smart Phones
- Portable Media Players/ MP3 Players
- Digital Still and Video Cameras
- Portable Instruments
- WLAN PC Cards

Typical Application Circuit

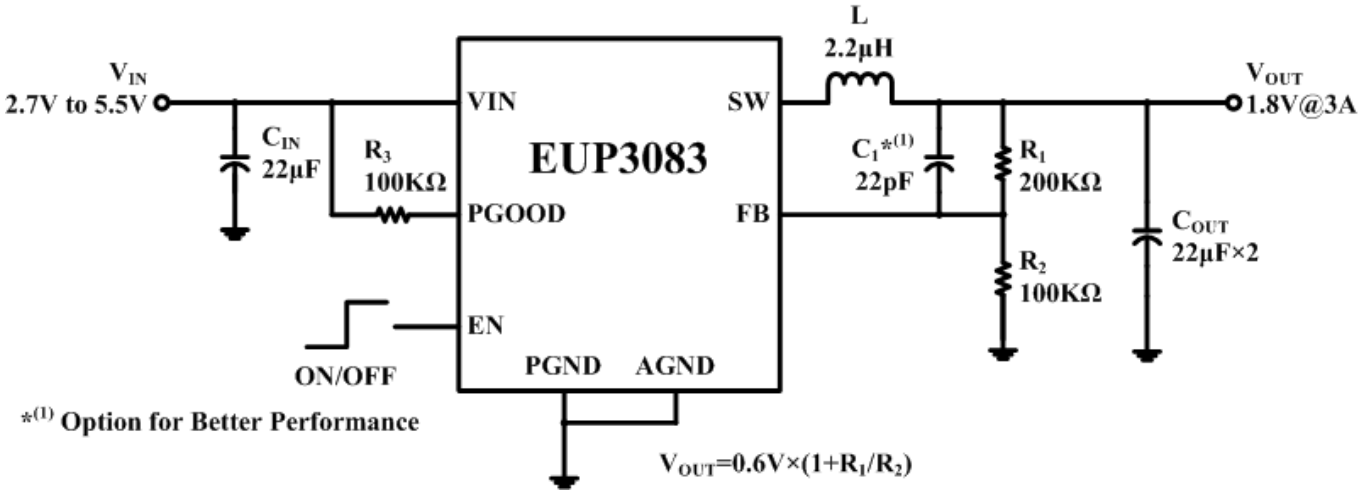


Figure 1. Application Circuit

Functional Block Diagram

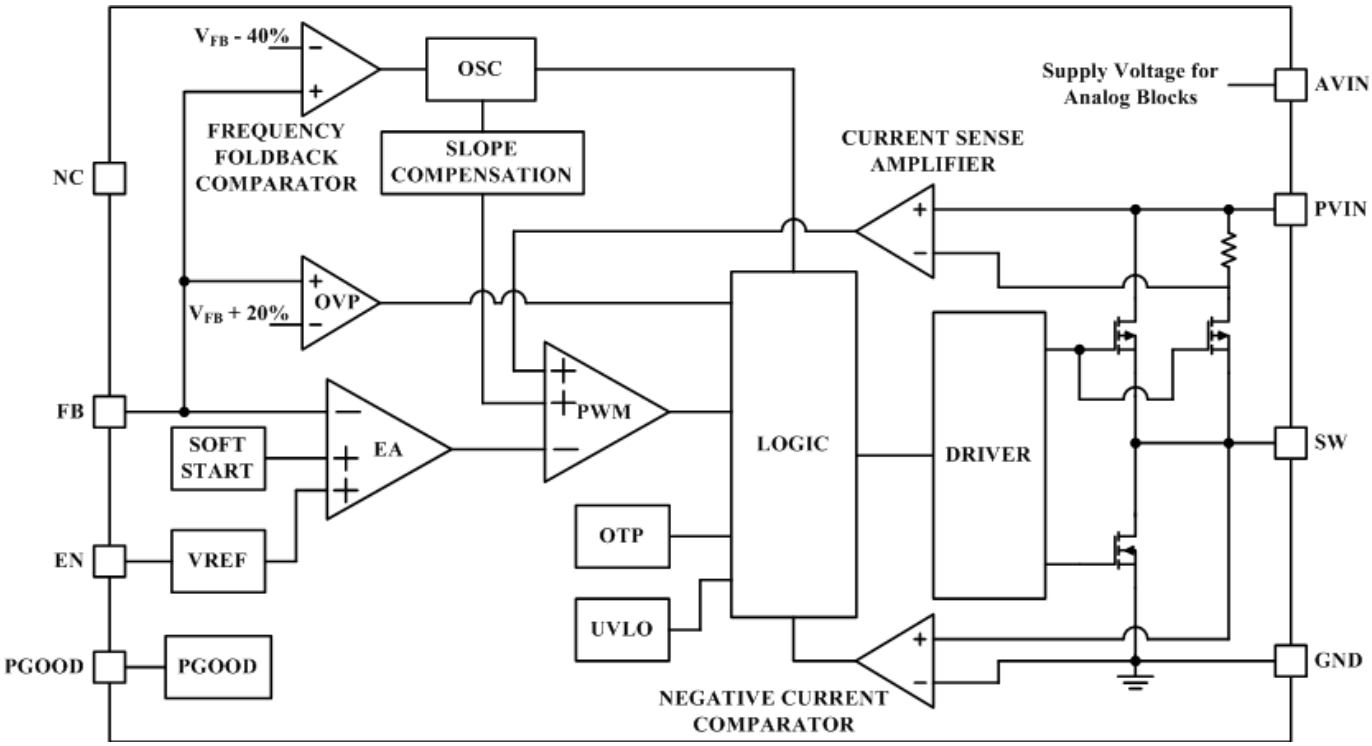
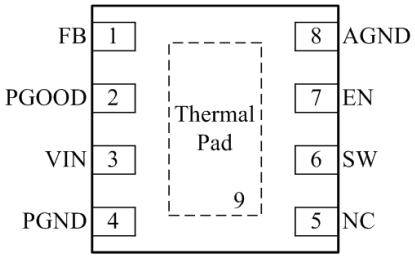


Figure 2. Block Diagram

Pin Configurations

Package Type	Pin Configurations
EUP3083 TDFN-8L(2×2)	

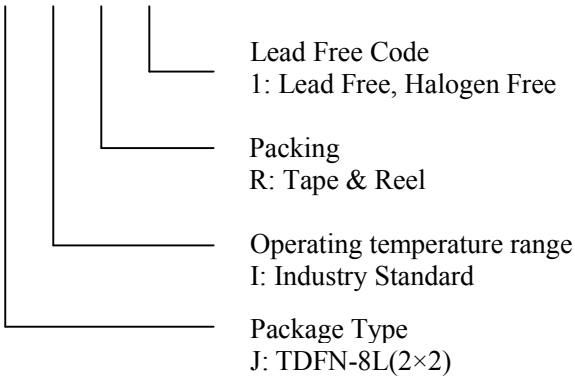
Pin Description

PIN	EUP3083 TDFN-8L(2×2)	DESCRIPTION
FB	1	Feedback Pin.
PGOOD	2	Power Good Output Pin. PGOOD indicates the status of the output voltage.
VIN	3	Supply Voltage Pin.
PGND	4	Power Ground Pin.
NC	5	No Internal Connect (Floating or Connecting to GND).
SW	6	Switch Node Connection to Inductor. This pin connects to the drains of the internal main and synchronous power MOSFET switches.
EN	7	Chip Enable Pin. Forcing this pin above 1.5V enables the part. Forcing this pin below 0.3V shuts down the device. Do not leave EN floating.
AGND	8	Signal Ground Pin.
Thermal Pad	9	The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.

Ordering Information

Order Number	Package Type	Marking	Quantity per Reel	Operating Temperature Range
EUP3083JIR1	TDFN-8L(2×2)	XXX a00	3000	-40 °C to +85°C

EUP3083 □ □ □ □



Absolute Maximum Ratings(1)

- Input Supply Voltage V_{IN} ---------- -0.3V to 6V
- EN, FB, SW Voltages ---------- -0.3V to V_{IN} +0.3V
- SW to GND (<20ns) ---------- -3V to V_{IN} +3V
- Junction Temperature ---------- 150°C
- Storage Temperature ---------- -65°C to +150°C
- Lead Temp (Soldering, 10sec) ---------- 260°C
- Thermal Resistance θ_{JA} (TDFN-8L(2×2)) ---------- 66°C /W

Recommend Operating Conditions(2)

- Supply Voltage (V_{IN}) ---------- 2.7V to 5.5V
- Operating Temperature Range ---------- -40°C to +85°C

Note (1): Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.

Note (2): The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

Unless otherwise specified, T_A=+25°C, V_{IN}=3.6V.

Symbol	Parameter	Conditions	EUP3083			Unit
			Min	Typ	Max	
General Section						
V_{IN}	Input Voltage Range		2.7		5.5	V
V_{UVLO}	V_{IN} under Voltage Lockout Threshold	V_{IN} Rising		2.35	2.5	V
		V_{IN} Falling	2	2.15		
I_Q	Quiescent Current	V_{FB}=105%×V_{REF}, SW open		30		μA
I_{SHDN}	Shutdown Current	V_{EN}=0V			1	μA
V_{ENH}	EN Threshold	On State			1.5	V
V_{ENL}		Off State	0.3			V
V_{FB}	Regulated Feedback Voltage	(3)	0.594	0.600	0.606	V
Modulator Section						
R_{PMOS}	PMOS on Resistance	I_{SW}=200mA		100		mΩ
R_{NMOS}	NMOS on Resistance	I_{SW}=-200mA		60		mΩ
F_{OSC}	Oscillator Frequency	V_{FB}=0.6V	0.8	1	1.2	MHz
		V_{FB}=0V		354		KHz
I_{PK}	Peak Inductor Current	V_{IN}=5V, V_{FB}=90%×V_{REF}		5		A
R_{DSCH}	Output Discharge Switch on Resistance			45		Ω
T_{SD}	Thermal Shutdown Threshold			160		℃
$T_{SD\ HYS}$	Thermal Shutdown Hysteresis			30		℃
Soft Start and Power Good Section						
T_{SS}	Soft Start Time		0.56	0.75	0.94	ms
V_{PGLR}	PGOOD Low Threshold	FB rising, PG Low to High		90		%
V_{PGLF}		FB falling, PG High to Low		85		
R_{PG}	PGOOD Open-Drain Impedance (PGOOD=low)			35		Ω

Note (3): The EUP3083 is tested in a proprietary test mode that connects FB to the output of the error amplifier.

Suggested Component Values

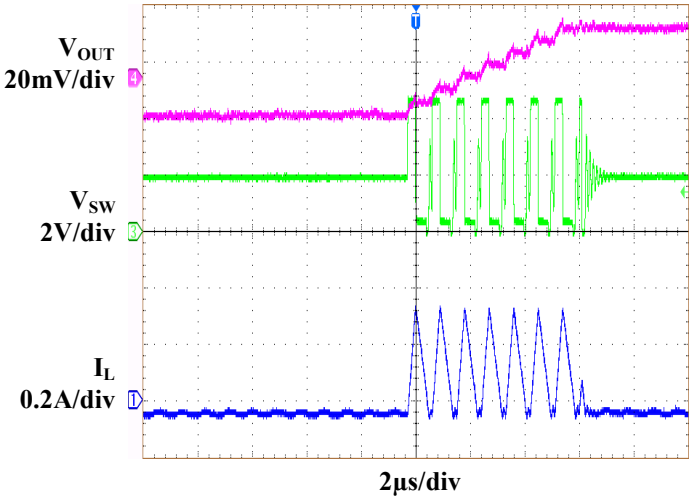
V_{OUT} (V)	C_{IN} (μF)	L (μH)	C_1 (pF)(4)	R_1 (KΩ)	R_2 (KΩ)	C_{OUT} (μF)
1	22	2.2	22	66.5	100	22×2
1.05	22	2.2	22	75	100	22×2
1.2	22	2.2	22	100	100	22×2
1.5	22	2.2	22	150	100	22×2
1.8	22	2.2	22	200	100	22×2
3.3	22	2.2	22	450	100	22×2

Note (4): C_1 is an optional capacitor for better performance.

Typical Operating Characteristics

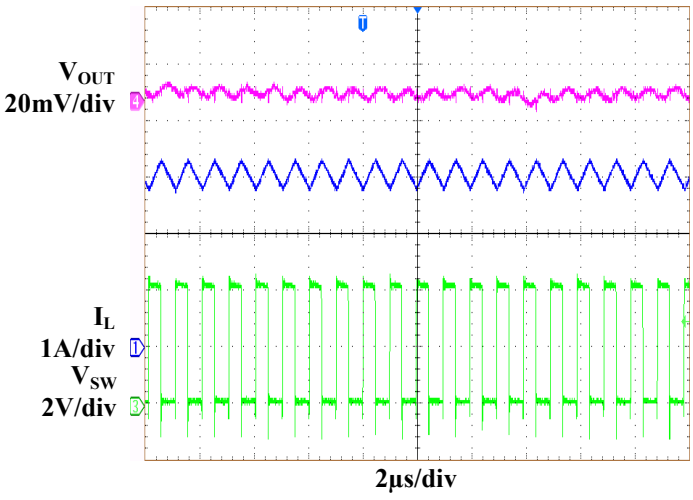
Steady State

V_{IN}=5V, V_{OUT}=1.8V, No Load



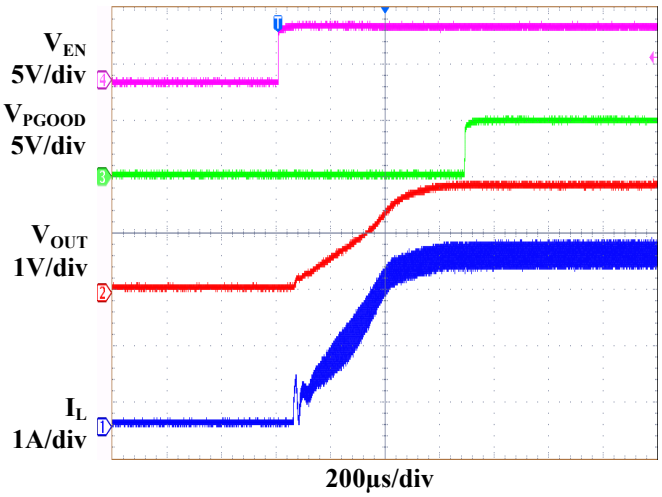
Steady State

V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A



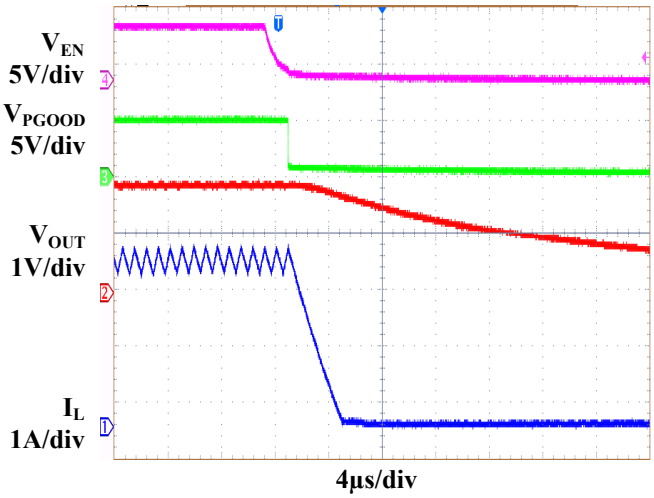
Startup through Enable

V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A



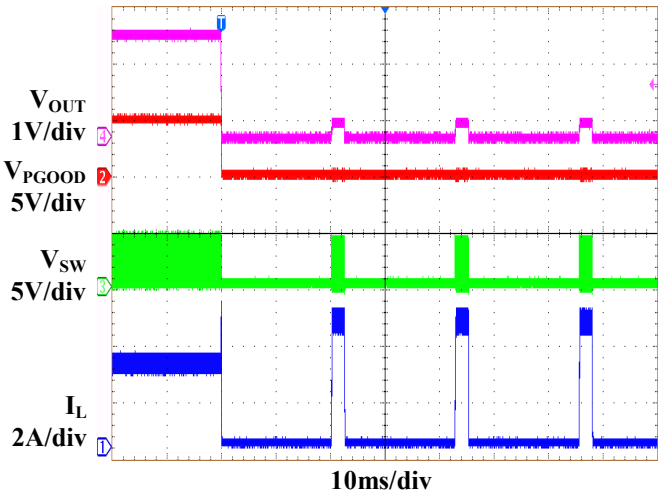
Shutdown through Enable

V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A



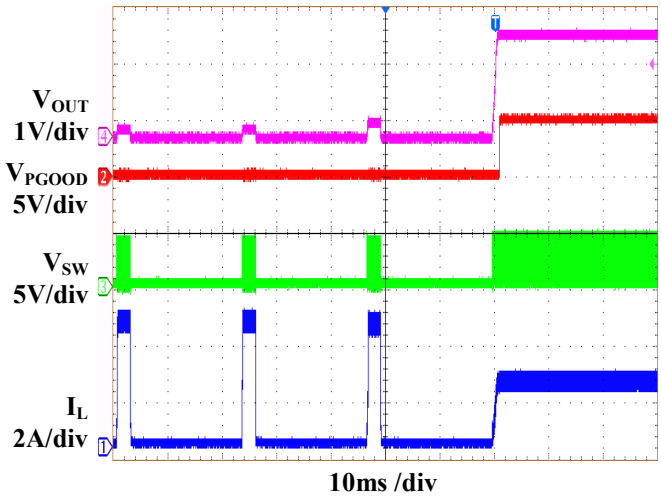
Short Circuit

V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A



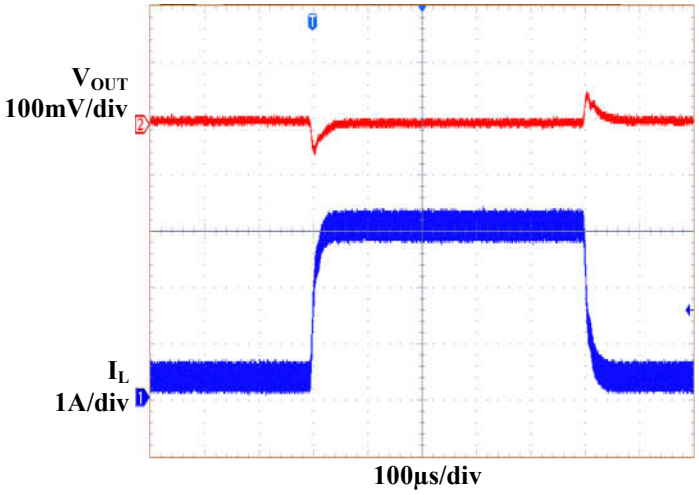
Short Circuit Recovery

V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=3A

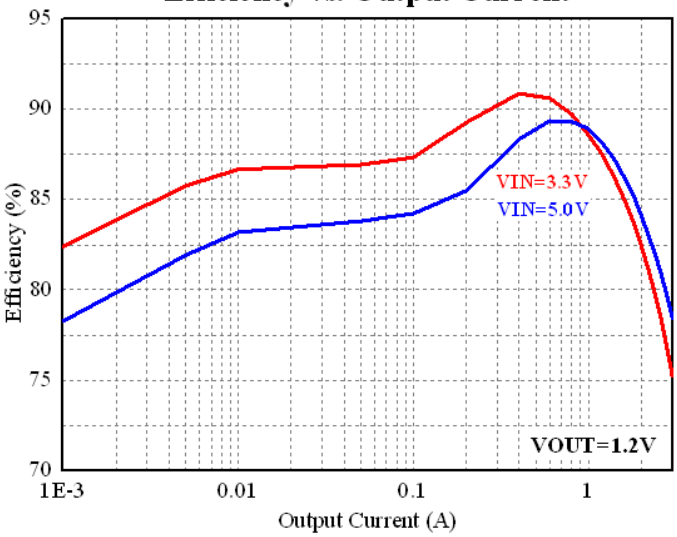


Load Transient Response

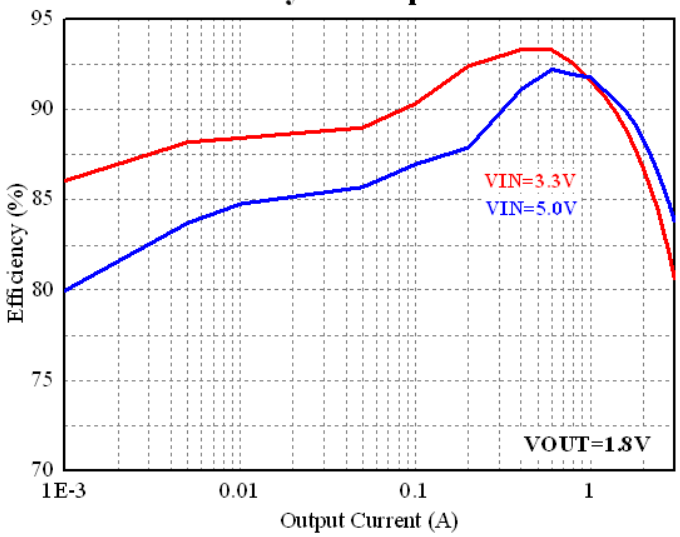
V_{IN}=5V, V_{OUT}=1.8V, I_{OUT}=0.3A to 3A



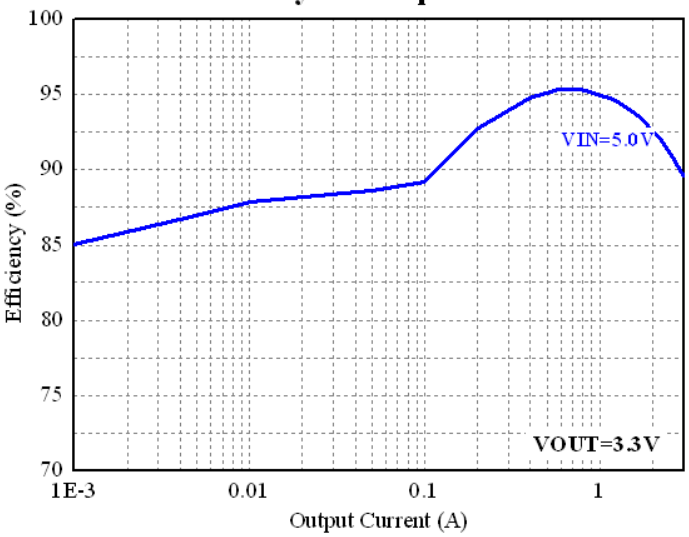
Efficiency vs. Output Current



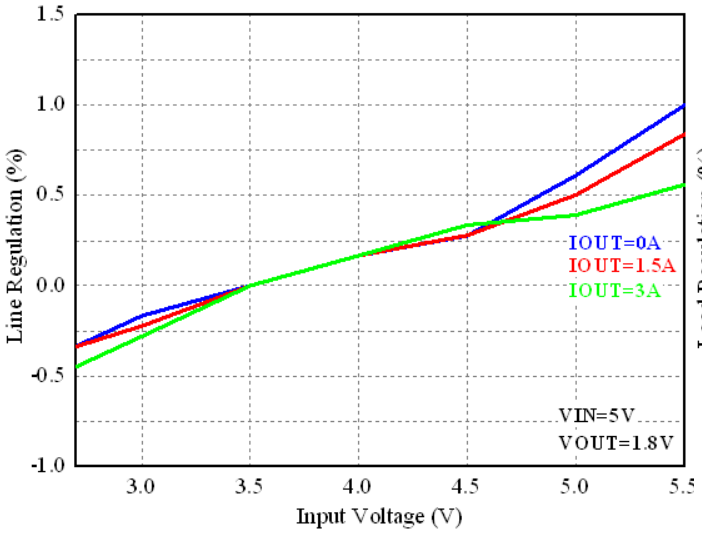
Efficiency vs. Output Current



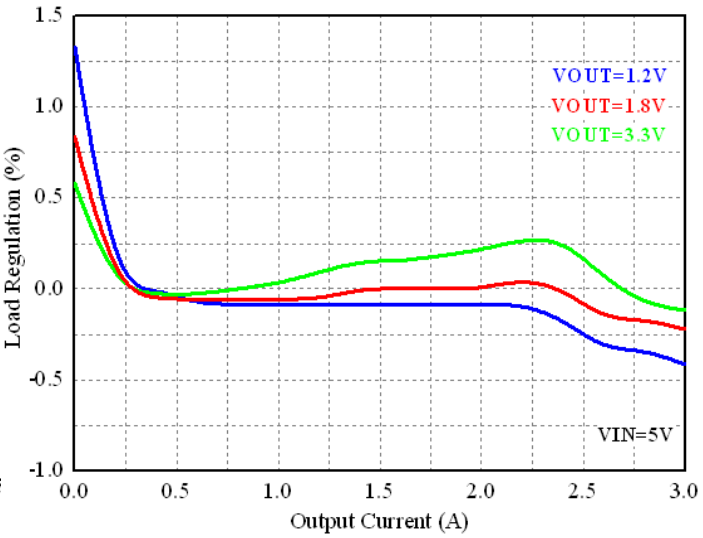
Efficiency vs. Output Current



Line Regulation



Load Regulation



Application Information

Main Control Loop

The EUP3083 uses a slope-compensated constant frequency, current mode architecture. Both the main (P-Channel MOSFET) and synchronous (N-channel MOSFET) switches are internal. During normal operation, the EUP3083 regulates output voltage by switching at a constant frequency and then modulating the power transferred to the load each cycle using PWM comparator. The duty cycle is controlled by three weighted differential signals: the output of error amplifier, the main switch sense voltage and the slope-compensation ramp. It modulates output power by adjusting the inductor-peak current during the first half of each cycle. An N-channel, synchronous switch turns on during the second half of each cycle (off time). When the inductor current starts to reverse or when the PWM reaches the end of the oscillator period, the synchronous switch turns off. This keeps excess current from flowing backward through the inductor, from the output capacitor to GND, or through the main and synchronous switch to GND.

Inductor Selection

The output inductor is selected to limit the ripple current to some predetermined value, large value inductors lower the ripple currents. Higher V_{IN} or V_{OUT} also increases the ripple current as shown in equation. A reasonable starting point for setting ripple current is ΔI_L=400mA.

$$\Delta I_L = \frac{1}{(f)(L)} \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 3.2A rated inductor should be enough for most applications (3A+200mA). For better efficiency, choose a low DC-resistance inductor.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. The primary function of the input capacitor is to provide a low impedance loop for the edges of pulsed current drawn by the EUP3083. A low ESR input capacitor sized for the maximum RMS current must be used. The size required will vary depending on the load, output voltage and input voltage source impedance characteristics. A typical value is around 22µF.

The input capacitor RMS current varies with the input voltage and the output voltage. The equation for the maximum RMS current in the input capacitor is:

$$I_{RMS} = I_O \times \sqrt{\frac{V_O}{V_{IN}} \times \left(1 - \frac{V_O}{V_{IN}}\right)}$$

The output capacitor C_{OUT} has a strong effect on loop stability. The selection of C_{OUT} is driven by the required effective series resistance (ESR). ESR is a direct function of the volume of the capacitor, that is, physically larger capacitors have lower ESR. Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \times \left(ESR + \frac{1}{8fC_{OUT}}\right)$$

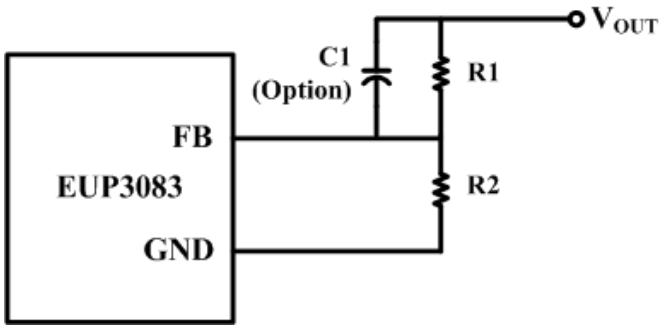
When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6V \times \left(1 + \frac{R1}{R2}\right)$$

For EUP3083 application, the external resistive divider is connected to the output, allowing remote voltage sensing as shown in below figure.



C1 is an optional feed-forward capacitor which can speed loop response and reduce output ripple during load transient. A typical value is around 22pF.

Short Circuit Protection

Short circuit protection continually monitors the FB voltage after soft-start is completed. If output voltage is lower than 60% of the nominal output voltage by over current or short circuit, the device will enters hiccup mode. In hiccup mode, there is a 20ms delay time period before restart.

Thermal Considerations

To avoid the EUP3083 from exceeding the maximum

junction temperature, the user will need to do a thermal analysis. The goal of the thermal analysis is to determine whether the operating conditions exceed the maximum junction temperature of the part. The temperature rise is given by:

$$T_R=(P_D)(\theta_{JA})$$

Where $P_D=I_{LOAD}^2 \times R_{DS(ON)}$ is the power dissipated by the regulator; θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.
The junction temperature, T_J, is given by:

$$T_J=T_A+T_R$$

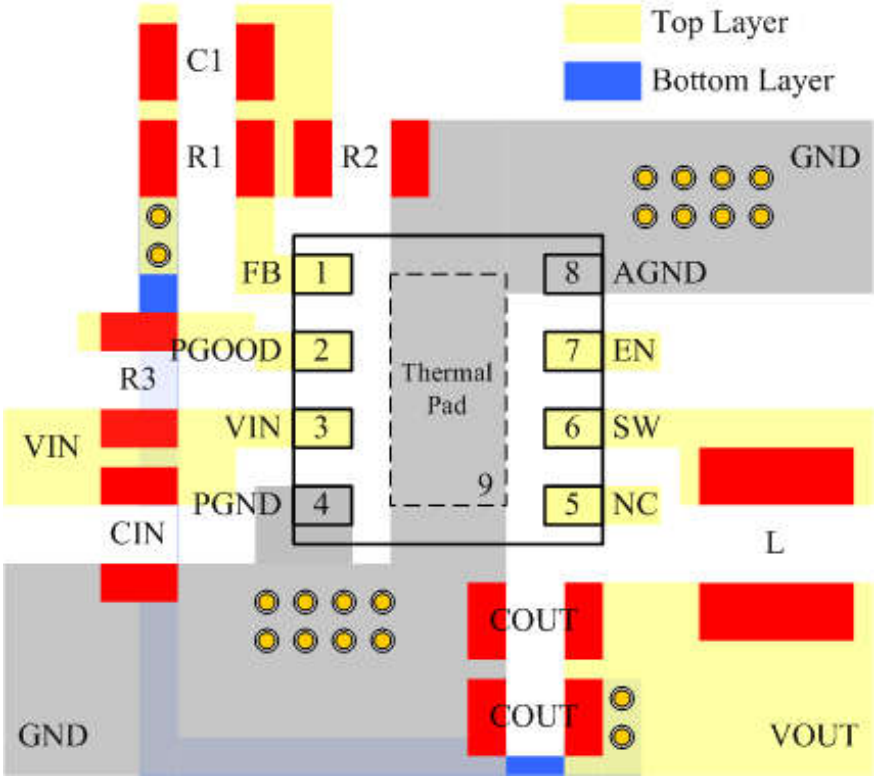
Where T_A is the ambient temperature. T_J should be below the maximum junction temperature of 150°C.

PC Board Layout Checklist

When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the EUP3083.

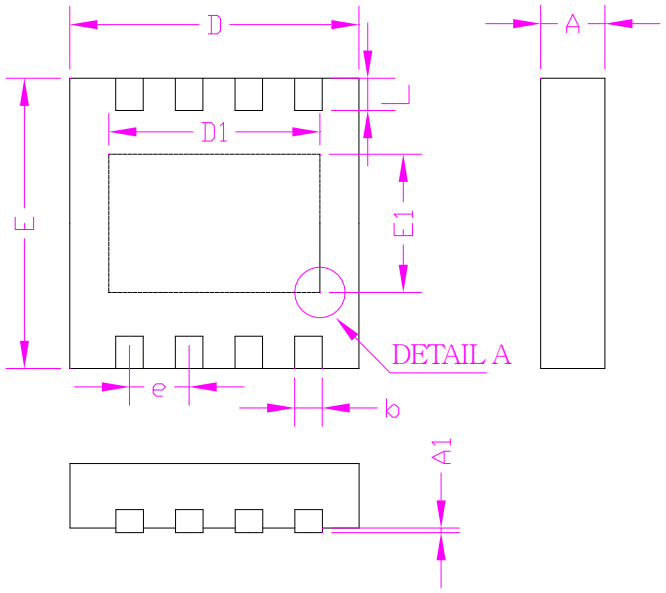
1. The input capacitor C_{IN} should connect to V_{IN} as closely as possible. This capacitor provides the AC current to the internal power MOSFETs.
2. The power traces, consisting of the GND trace, the SW trace and the V_{IN} trace should be kept short, direct and wide.
3. The FB pin should connect directly to the feedback resistors. The resistive divider R1/R2 must be connected between the C_{OUT} and ground.
4. Keep the switching node, SW, away from the sensitive FB node.

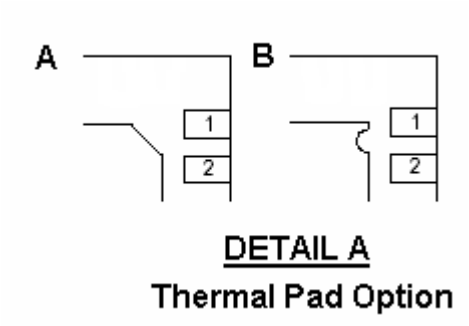
An example of PCB layout guide is shown in the figure below for reference.



Packaging Information

TDFN-8L(2×2)





SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	-	0.05	0.000	-	0.002
b	0.15	0.25	0.35	0.006	0.010	0.014
D	1.90	2.00	2.10	0.075	0.079	0.083
D1	1.10	1.40	1.70	0.043	0.055	0.067
E	1.90	2.00	2.10	0.075	0.079	0.083
E1	0.60	0.80	1.00	0.024	0.031	0.039
e		0.50			0.020	
L	0.25	0.35	0.45	0.010	0.014	0.180