

Advanced Stereo Headphone Amplifier

DESCRIPTION

EUA6211 is a dual audio power amplifier designed for portable communication device applications such as mobile phones. EUA6211 operates from a single 2.5V to 5.5V supply, consumes only 3.8mA of supply current, capable of delivering 30mW of continuous average power into a 16Ω load from a 3V power supply with a THD+N of 1%.

Base on the power supply delivered to the device, an internal power management block generates a negative voltage. Thus, the internal amplifiers provide outputs referenced to Ground. In this configuration, the two external heavy coupling capacitors can be removed. It offers significant space and cost savings compared to a typical stereo application.

EUA6211 has an internal gain of $-1.5V/V$ with low 0.03% THD+N performance. An 80dB at 1kHz power-supply rejection ratio (PSRR) allows these devices to operate from noisy digital supplies without an additional linear regulator. Comprehensive click-and-pop circuitry suppresses audible clicks and pops on startup and shutdown.

Other features include short-circuit and thermal-overload protection, and are specified over the extended $-40^{\circ}C$ to $+85^{\circ}C$ temperature range. EUA6211 can also use in line driver application. The device is available in TDFN-12 package.

FEATURES

- No Bulky DC-Blocking Capacitors Required
- 2.5V to 5.5V Operation
- Fixed $-1.5V/V$ Gain
- Low 0.03% THD+N
- High PSRR (80dB at 1kHz)
- Integrated Click-and-Pop Suppression
- Low Quiescent Current (3.8mA)
- Low-Power Shutdown Mode, $< 0.1\mu A$
- SNR $> 105dB$
- Typical $V_n < 10\mu V_{rms}$ 20Hz-20kHz
- THD+N $< 0.005\%$ at 10kΩ Load
- 2V_{rms} Output Voltage Into 600Ω Load
- Short Circuit and Thermal Protection
- $\pm 8kV$ HBM ESD-Protected Outputs
- Available in TDFN-12 Package
- RoHS Compliant and 100% Lead(Pb)-Free Halogen-Free

APPLICATIONS

- Cellular Phones
- MP3 Players
- Notebook PCs
- Handheld Gaming Consoles

Typical Application Circuit

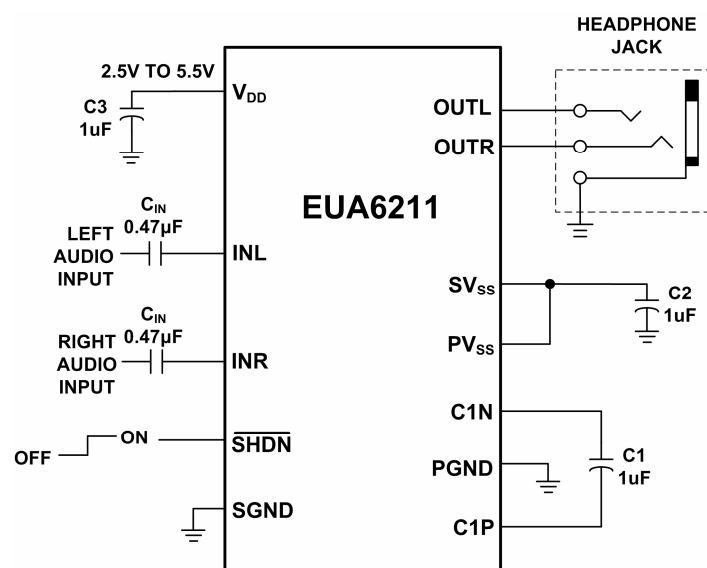


Figure1.

Typical Application Circuit (Line Driver Application)

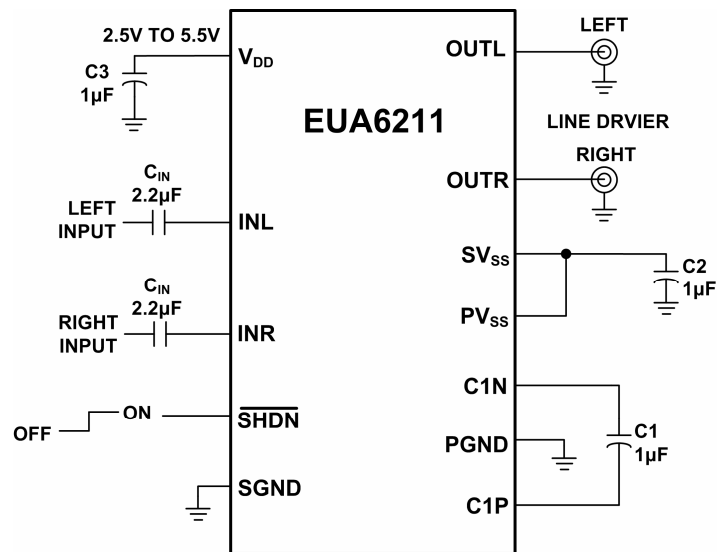


Figure2.

Block Diagram

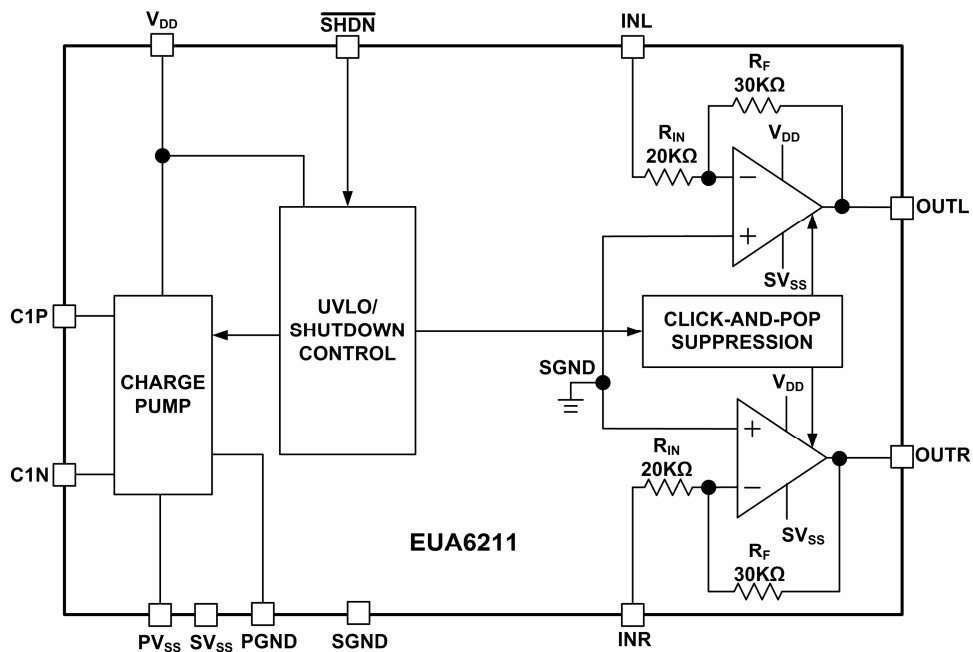


Figure3.

Pin Configurations

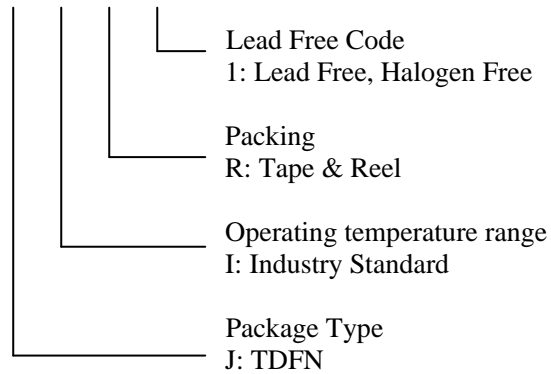
Package Type	Pin Configurations																																							
TDFN-12	<p>(TOP VIEW)</p> <p>The diagram shows a rectangular package with 12 pins arranged in two columns of six. A central rectangular area is labeled 'Thermal Pad'. The pins are numbered 1 through 12, with corresponding labels to their left and right.</p> <table><tr><th>Pin Label</th><th>Pin Number</th><th>Pin Label</th></tr><tr><td>SV_{SS}</td><td>1</td><td>12</td></tr><tr><td>PV_{SS}</td><td>2</td><td>11</td></tr><tr><td>C1N</td><td>3</td><td>10</td></tr><tr><td>PGND</td><td>4</td><td>9</td></tr><tr><td>C1P</td><td>5</td><td>8</td></tr><tr><td>V_{DD}</td><td>6</td><td>7</td></tr><tr><td></td><td></td><td>OUTL</td></tr><tr><td></td><td></td><td>OUTR</td></tr><tr><td></td><td></td><td>INL</td></tr><tr><td></td><td></td><td>SHDN</td></tr><tr><td></td><td></td><td>INR</td></tr><tr><td></td><td></td><td>SGND</td></tr></table>	Pin Label	Pin Number	Pin Label	SV _{SS}	1	12	PV _{SS}	2	11	C1N	3	10	PGND	4	9	C1P	5	8	V _{DD}	6	7			OUTL			OUTR			INL			SHDN			INR			SGND
Pin Label	Pin Number	Pin Label																																						
SV _{SS}	1	12																																						
PV _{SS}	2	11																																						
C1N	3	10																																						
PGND	4	9																																						
C1P	5	8																																						
V _{DD}	6	7																																						
		OUTL																																						
		OUTR																																						
		INL																																						
		SHDN																																						
		INR																																						
		SGND																																						

Pin Description

PIN	TDFN-12	DESCRIPTION
SV _{SS}	1	Amplifier Negative Supply. Connect to PV _{SS} .
PV _{SS}	2	Charge-Pump Output. Connect to SV _{SS} and bypass with a 1μF ceramic capacitor to PGND.
C1N	3	Flying Capacitor Negative Terminal. Connect a 1μF ceramic capacitor from C1P to C1N.
PGND	4	Power Ground. Connect to SGND.
C1P	5	Flying Capacitor Positive Terminal. Connect a 1μF ceramic capacitor from C1P to C1N.
V _{DD}	6	Positive Power-Supply Input. Bypass with a 1μF capacitor to PGND.
SGND	7	Signal Ground. Connect to PGND.
INR	8	Right-Channel Input.
SHDN	9	Active-Low Shutdown Input.
INL	10	Left-Channel Input.
OUTR	11	Right-Channel Output.
OUTL	12	Left-Channel Output.
Thermal Pad	-	Exposed pad, it can be left floating, ensure that the exposed pad is isolated from PGND and SGND.

Ordering Information

Order Number	Package Type	Marking	Quantity per Reel	Operating Temperature Range
EUA6211JIR1	TDFN-12	XXXXX A6211	2500	-40 °C to 85°C

EUA6211 ☐ ☐ ☐ ☐

Absolute Maximum Ratings

▪ V_{DD} to GND	-----	-0.3 V to +6V
▪ PV_{SS} , SV_{SS}	-----	-0.3V to +0.3V
▪ PGND to SGND	-----	-0.3V to +0.3V
▪ C1P to PGND	-----	-0.3V to ($V_{DD}+0.3V$)
▪ C1N to PGND	-----	($PV_{SS}-0.3V$) to +0.3V
▪ PV_{SS} , SV_{SS} to PGND	-----	-6V to +0.3V
▪ IN_{-} to SGND	-----	($SV_{SS}-0.3V$) to ($V_{DD}+0.3V$)
▪ OUT_{-} to SV_{SS} (Note 1)	-----	-0.3V to Min ($V_{DD} - SV_{SS}+0.3V$, +9V)
▪ OUT_{-} to SV_{SS} (Note 2)	-----	+0.3V to Max ($SV_{SS} - V_{DD}-0.3V$, -9V)
▪ \overline{SHDN} to GND	-----	-0.3V to +6V
▪ Storage temperature	-----	-65°C to 150°C
▪ Junction Temperature	-----	150°C
▪ Lead Temperature (soldering, 10s)	-----	260°C
▪ Thermal Resistance		
θ_{JA} (TDFN-12)	-----	70°C/W

Note 1: $OUTR$ and $OUTL$ should be limited to no more than 9V above SV_{SS} , or above $V_{DD} + 0.3V$, whichever limits first.

Note 2: $OUTR$ and $OUTL$ should be limited to no more than 9V below V_{DD} , or below $SV_{SS} - 0.3V$, whichever limits first.

Electrical Characteristics

($V_{DD}=5V$, $PGND=SGND$, $\overline{SHDN}=5V$, $C1=C2=1\mu F$, $R_L=\infty$, resistive load reference to ground; gain= -1.5V/V, $T_A=-40^{\circ}C$ to $+85^{\circ}C$, unless otherwise noted. Typical values are at $T_A=25^{\circ}C$.) (Note 3)

Symbol	Parameter	Conditions	EUA6211			Unit
			Min.	Typ.	Max.	
GENERAL						
V _{DD}	Supply Voltage Range	Guaranteed by PSRR test	2.5		5.5	V
I _{CC}	Quiescent Current			3.8	5.5	mA
I _{SHDN}	Shutdown Current	$\overline{SHDN}=SGND=PGND$		0.1	1	μA
t _{SON}	Shutdown to Full Operation			160		μs
R _{IN}	Input Impedance	measured at INL/INR	12	19	28	kΩ
V _{OS}	Output Offset Voltage	(Note 4)		± 1	± 10	mV
PSRR	Power-Supply Rejection Ratio	V _{DD} =2.7V to 5.5V, T _A =+25°C		88		dB
		f=1kHz, 100mV _{P-P} (Note 4)		80		
		f=20kHz, 100mV _{P-P} (Note 4)		60		
P _{OUT}	Output Power	R _L =32Ω, THD+N=1%		130		mW
		R _L =16Ω, THD+N=1%		120		
A _V	Voltage Gain		-1.52	-1.5	-1.48	V/V
	Channel-to-Channel Gain Tracking			± 0.1		%
THD+N	Total Harmonic Distortion Plus Noise (Note 5)	R _L =32Ω, P _{OUT} =100mW, f _{IN} =1kHz		0.03		%
		R _L =16Ω, P _{OUT} =80mW, f _{IN} =1kHz		0.03		
V _{UVLH}	Power Supply Start-up Threshold Voltage			2		V
V _{UVLL}	Power Supply Shut-down Threshold Voltage			1.8		
OT	Thermal Shutdown			150		°C
	Thermal Shutdown Hysteresis			20		

Electrical Characteristics (continued)

($V_{DD}=5V$, $PGND=SGND$, $\overline{SHDN}=5V$, $C1=C2=1\mu F$, $R_L=\infty$, resistive load reference to ground; gain= -1.5V/V, $T_A=-40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A=25^\circ C$.) (Note 3)

Symbol	Parameter	Conditions	EUA6211			Unit
			Min.	Typ.	Max.	
SNR	Signal-to-Noise Ratio	$R_L=1k\Omega$, $BW=22Hz$ to $22kHz$		102		dB
		$V_{OUT}=2V_{RMS}$ A-Weighted		105		
		$R_L=32\Omega$, $BW=22Hz$ to $22kHz$		98		
		$P_{OUT}=45mW$ A-Weighted		101		
	Crosstalk	L to R, R to L, $f=10kHz$, $R_L=16\Omega$, $P_{OUT}=15mW$		-75		dB
f_{OSC}	Charge-Pump Oscillator Frequency		190	280	400	kHz
DIGITAL INPUTS (\overline{SHDN})						
VINH	Input-Voltage High		1.4			V
VINL	Input-Voltage Low				0.4	V
	Input Leakage Current				± 1	μA

Electrical Characteristics

($V_{DD}=3V$, $PGND=SGND$, $\overline{SHDN}=3V$, $C1=C2=1\mu F$, $R_L=\infty$, resistive load reference to ground; gain= -1.5V/V, $T_A=-40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A=25^\circ C$.) (Note 3)

Symbol	Parameter	Conditions	EUA6211			Unit
			Min.	Typ.	Max.	
I_{CC}	Quiescent Current			2.7		mA
I_{SHDN}	Shutdown Current	$\overline{SHDN}=SGND=PGND$		0.1	1	μA
PSRR	Power-Supply Rejection Ratio (Note 4)	$f=1kHz$, $100mV_{P-P}$		77		dB
		$f=20kHz$, $100mV_{P-P}$		60		
P_{OUT}	Output Power	$R_L=32\Omega$, $THD+N=1\%$		40		mW
		$R_L=16\Omega$, $THD+N=1\%$		30		
THD+N	Total Harmonic Distortion Plus Noise (Note 5)	$R_L=32\Omega$, $P_{OUT}=30mW$, $f_{IN}=1kHz$		0.03		%
		$R_L=16\Omega$, $P_{OUT}=30mW$, $f_{IN}=1kHz$		0.03		

Electrical Characteristics (for Line Driver Application)

($V_{DD}=3.3V$, $PGND=SGND$, $\overline{SHDN}=3.3V$, $C1=C2=1\mu F$, $R_L=10k\Omega$, resistive load reference to ground; gain= -1.5V/V, $T_A=-40^\circ C$ to $+85^\circ C$, unless otherwise noted. Typical values are at $T_A=25^\circ C$.) (Note 3)

Symbol	Parameter	Conditions	EUA6211			Unit
			Min.	Typ.	Max.	
V_O	Output Voltage, Outputs in Phase	1% THD+N, $f=1kHz$, $10k\Omega$ load		2.3		Vrms
I_{CC}	Quiescent Current			2.8	4.5	mA
THD+N	Total Harmonic Distortion Plus	$f=1kHz$, $10k\Omega$ load, $V_O=2V_{rms}$		0.03%		
SNR	Signal-to-Noise Ratio	A-weighted, $2V_{rms}$ ref		105		dB
DNR	Dynamic Range	A-weighted, $2V_{rms}$ ref		105		dB
V_n	Noise Voltage	A-weighted		10		μV
Z_o	Output Impedance when Muted	$\overline{SHDN}=GND$		15		$k\Omega$
	Input-to-Output Attenuation	1 Vrms, 1kHz Input		67		dB
	Slew Rate			5		V/ μs
	Crosstalk-Line L-R and R-L	$10k\Omega$ load, $V_O=2V_{rms}$		-120		dB
Ilimit	Current Limit	$V_{DD}=3.3V$		200		mA

Note 3: All specifications are 100% tested at $T_A = +25^\circ C$; temperature limits are guaranteed by design.

Note 4: The amplifier inputs are AC-coupled to GND.

Note 5: Measurement bandwidth is 22Hz to 22kHz.

Typical Operating Characteristics

($V_{DD}=5V$, $PGND=SGND=0V$, $\overline{SHDN}=V_{DD}$, $C1=C2=1\mu F$, $R_L=R_R$, gain=-1.5V/V, THD+N measurement bandwidth=22Hz to 22kHz, both outputs driven in phase, $T_A=+25^\circ C$, unless otherwise noted.)

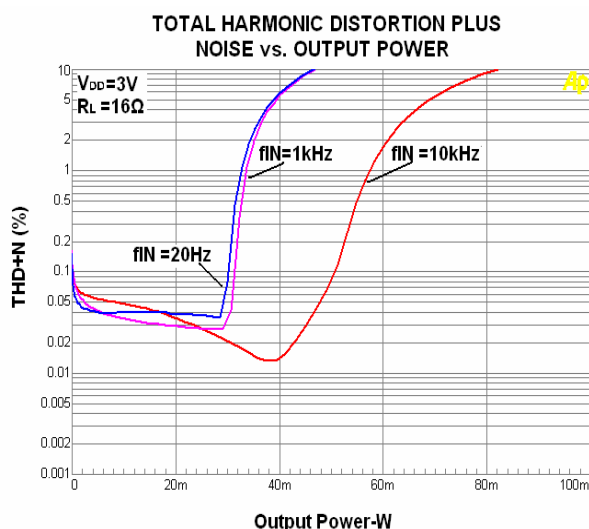


Figure4.

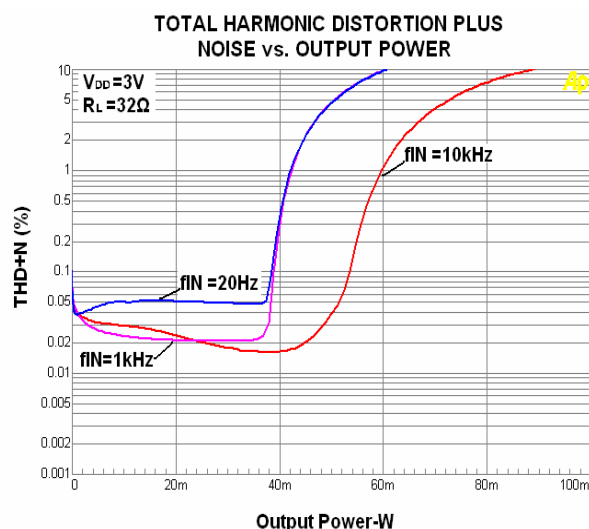


Figure5.

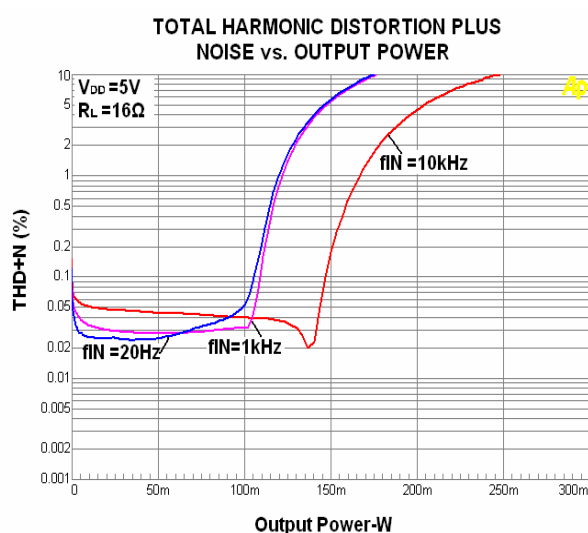


Figure6.

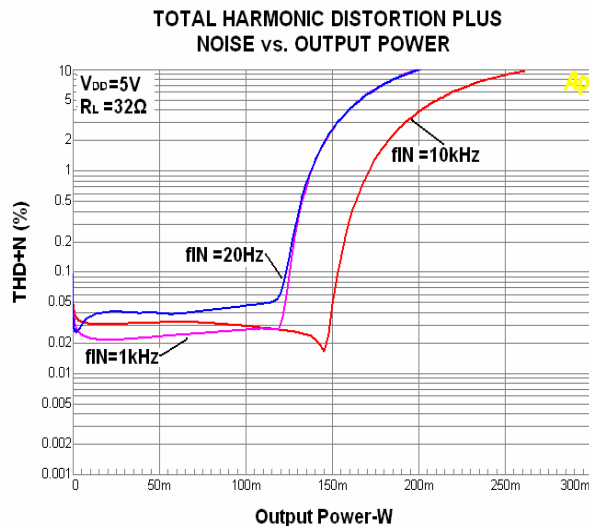


Figure7.

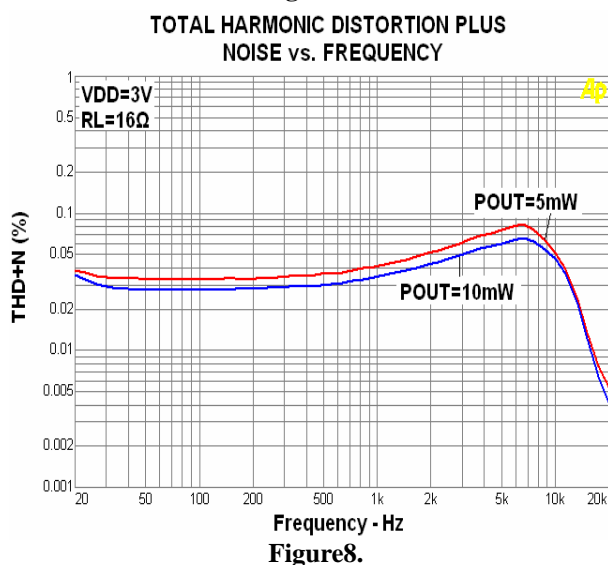


Figure8.

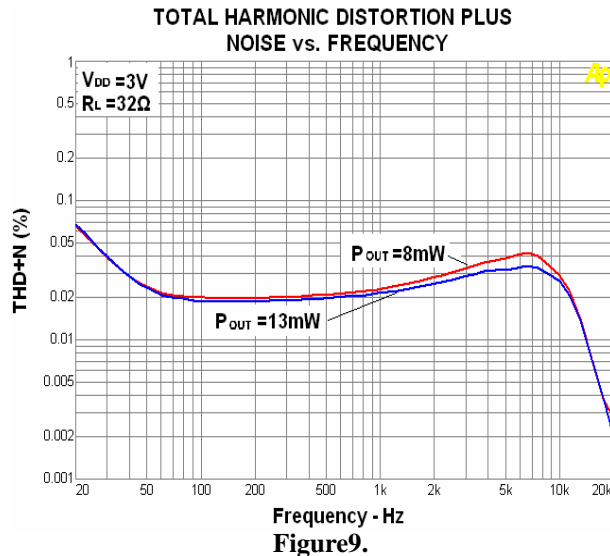


Figure9.

Typical Operating Characteristics (continued)

($V_{DD}=5V$, $PGND=SGND=0V$, $\overline{SHDN}=V_{DD}$, $C1=C2=1\mu F$, $R_L=R_R$, $gain=-1.5V/V$, THD+N measurement bandwidth=22Hz to 22kHz, both outputs driven in phase, $T_A=+25^\circ C$, unless otherwise noted.)

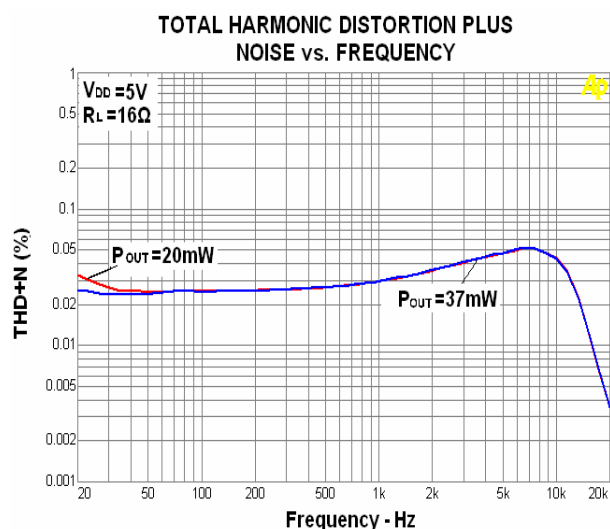


Figure10.

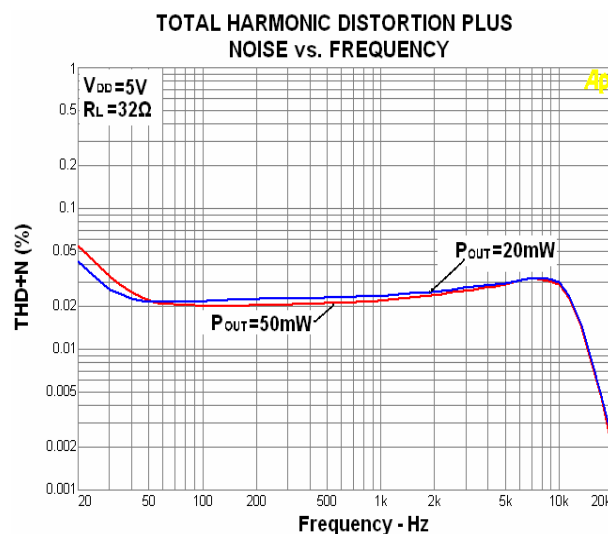


Figure11.

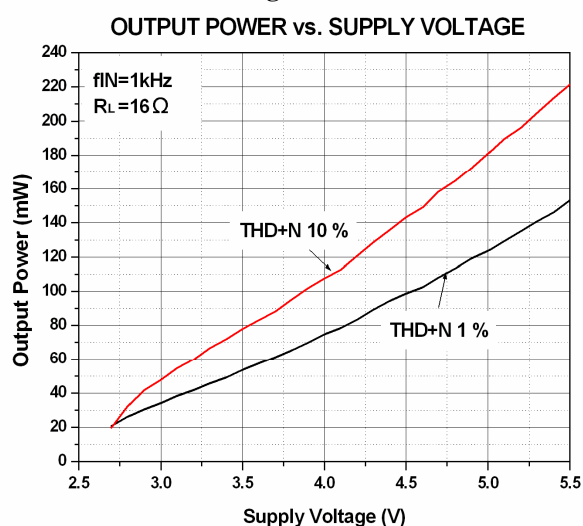


Figure12.

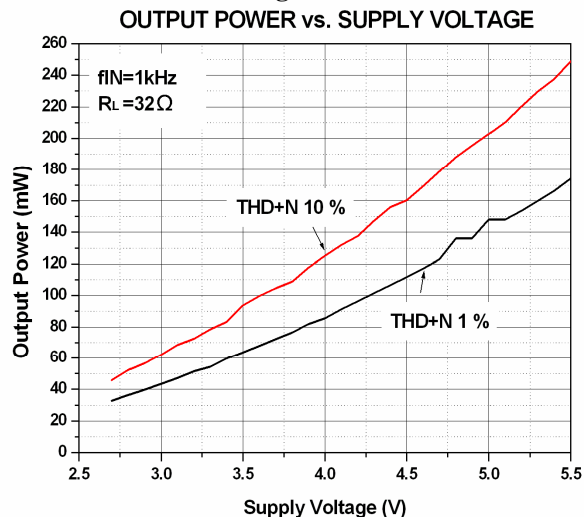


Figure13.

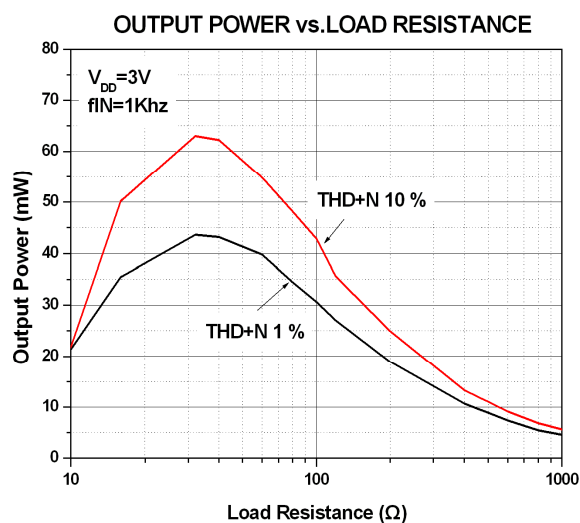


Figure14.

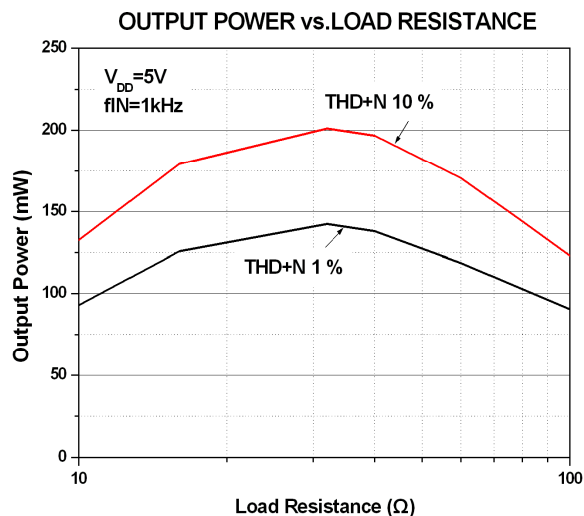


Figure 15.

Typical Operating Characteristics (continued)

($V_{DD}=5V$, $PGND=SGND=0V$, $\overline{SHDN}=V_{DD}$, $C1=C2=1\mu F$, $R_L=R_R$, gain=-1.5V/V, THD+N measurement bandwidth=22Hz to 22kHz, both outputs driven in phase, $T_A=+25^\circ C$, unless otherwise noted.)

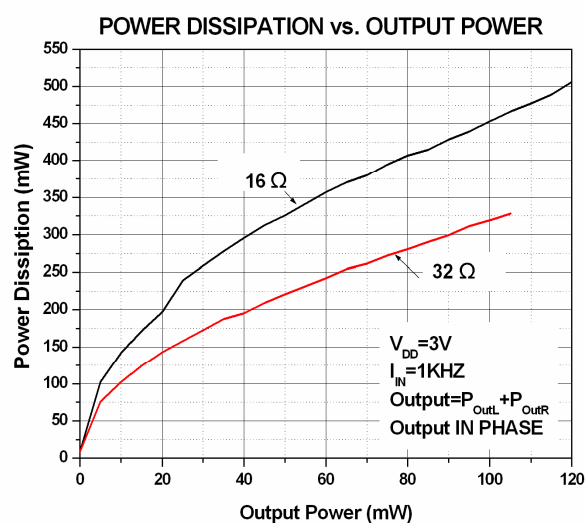


Figure16.

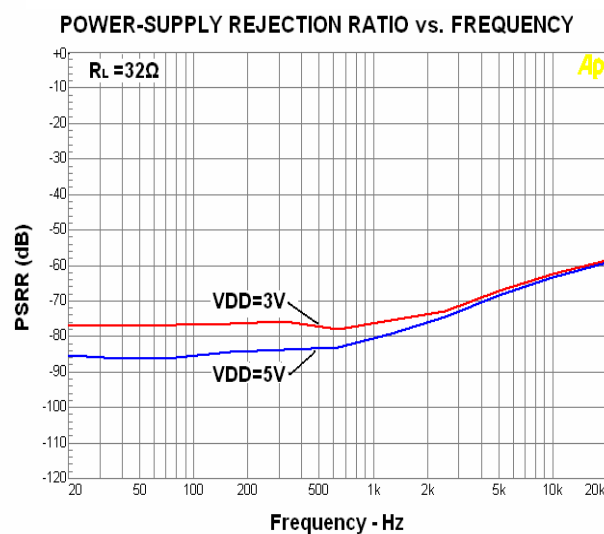


Figure17.

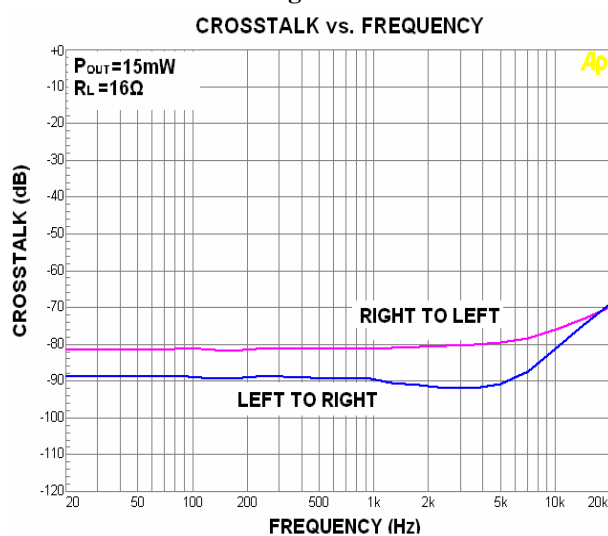


Figure18.

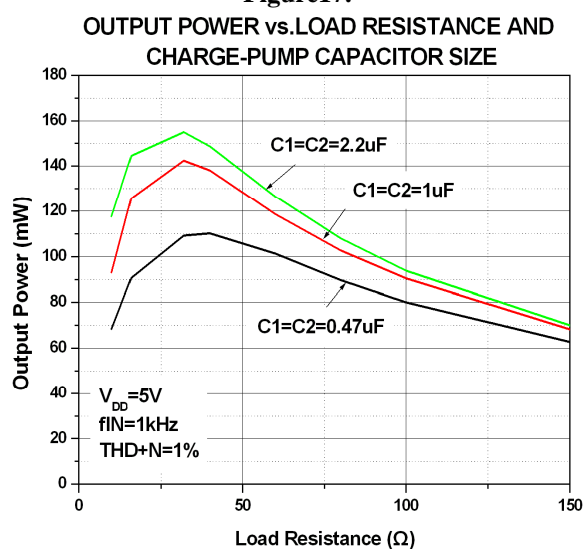


Figure19.

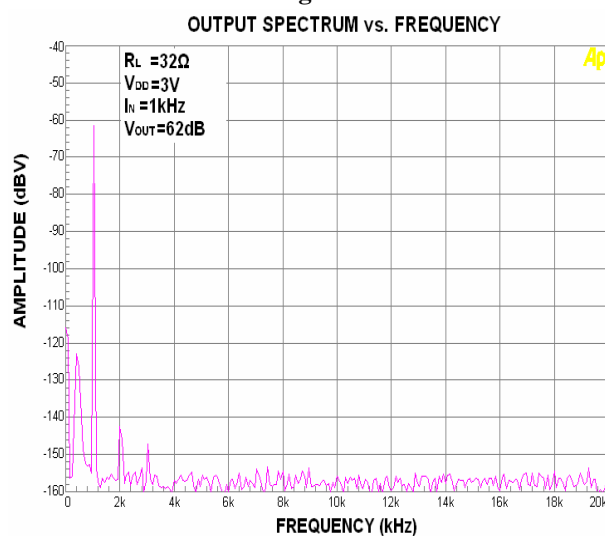


Figure20.

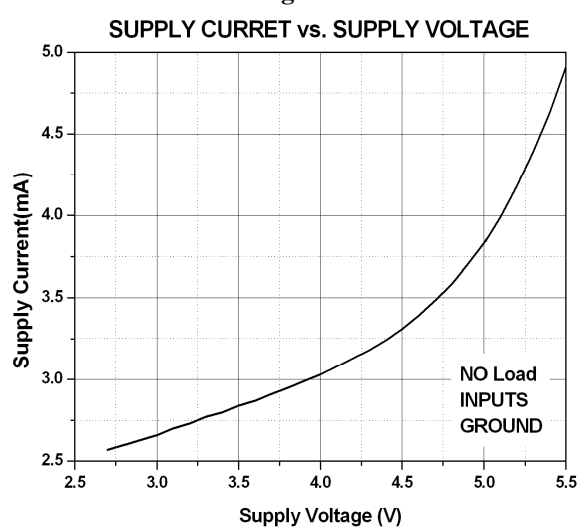


Figure21.

Typical Operating Characteristics (continued)

($V_{DD}=5V$, $PGND=SGND=0V$, $\overline{SHDN}=V_{DD}$, $C1=C2=1\mu F$, $R_L=R_R$, gain=-1.5V/V, THD+N measurement bandwidth=22Hz to 22kHz, both outputs driven in phase, $T_A=+25^\circ C$, unless otherwise noted.)

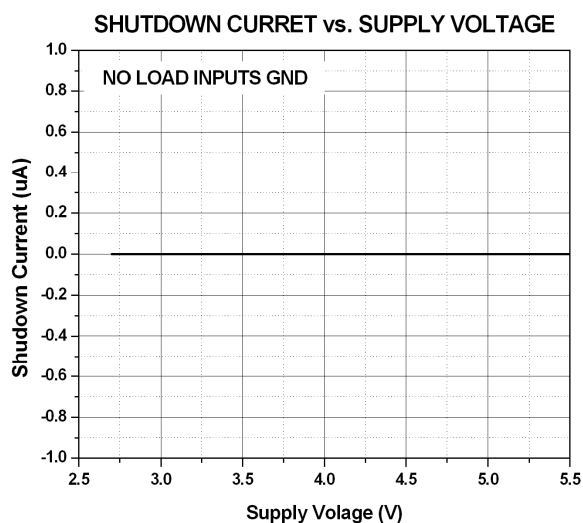


Figure22.

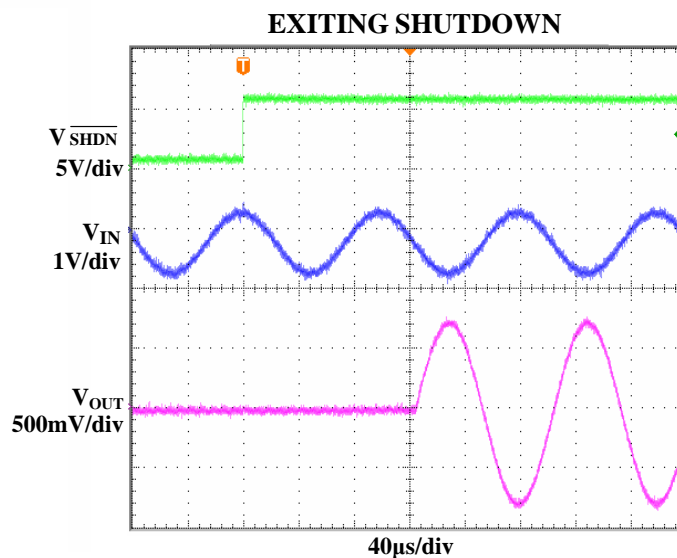


Figure23.

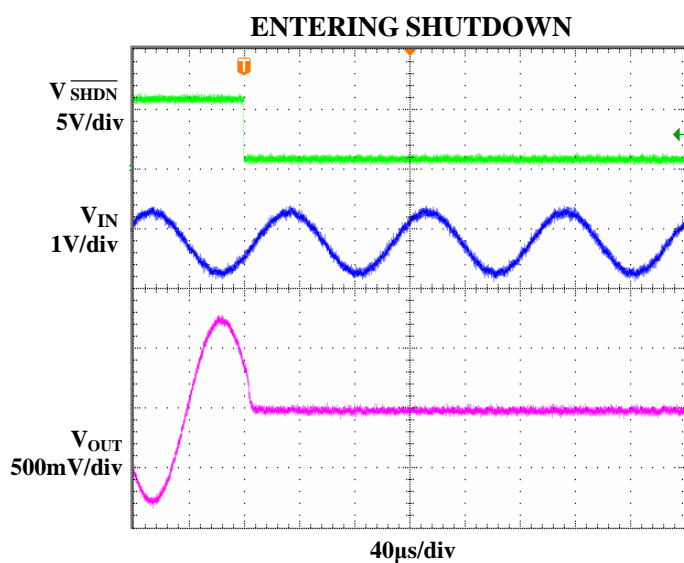


Figure24.

Typical Operating Characteristics (for Line Driver Application)

($V_{DD}=3.3V$, $PGND=SGND=0V$, $\overline{SHDN}=V_{DD}$, $C1=C2=1\mu F$, $R_L=R_R$, gain=-1.5V/V, both outputs driven in phase, $T_A=+25^\circ C$, unless otherwise noted.)

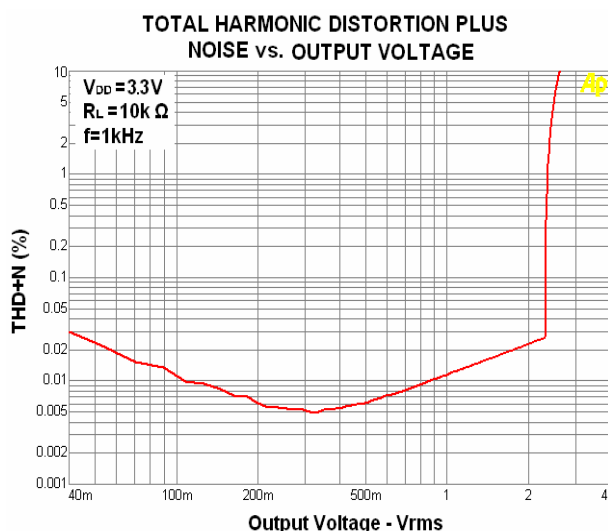


Figure25.

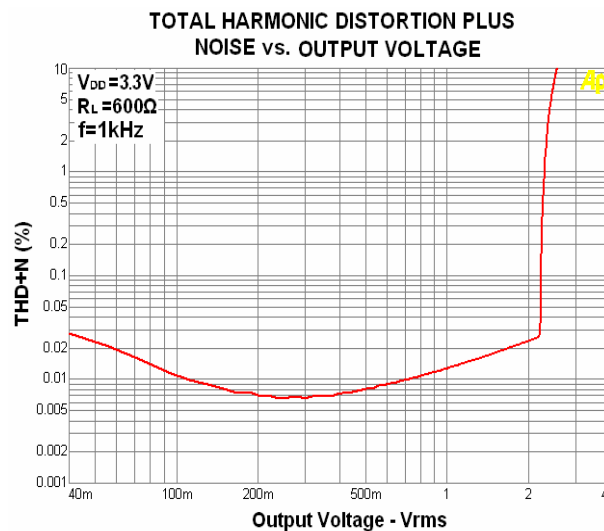


Figure26.

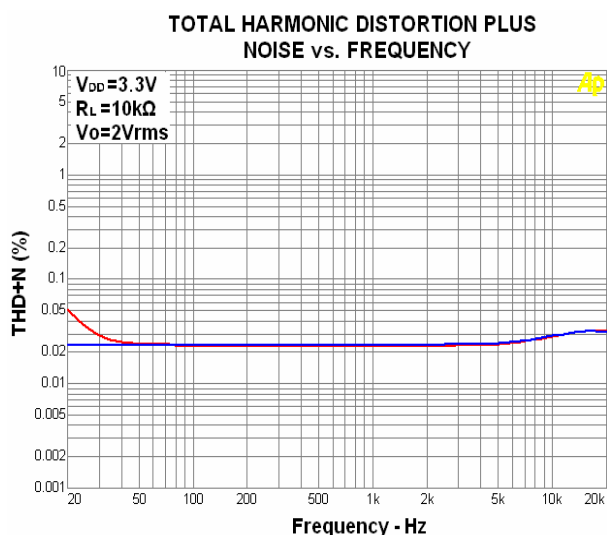


Figure27.

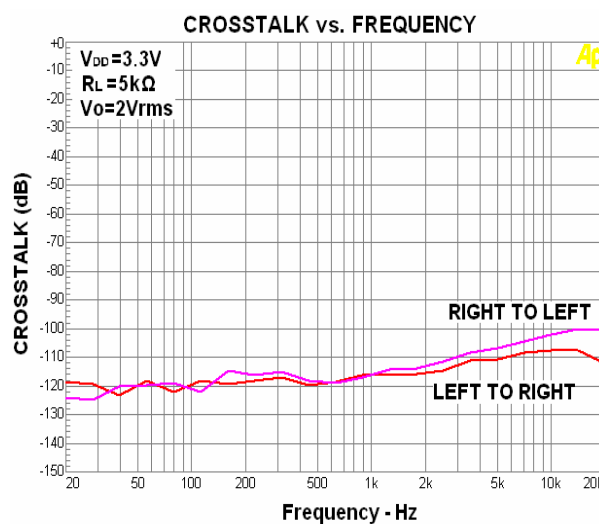


Figure28.

Detail Description

The EUA6211 is a stereo headphone amplifier with a unique ground architecture. This architecture creates an output waveform (Figure 29) which eliminates the need to use 2 external big capacitors required by conventional headphone amplifiers.

The structure of the EUA6211 is basically composed of 2 ground referenced amplifiers, a charge pump, an UVLO, a short circuit protection and also a thermal shutdown. A special circuitry is embedded to eliminate any pop and click noise that occurs during turn on and turn off time.

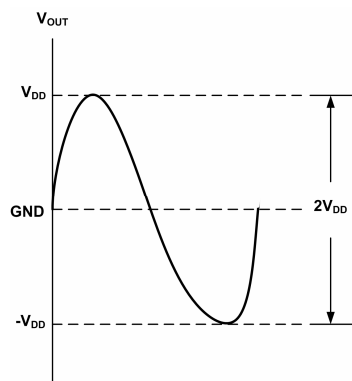


Figure 29. Output Waveform

Charge Pump

The EUA6211 features a low-noise charge pump. The 280kHz switching frequency is well beyond the audio range and does not interfere with audio signals. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. Additional high-frequency noise attenuation can be achieved by increasing the value of C2 (see the Typical Application Circuit).

Click-and-Pop Suppression

In conventional single-supply audio amplifiers, the output-coupling capacitor contributes significantly to audible clicks and pops. Upon startup, the amplifier charges the coupling capacitor to its bias voltage, typically half the supply. Likewise, on shutdown, the capacitor is discharged. This results in a DC shift across the capacitor, which appears as an audible transient at the speaker. Since the EUA6211 does not require output-coupling capacitors, this problem does not arise. Additionally, the EUA6211 features extensive click-and-pop suppression that eliminates any audible transient sources internal to the device.

Shutdown

The EUA6211 features a $< 0.1\mu\text{A}$, low-power shutdown mode that reduces quiescent current consumption and extends battery life for portable applications. Drive $\overline{\text{SHDN}}$ low to disable the device and the charge pump. In shutdown mode, the amplifier output impedance is set to $15\text{k}\Omega \parallel \text{RF}$. The amplifiers and charge pump are enabled once $\overline{\text{SHDN}}$ is driven high.

Application Information

Power Dissipation

Under normal operating conditions, linear power amplifiers can dissipate a significant amount of power. The maximum power dissipation for each package is given in the Absolute Maximum Ratings section under Continuous Power Dissipation or can be calculated by the following equation:

$$P_{\text{DISSPKG (MAX)}} = \frac{T_{\text{J(MAX)}} - T_{\text{A}}}{\theta_{\text{JA}}}$$

where $T_{\text{J(MAX)}}$ is $+150^{\circ}\text{C}$, T_{A} is the ambient temperature, and θ_{JA} is the reciprocal of the derating factor in $^{\circ}\text{C/W}$ as specified in the Absolute Maximum Ratings section.

Maximum Output Swing

$V_{\text{DD}} < 4.35\text{V}$

If the output load impedance is greater than $1\text{k}\Omega$, the EUA6211 can swing within a few millivolts of its supply rail. For example, with a 3.3V supply, the output swing is $2V_{\text{RMS}}$, or 2.83V peak while maintaining a low 0.03% THD+N. If the supply voltage drops to 3V, the same 2.83V peak has only 0.05% THD+N.

$V_{\text{DD}} > 4.35\text{V}$

Internal device structures limit the maximum voltage swing of the EUA6211 when operated at supply voltages greater than 4.35V. The output must not be driven such that the peak output voltage exceeds the opposite supply voltage by 9V. For example, if $V_{\text{DD}} = 5\text{V}$, the charge pump sets $PV_{\text{SS}} = -5\text{V}$. Therefore, the peak output swing must be less than $\pm 4\text{V}$ to prevent exceeding the absolute maximum ratings.

UVLO

The EUA6211 features an undervoltage lockout (UVLO) function that prevents the device from operating if the supply voltage is less than 2.5V. This feature ensures proper operation during brownout conditions and prevents deep battery discharge. Once the supply voltage exceeds the UVLO threshold, the EUA6211 charge pump is turned on and the amplifiers are powered, provided that $\overline{\text{SHDN}}$ is high.

Component Selection

Input-Coupling Capacitor

The input capacitor (C_{IN}), in conjunction with the input resistor (R_{IN}), forms a highpass filter that removes the DC bias from an incoming signal (see the Typical Application Circuit). The AC-coupling capacitor allows the device to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3\text{dB}} = \frac{1}{2\pi R_{\text{IN}} C_{\text{IN}}}$$

Choose the C_{IN} such that f_{-3dB} is well below the lowest frequency of interest. Setting f_{-3dB} too high affects the device's low-frequency response. Use capacitors whose dielectrics have low-voltage coefficients, such as tantalum or aluminum electrolytic. Capacitors with high-voltage coefficients, such as ceramics, can result in increased distortion at low frequencies.

Charge-Pump Capacitor Selection

Use ceramic capacitors with a low ESR for optimum performance. For optimal performance over the extended temperature range, select capacitors with an X7R dielectric.

Flying Capacitor (C1)

The value of the flying capacitor (see the Typical Application Circuit) affects the charge pump's load regulation and output resistance. A C1 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C1 improves load regulation and reduces the charge-pump output resistance to an extent. See the Output Power vs. Load Resistance and Charge-Pump Capacitor Size graph in the Typical Operating Characteristics. Above 1 μ F, the on-resistance of the switches and the ESR of C1 and C2 dominate.

Hold Capacitor (C2)

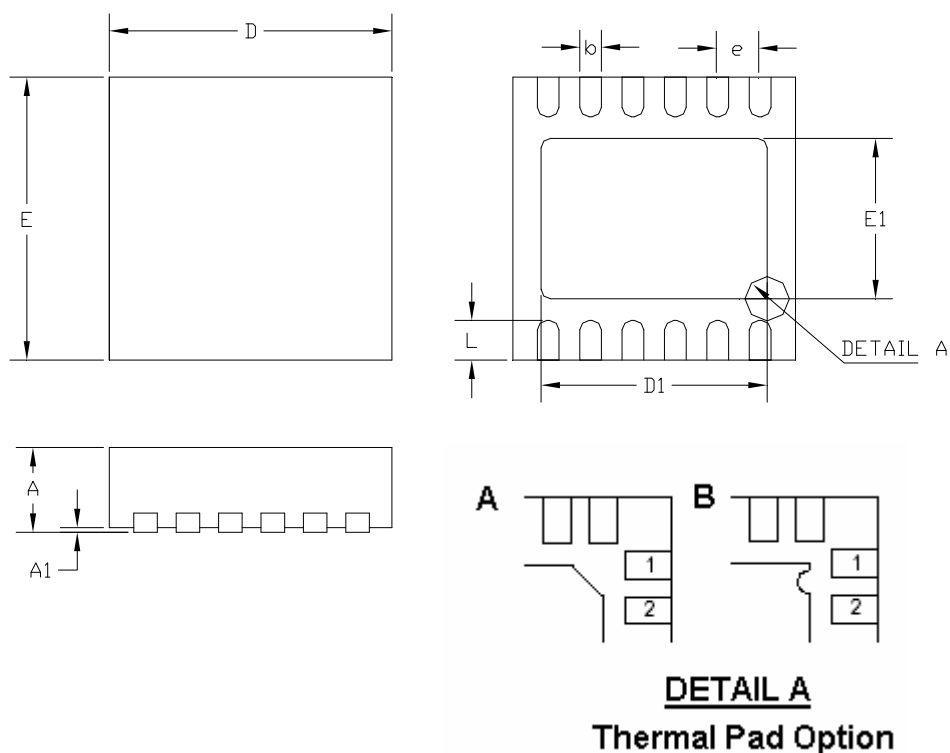
The hold capacitor value (see the Typical Application Circuit) and ESR directly the ripple at PV_{SS} . Increasing the value of C2 reduces output ripple. Likewise, decreasing the ESR of C2 reduces both ripple and output resistance. Lower capacitance values can be used in systems with low maximum output power levels. See the Output Power vs. Load Resistance and Charge-Pump Capacitor Size graph in the Typical Operating Characteristics.

Power-Supply Bypass Capacitor (C3)

The power-supply bypass capacitor (see the Typical Application Circuit) lowers the output impedance of the power supply, and reduces the impact of the EUA6211's charge-pump switching transients. Bypass V_{DD} with C3, the same value as C1, and place it physically close to the V_{DD} and PGND pins.

Amplifier Gain

The gain of the EUA6211 amplifier is internally set to -1.5V/V. All gain-setting resistors are integrated into the device, reducing external component count. The internally set gain, results in a headphone amplifier that requires only five small capacitors to complete the amplifier circuit: two for the charge pump, two for audio input coupling, and one for power-supply bypassing (see the Typical Application Circuit).

Packaging Information**TDFN-12**

Note: Exposed pad outline drawing is for reference only.

SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	0.70	0.75	0.80	0.028	0.029	0.031
A1	0.00	-	0.05	0.000	-	0.002
b	0.15	-	0.30	0.006	-	0.012
E	2.90	3.00	3.10	0.114	0.118	0.122
D	2.90	3.00	3.10	0.114	0.118	0.122
D1	2.30	2.50	2.65	0.091	0.098	0.104
E1	1.40	1.60	1.75	0.055	0.063	0.069
e	0.45 REF			0.018 REF		
L	0.30	0.40	0.50	0.012	0.016	0.020