60V, 3A, Asynchronous Step-Down Converter with Programmable Frequency

DESCRIPTION

The EUP3253 is a 60V, 3A, step down regulator with an integrated high side MOSFET. The EUP3253 adopting the peak current mode control, supports the PSM mode which assists the converter on achieving high efficiency at light load or standby condition.

The EUP3253 features programmable switching frequency from 100 kHz to 2MHz with an external resistor, which provides the flexibility to optimize either efficiency or external component size. The converter supports external clock synchronization with a frequency band from 160 kHz to 2MHz. The EUP3253 allows power conversion from high input voltage to low output voltage with a minimum 130ns on-time of high-side MOSFET.

Fault protection includes secondary cycle-by-cycle current limit, short circuit protection and thermal shutdown. Internal soft-start minimizes the inrush supply current and the output overshoot at initial startup.

The EUP3253 is available in an 8-pin SOP-8(EP) package.

FEATURES

- Wide Input Voltage Range: 4.5V to 60V
- High Efficiency at Light Loads with PSM Mode
- 150μA Operating Quiescent Current
- 3μA Shutdown Current
- 100kHz to 2MHz Fixed Switching Frequency
- Synchronizes to External Clock
- Adjustable UVLO Voltage and Hysteresis
- 0.8V 1% Internal Voltage Reference
- Internal Soft-start
- Short Circuit Protection
- Thermal Shutdown
- SOP-8(EP) Package

APPLICATIONS

- Vehicle Accessories : GPS, Entertainment
- 12-V, 24-V, 48-V Industrial, Automotive and Communications Power Systems
- USB Dedicated Charging Ports and Battery Chargers

Typical Application Circuit

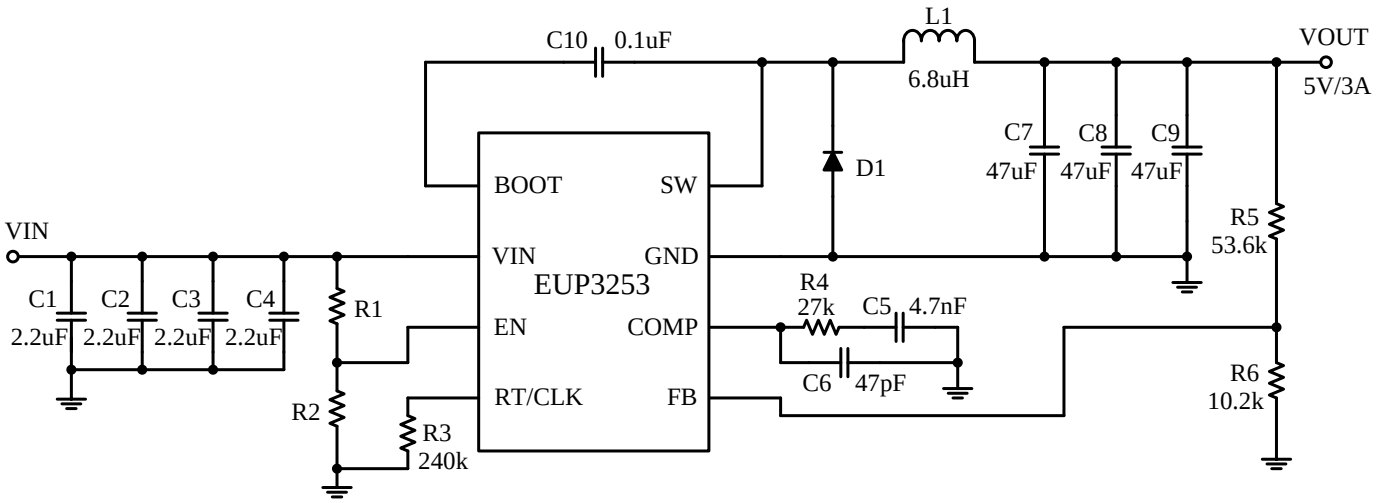
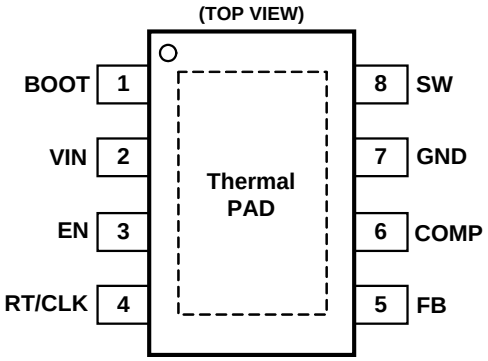


Figure 1. Application Circuit

Pin Configurations

Package Type	Pin Configurations
EUP3253 SOP-8 (EP)	

Pin Description

Pin	Pin Name	Description
1	BOOT	A bootstrap capacitor is required between BOOT and SW. If the voltage on this capacitor is below the minimum required to operate the high side MOSFET, the output is switched off until the capacitor is refreshed.
2	VIN	Input Supply Pin. Drive VIN with a 4.5V to 60V power source. Bypass VIN to GND with a suitably large capacitor to minimize input ripple to the IC.
3	EN	Enable Input. Drive EN high or floating to turn on the regulator; low to turn it off. Adjust the input under voltage lockout with two resistors.
4	RT/CLK	Set the internal oscillator clock frequency or synchronize to an external clock. Connect a resistor from this pin to ground to set switching frequency. An external clock can be input directly to the RT/CLK pin. The internal oscillator synchronizes to the external clock frequency with PLL.
5	FB	Output Feedback Input. FB senses the output voltage and regulates it. Drive FB with a resistive voltage divider connected to it from the output voltage.
6	COMP	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this terminal.
7	GND	Ground.
8	SW	Power switching output. The source of the internal high-side power MOSFET, Connect the output LC filter from SW to the output load.
9	Thermal Pad	Exposed pad. Must be connected to ground plane on PCB for proper operation and optimized thermal performance.

Ordering Information

Order Number	Package Type	Marking	Quantity per Reel	Operating Temperature Range
EUP3253WIR1	SOP-8 (EP)	xxxxx P3253	2500	-40 °C to +85°C

EUP3253 □ □ □ □

- Lead Free Code
  1: Lead Free, Halogen-Free
- Packing
  R: Tape & Reel
- Operating temperature range
  I: Industry Standard
- Package Type
  W: SOP8 (EP)

Block Diagram

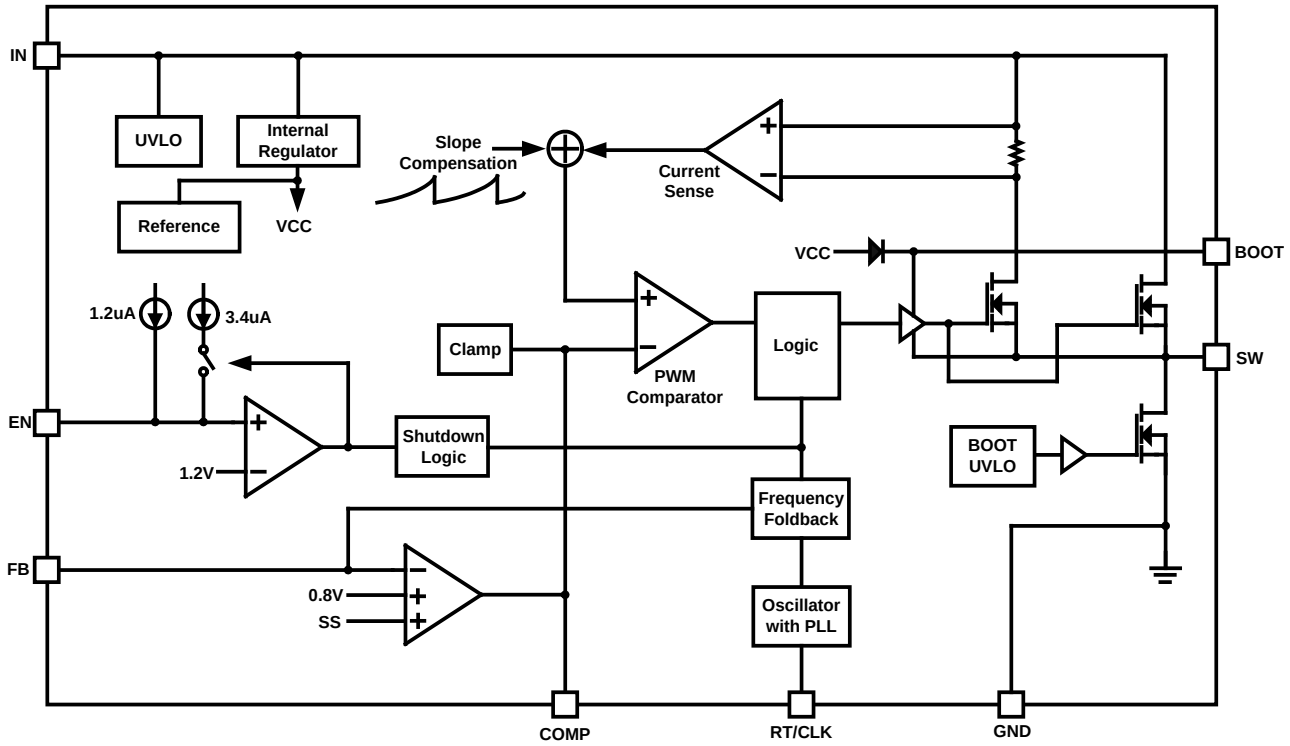


Figure 2. Functional Block Diagram

Absolute Maximum Ratings(1)

- Input Voltage (V_{IN}) ---------- -0.3V to 65V
- Enable Voltage (V_{EN}) ---------- -0.3V to 8V
- BOOT to SW (BOOT−SW) ---------- -0.3V to 6V
- All Other Pins ---------- -0.3V to 6V
- Junction Temperature ---------- 150°C
- Storage Temperature ---------- -65°C to +150°C
- Lead Temp(Soldering, 10sec) ---------- 260°C
- Thermal Resistance θ_{JA} SOP8(EP) ---------- 60°C/W
- Thermal Resistance θ_{JC} SOP8(EP) ---------- 20°C/W

Recommend Operating Conditions(2)

- Supply Voltage (V_{IN}) ---------- 4.5V to 60V
- Ambient Operating Temperature ---------- -40°C to +85°C

Note(1):Stress beyond those listed under "Absolute Maximum Ratings" may damage the device.
Note(2):The device is not guaranteed to function outside the recommended operating conditions.

Electrical Characteristics

(VIN=12V, T_A=25℃, unless otherwise specified.)

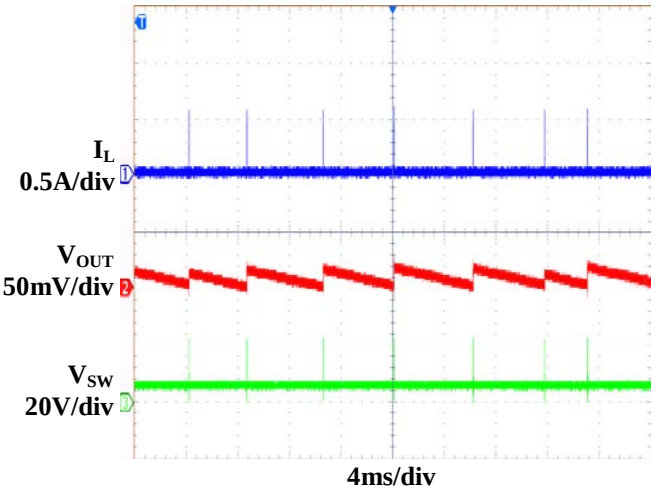
Parameter	Conditions	EUP3253			Unit
		Min	Typ	Max	
Operating input voltage		4.5		60	V
VIN UVLO threshold	Rising	4.0	4.3	4.48	V
VIN UVLO threshold hysteresis			320		mV
Shutdown supply current	EN=0V		3	5	μA
Non-switching supply current	FB=0.9V		150	200	
EN threshold voltage		1.1	1.2	1.3	V
EN Input current	EN threshold +0.2V		-4.6		μA
	EN threshold -0.2V		-1.2		
EN Hysteresis current			-3.4		μA
Voltage reference		0.792	0.8	0.808	V
On-resistance		55	103	200	mΩ
COMP to SW current trans-conductance			15		A/V
Current limit threshold			5.2		A
Thermal shutdown			170		℃
Thermal shutdown hysteresis			40		℃
Switching frequency range using RT		100		2000	kHz
Switching frequency F_{SW}	RT=200KΩ	450	500	550	kHz
Switching frequency range using CLK		160		2000	kHz
RT/CLK high threshold			1.55	2	V
RT/CLK low threshold		0.5	1.2		V
Minimum on time			130		ns
Soft start time	RT=200KΩ		2		ms

Typical Operating Characteristics

T_A=25°C, V_{IN}=24V, V_{OUT}=5V, unless otherwise specified.

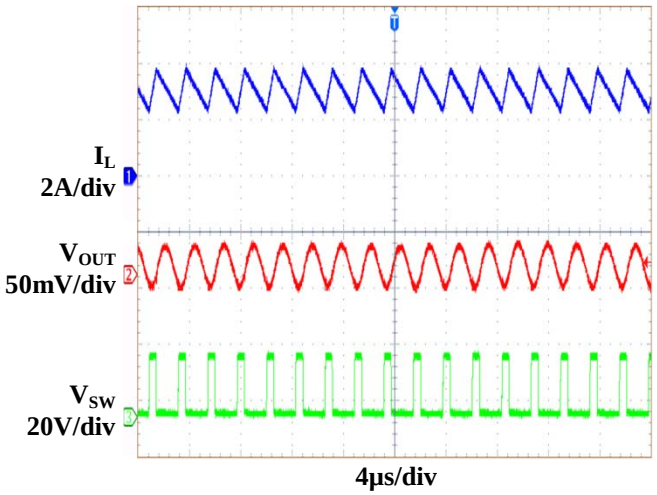
Steady State

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=0A



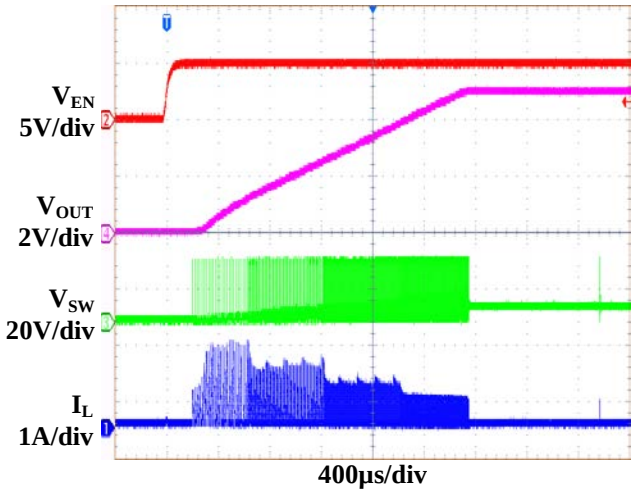
Steady State

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=3A



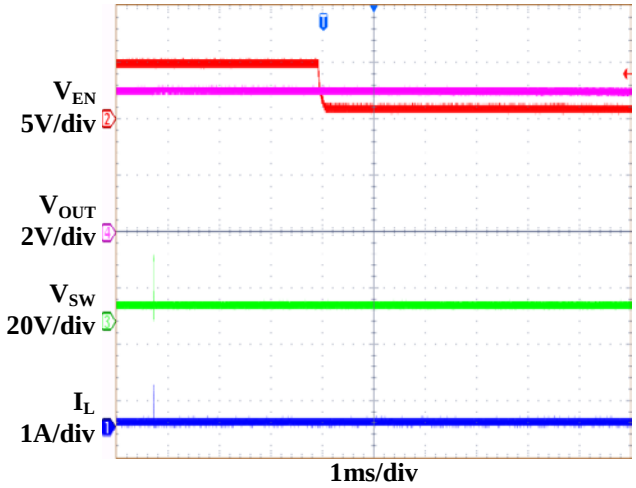
Startup through EN

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=0A



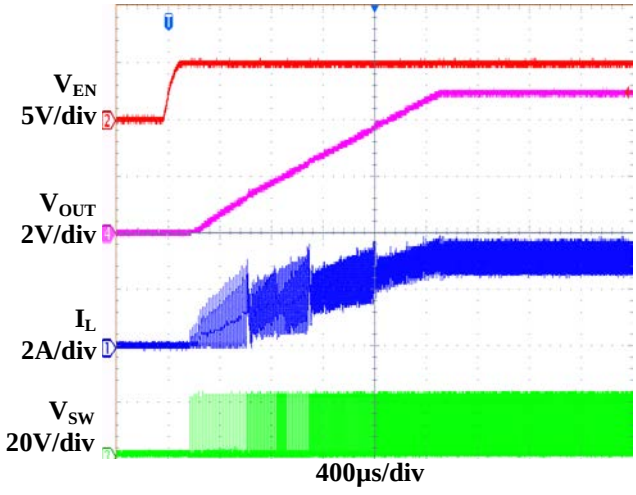
Shutdown through EN

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=0A



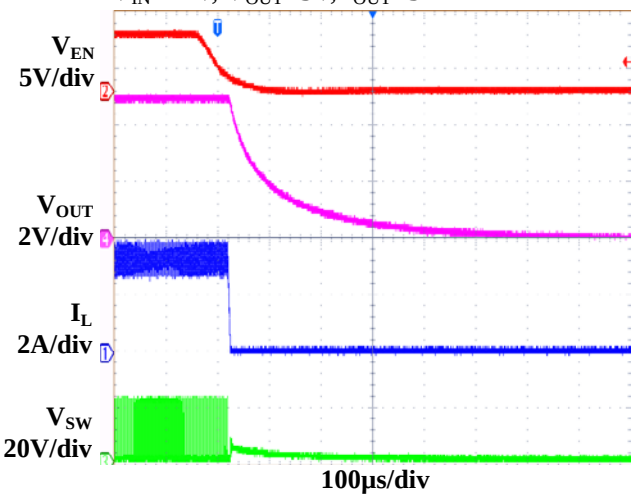
Startup through EN

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=3A



Shutdown through EN

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=3A

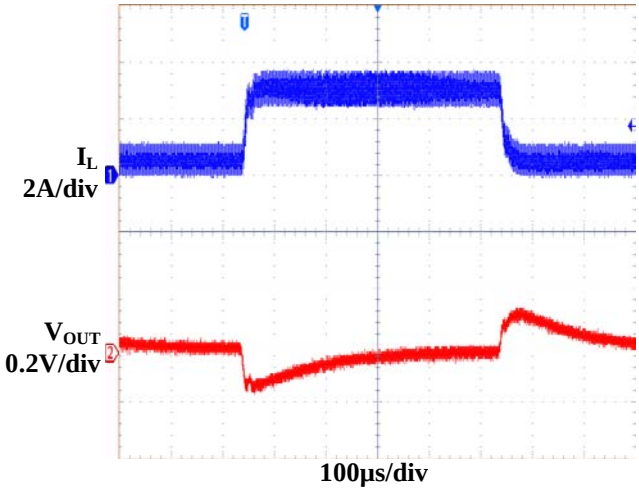


Typical Operating Characteristics

T_A=25°C, V_{IN}=24V, V_{OUT}=5V, unless otherwise specified.

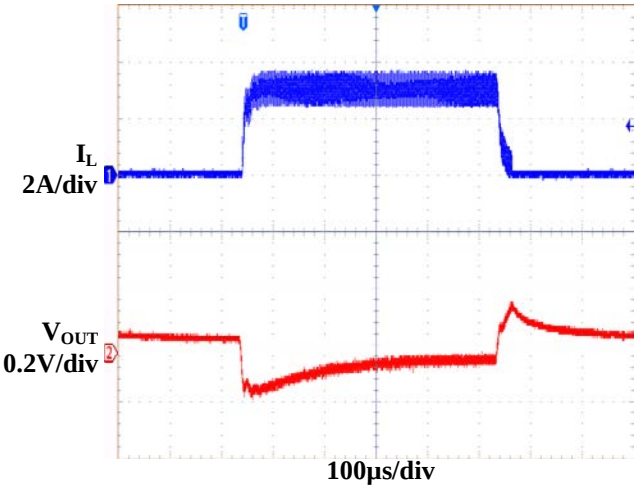
Load Transient Response

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=0.5A to 3A



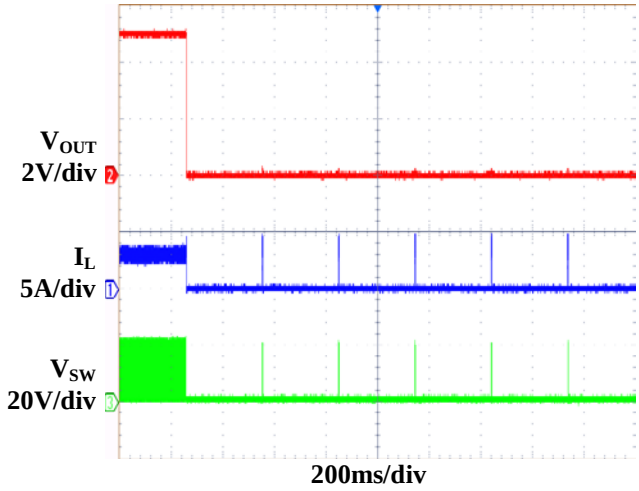
Load Transient Response

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=0A to 3A



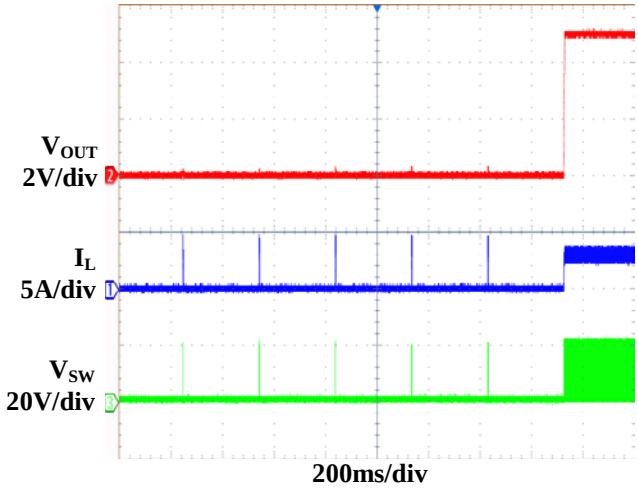
Short Circuit

V_{IN}=24V, V_{OUT}=5V, I_{OUT}=3A

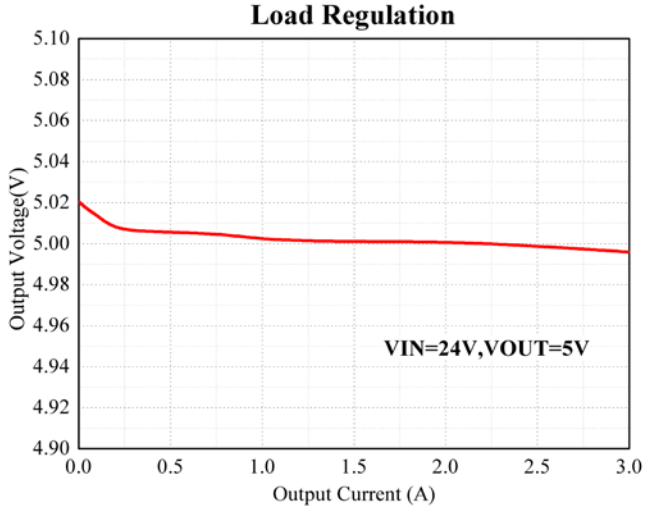


Short Circuit Recovery

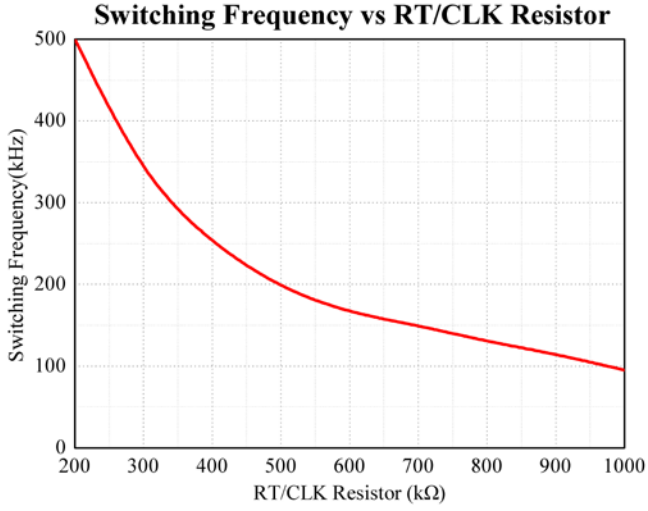
V_{IN}=24V, V_{OUT}=5V, I_{OUT}=3A



Load Regulation

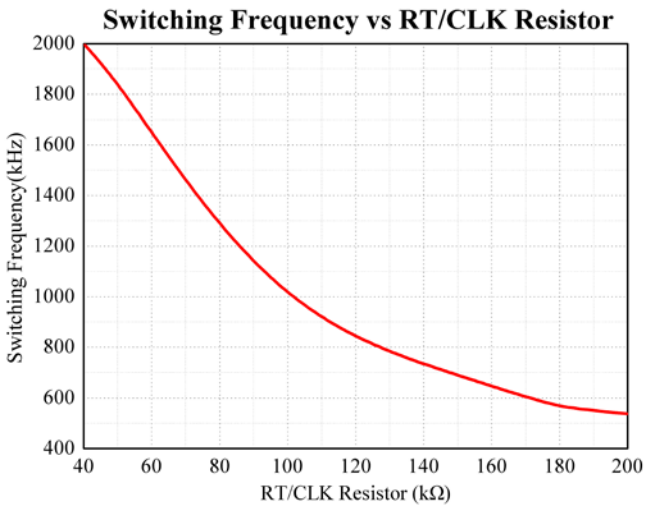


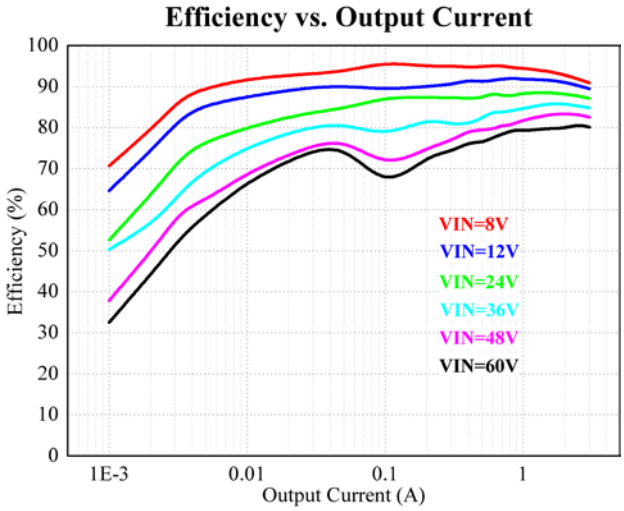
Switching Frequency vs RT/CLK Resistor



Typical Operating Characteristics

T_A=25°C, V_{IN}=24V, V_{OUT}=5V, unless otherwise specified.





Functional Description

The EUP3253 is a 60V, 3A high efficiency asynchronous step-down converter. It utilizes the peak current mode control. Current mode control provides simple external compensation and flexible component selection. A low ripple pulse skip mode reduces the no load supply current to 150μA, 3μA shutdown current. A wide switching frequency range allows either efficiency or external component size to be optimized.

Peak Current Mode Control

The EUP3253 employs fixed frequency peak current mode control. An internal clock initiates turning on the high-side power MOSFET in each cycle, then inductor current rises linearly. When the current through high-side MOSFET reaches the threshold level set by the COMP voltage of the internal error amplifier, the integrated high-side MOSFET is turned off. The error amplifier serves the COMP node by comparing the voltage of the FB pin with an internal 0.8V reference voltage. When the load current increases, a reduction in the feedback voltage relative to the reference raises COMP voltage till the average inductor current matches the increased load current. This feedback loop well regulates the output voltage to the reference. The device also integrates an internal slope compensation circuitry to prevent sub-harmonic oscillation when duty cycle is greater than 50% for a fixed frequency peak current mode control.

Pulse Skip Mode

The EUP3253 operates in Pulse Skipping Mode (PSM) with light load current to improve efficiency. When the load current decreases, the feedback voltage leads COMP voltage drop. When COMP falls to a low clamp threshold, device enters PSM. The output voltage decays due to output capacitor discharging during skipping period. Once FB voltage drops lower than the reference voltage and the COMP voltage rises above low clamp threshold. Then high-side power MOSFET turns on in next clock pulse.

After several switching cycles with typical peak inductor current, the COMP voltage drops and is clamped again. Pulse skipping mode repeats if the output continues light loaded. This control scheme helps achieving higher efficiency by skipping cycles to reduce switching power loss and gate drive charging loss. The controller consumption quiescent current is 150μA during skipping period with no switching to improve efficiency further.

Enable and Under Voltage Lockout Threshold

The EUP3253 provides an EN pin as an external chip enable control to enable or disable the device. If V_{EN} is held below the enable threshold voltage, switching is inhibited even if the VIN voltage is above VIN under-voltage lockout threshold (V_{UVLOH}). If V_{EN} is held below 1.2V, the converter will enter into shutdown mode. During shutdown mode, the supply current can be reduced to 3μA. If the EN voltage rises above the enable threshold voltage while the VIN voltage is higher than V_{UVLOH}, the device will be turned on. The EN terminal has an internal pull-up current source I_{EN} that enables operation of the EUP3253 when the EN terminal floats. The EN pin can be used to adjust the under-voltage lockout (UVLO) threshold and hysteresis by using two external divided resistors.

Soft-Start

The EUP3253 has internal soft start feature to minimize the inrush supply current and the output overshoot at initial startup. When the EUP3253 starts up, the internal reference voltage which is compared with V_{FB} ramps up gradually, so the output voltage ramps up as well. The soft start time is reverse proportion to the frequency. The soft start time is about 2ms for 500kHz switching frequency.

Switching Frequency and Synchronization

The EUP3253 provides a RT/SYNC pin for switching frequency selection. The switching frequency can be set by using external resistor and the switching frequency range is from 100 kHz to 2MHz. It can also be synchronized with an external clock ranging from 160kHz to 2MHz by RT/SYNC pin.

The EUP3253 implements a frequency fold back function to protect the device at over load or short circuited condition, especially higher switching frequency and input voltage. The switching frequency is divided by 8, 4, 2, and 1 as the FB terminal voltage ramps from 0 to 0.8 volts. The frequency fold back function increases the switching cycle period and provides more time for the inductor current to ramp down.

Bootstrap Voltage Regulator

An external bootstrap capacitor between BOOT pin and SW pin powers the floating gate driver to high-side power MOSFET. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1μF.

The UVLO of high-side MOSFET gate driver has rising threshold of 2.5V and hysteresis of 200mV. When the device operates with high duty cycle or extremely light load, bootstrap capacitor may be not recharged in considerable long time. The voltage at bootstrap capacitor is insufficient to drive high-side MOSFET fully on. When the voltage across bootstrap capacitor drops below 2.3V, BOOT UVLO occurs. The converter forces turning on an integrated low-side MOSFET periodically to refresh the voltage of bootstrap capacitor to guarantee the converter's operation over a wide duty range. Low-side MOSFET only turns on for 130ns in each refresh cycle to minimize the output voltage ripple.

Over-Temperature Protection

The EUP3253 includes an over-temperature protection

(OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold T_{SD}. Once the junction temperature cools down by a thermal shutdown hysteresis (ΔT_{SD}), the IC will resume normal operation with a complete soft-start.

Application Information

Setting the Output Voltage

The output voltage is set through a resistive voltage divider and can be expressed by the equation as follows:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R5}{R6}\right)$$

Inductor

The inductor is required to supply constant current to the load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will in turn result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and lower saturation current. A good rule for determining inductance is to allow the peak-to-peak ripple current to be approximately 30% of the maximum switch current limit. So, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, F_{LX} is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current. Choose an inductor that will not saturate under the maximum inductor peak current, calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \times F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where I_{LOAD} is the load current, the choice of which style inductor to use mainly depends on the price vs size requirements and any EMI constraints. In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device which is typically 5.2A. The most conservative approach is to choose an inductor with a saturation current rating greater than 5.2A. Because of the maximum I_{LP} limited by device, the maximum output current that the EUP3253 can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors are preferred, but tantalum or low-ESR electrolytic capacitors will also suffice. Choose X5R or X7R dielectrics when using ceramic capacitors. Since the input capacitor (C_{IN}) absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{CIN} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, where $I_{CIN} = I_{LOAD}/2$. For simplification, use an input capacitor with a RMS current rating greater than half of the maximum load current. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple for low ESR capacitors can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{C_{IN} \times F_{SW}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where C_{IN} is the input capacitance. For this example design, a ceramic capacitor with at least a 60V voltage rating is required to support the maximum input voltage.

Switching Frequency

Higher switching frequency support smaller profiles of output inductors and output capacitors, resulting in lower voltage and current ripples. However, the higher switching frequency causes extra switching loss, which downgrades converter's overall power efficiency and thermal performance. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage, the output voltage and the frequency fold back protection. The 130ns limitation of T_{ONMIN} also restricts the selection of higher switching frequency. In this design, a moderate switching frequency of 400 kHz is selected to achieve both small solution size and high efficiency operation.
The resistor connected from RT/CLK to GND sets switching frequency of the converter. The resistor value required for a desired frequency can be calculated using equation below, Where F_{SW} is the desired switching frequency.

$$R_T(K\Omega) = \frac{100000}{F_{SW}(KHz)}$$

Output Capacitor

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance. The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To

achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by equation below:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^2 \times L \times C_{OUT}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Where C_{OUT} is the output capacitance value and F_{SW} is the switching frequency. Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, four 47µF ceramic output capacitors work for most applications.

Bootstrap Capacitor Selection

The bootstrap capacitor between the BOOT pin and the SW pin is used to create a voltage rail above the applied input voltage. Specifically, the bootstrap capacitor is charged through an internal diode to an internal voltage source each time when the low-side freewheel diode conducts. The charge on this capacitor is then used to supply the required current during the remainder of the switching cycle. A 0.1µF ceramic capacitor must be connected between the BOOT and SW terminals for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Thermal Shutdown

The EUP3253 stops switching when its junction temperature exceeds 170°C and resumes when the temperature has dropped by 40°C to protect the device.

Layout Considerations

For all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade performance. When laying out the printed circuit board, the following guidelines should be used to ensure proper operation of the EUP3253.

1. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
2. The power traces, consisting of the GND trace, the SW trace and the VIN trace should be kept short, direct and wide.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
4. The compensation and feedback components must be connected as close as possible between the COMP/FB and GND.
5. Keep the switching node, SW, away from the sensitive VOUT/FB/COMP node.
6. The RT/CLK terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.
7. Output inductor and freewheeling diode should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.
8. UVLO adjust (by EN pin) and RT resistors, loop compensation and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.
9. Route BOOT capacitor trace on the other layer than top layer to provide wide path for topside ground.

An example of PCB layout guide is shown in the figure below for reference.

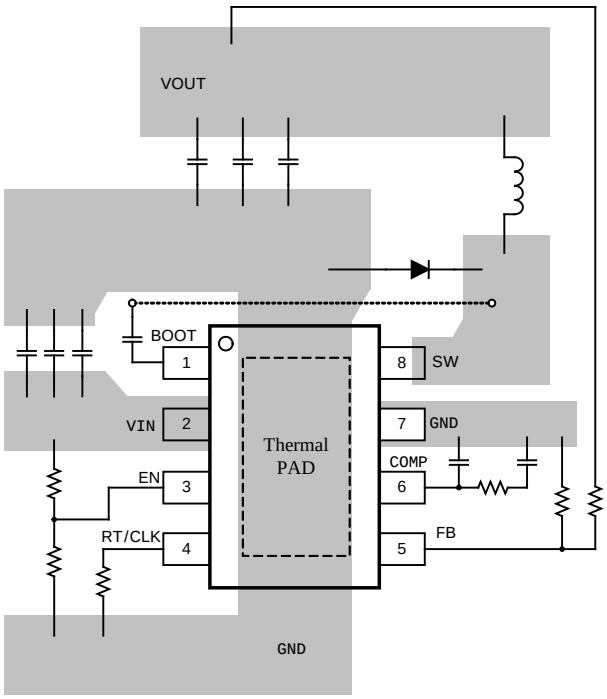
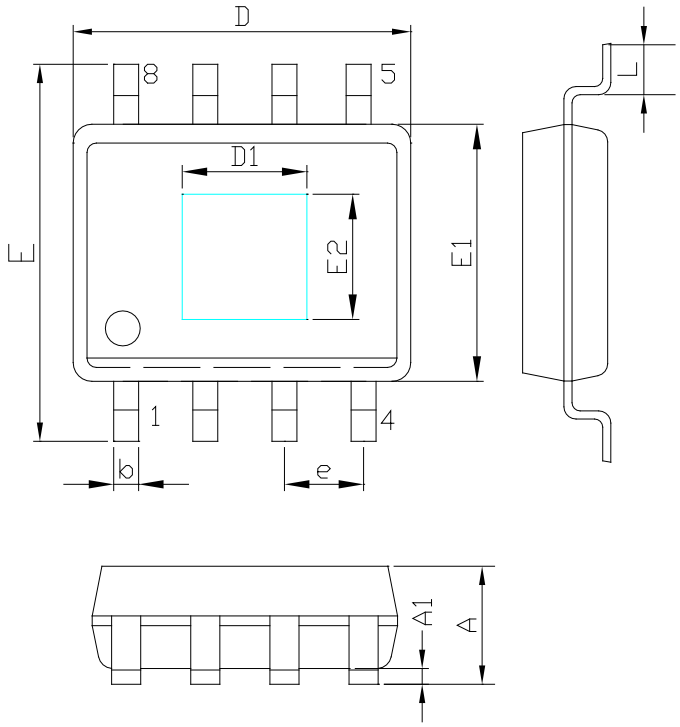


Figure 3. PCB Layout Example

Packaging Information

SOP-8 (EP)



Remark: Exposed pad outline drawing is for reference only.

SYMBOLS	MILLIMETERS			INCHES		
	MIN.	Normal	MAX.	MIN.	Normal	MAX.
A	1.35	-	1.75	0.053	-	0.069
A1	0.00	-	0.25	0.000	-	0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E1	3.70	3.90	4.00	0.146	0.154	0.157
D1	2.67	2.97	3.50	0.105	0.117	0.138
E2	1.78	2.18	2.60	0.070	0.086	0.102
E	5.80	6.00	6.20	0.228	0.236	0.244
L	0.40	-	1.27	0.016	-	0.050
b	0.31	-	0.51	0.012	-	0.020
e	1.27 REF			0.050 REF		