ISG3204LA

100V Half-Bridge SolidGaN for Motor Drive Application

1. Features

- 2.4mΩ Half-Bridge GaN FETs with Gate Driver
- 80V Continuous, 100V Transient Voltage Rating
- Capable of up to 5MHz Switching
- Independent High-Side and Low-Side PWM Inputs
- High-Side and Low-Side Driver Interlocking
- Internal Strong and Smart Bootstrap Switch
- Adaptive Shoot-Through Protection
- Fast Propagation Delay (20ns Typical)
- Excellent Delay Matching (1ns Typical)
- Built-In UVLO, OVLO, OTP Protections
- 35μA Low VCC Quiescent Current
- Integrated VCC/BST capacitors
- High dv/dt Immunity up to 50V/ns
- Adjustable Turn-on Speeds
- Optimized for Easy and Low-EMI PCB Layout
- LGA 5mmx6.5mm Package, 1.12mm Profile

2. Applications

- Motor Drive Applications

3. Description

The ISG3204 is a 100V, 60A, half-bridge SolidGaN in a compact 5mm x 6.5mm LGA package. Included in the package are two high-performance GaN FETs, drivers, and driver supply capacitors, offering the industry's most compact and efficient GaN power solution.

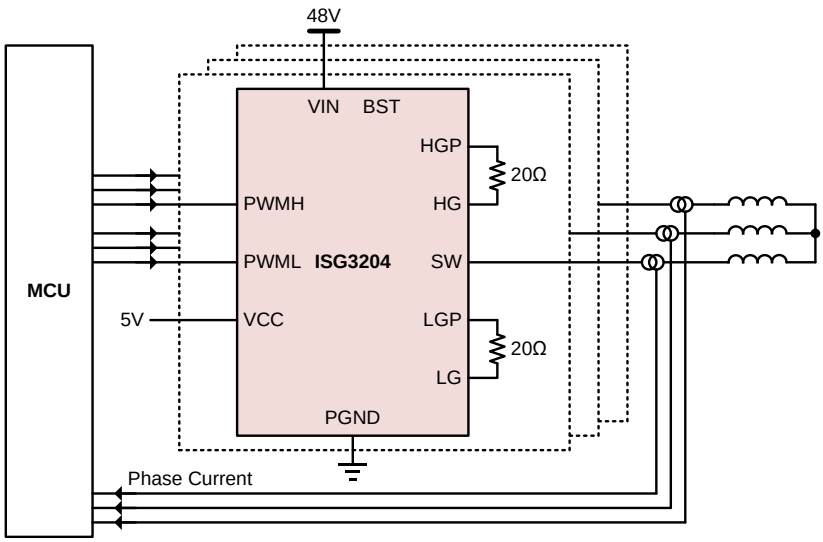
The ISG3204 provides two logic inputs for controlling the high-side and low-side GaN FETs for maximum flexibility. The split driver outputs allow for independent adjustment of turn-on and turn-off strengths, optimizing both EMI and efficiency.

The ISG3204 features input interlocking with internal adaptive shoot-through protection circuit, ensuring no simultaneous output conduction even at near zero dead time. Comprehensive fault protection is built into the ISG3204, including active bootstrap (BST) voltage control to prevent overcharge and ensure stable gate drive voltage, independent UVLO and OVLO for both VCC and BST, and over temperature protection.

With fast propagation delay, excellent delay matching, superior dv/dt immunity, and ultra-low in-package parasitic inductance loop, the ISG3204 enables designers to achieve substantial improvement in power density and efficiency.

4. Typical Application

48V 500W~1KW Motor Driver



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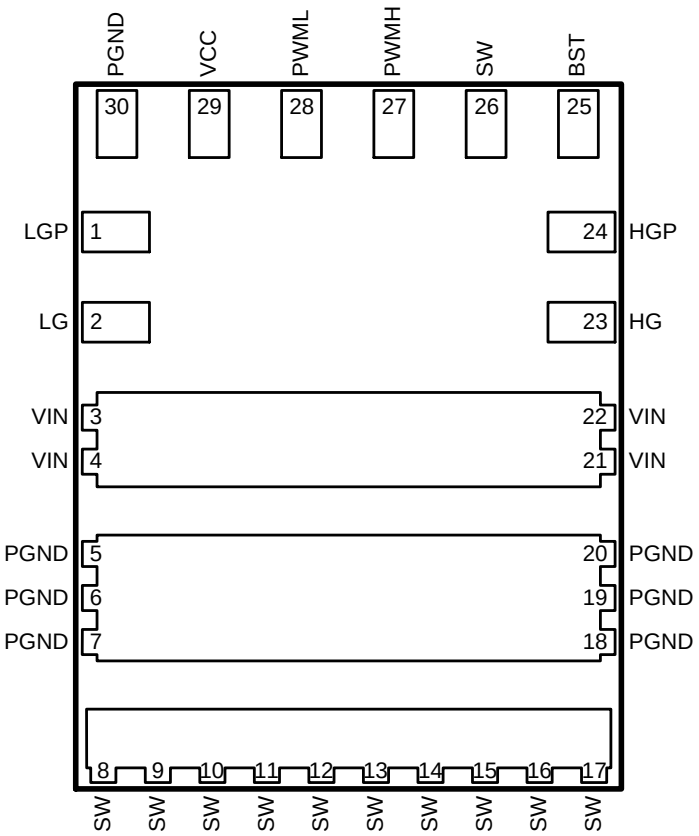
5. Revision History

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-11-24	Final datasheet release

6. Pin Configuration and Functions



30-Lead LGA (5mm x 6.5mm) Package – Top View

Pin Number	Pin Name	Description
1	LGP	Low-Side Gate Driver Source-Current Output. An optional resistor between LGP and LG can be employed to adjust turn-on speed of low side GaN FET.
2	LG	Low-Side Gate Terminal.
3-4,21-22	VIN	Input Voltage Supply. Locally bypass this pin to PGND with ceramic capacitors
5-7,18-20, 30	PGND	Power Ground.
8-17	SW	Switching Node for Main Power.
23	HG	High-Side Gate Terminal.
24	HGP	High-Side Gate Driver Source-Current Output. An optional resistor between HGP and HG can be employed to adjust turn-on speed of high side GaN FET.
25	BST	High-Side Gate Driver Bootstrap Rail. Two 0.1uF ceramic capacitors are integrated between BST and SW pins, and external bootstrap capacitor is optional.
26	SW	Switching Node for Gate Drive Loop. SW waveform can be monitored. Pin 26 is connected to Pin 8-17 internally and no external connection is necessary.
27	PWMH	High-Side Driver PWM Input. This pin has an internal 200kΩ pull-down resistor.
28	PWML	Low-Side Driver PWM Input. This pin has an internal 200kΩ pull-down resistor.
29	VCC	External 5V Driver Supply. Two 0.1uF ceramic capacitors are integrated between VCC and PGND pins, and external decoupling capacitor is optional.

7. Absolute Maximum Ratings

All pins are referred to PGND pins, unless otherwise specified. Stress beyond the absolute maximum ratings can cause permanent damage or deteriorate device reliability and lifetime.

Parameter	Min	Max	Unit
Drain-to-Source Voltage of Internal GaN FET		100	V
VIN		100	V
VCC, BST to SW	-0.3	6.0	V
SW	-5	100	V
BST	-0.3	105	V
HGP, HG	V_{SW}-0.3	V_{BST}+0.3	V
LGP, LG	-0.3	6.0	V
PWMH, PWML	-0.3	6.0	V
Continuous Current for Internal GaN FET		60 (1)	A
Pulsed Current for Internal GaN FET (25°C, T_{Pulse} = 100 μs)		230	A
Operating Junction Temperature T_J	-40	150	°C
Storage Temperature	-40	150	°C

(1) Ideal thermal condition. In real application the current capability depends on system thermal design.

8. ESD Ratings

Parameter	Value	Unit
Human Body Model (HBM), per JESD22-A114 (2)	±1000	V
Charged Device Model (CDM), per JESD22-C101F (3)	±1000	V

(2) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(3) JEDEC document JEP155 states that 250V CDM allows safe manufacturing with a standard ESD control process.

9. Recommended Operating Conditions

Parameter	Min	Max	Unit
VIN	0	80	V
VCC	4.5	5.5	V
PWMH, PWML	0	5.5	V
SW	-4	80	V
BST	SW+4.5	SW+5.5	V
SW Slew Rate		50	V/ns
Operating Junction Temperature T_J	-40	125	°C

10. Thermal Information

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	59	°C/W
$R_{\theta JC(TOP)}$	Thermal Resistance, Junction to Case Top	14.8	°C/W
$R_{\theta JC(BOT)}$	Thermal Resistance, Junction to Case Bottom	4.1	°C/W
T_{sold}	Reflow soldering temperature	≤260	°C

*According to standards defined in JESD51 and JESD51-1, thermal characteristic of the package is simulated. $R_{\theta JA}$ is

determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.

11. Electrical Characteristics

T_J = 25°C, VCC = BST = 5V, SW = PGND = 0V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Supply Input						
VCC Quiescent Current	I_{CC-Q}		35	60	μA	PWMH = PWML = 0
VCC Operating Current	I_{CC-OP}		20	30	mA	f = 1MHz
BST Quiescent Current	I_{BST-Q}		40	70	μA	PWMH = PWML = 0
BST Operating Current	I_{BST-OP}		20	30	mA	f = 1MHz
VCC Overvoltage Rising Threshold	V_{CC-OVR}	5.7	6	6.3	V	
VCC Overvoltage Hysteresis	$V_{CC-OVHYS}$		0.25		V	
VCC Undervoltage Rising Threshold	V_{CC-UVR}	3.9	4.1	4.3	V	
VCC Undervoltage Hysteresis	$V_{CC-UVHYS}$		0.3		V	
BST Undervoltage Rising Threshold	$V_{BST-UVR}$		3.6		V	
BST Undervoltage Hysteresis	$V_{BST-UVHYS}$		0.5		V	
PWM Input						
Input High Threshold	V_{IH}		1.8	2.2	V	
Input Low Threshold	V_{IL}	0.8	1.2		V	
Input Hysteresis	V_{I-HYS}		0.6		V	
Input Pull-Down Resistance	R_I		200		kΩ	
Bootstrap Switch						
Switch On Resistance	$R_{BST(ON)}$		4		Ω	
High and Low-Side Gate Driver						
Output Pull-Down Resistance	R_{DN}		0.2	1	Ω	I_{HG} or I_{LG} = 10mA
Output Pull-Up Resistance	R_{UP}		1	2	Ω	I_{HGP} or I_{LGP} = -10mA
Output Peak Source Current(4)	I_{OH}		1.7		A	HGP = SW or LGP = PGND
Output Peak Sink Current(4)	I_{OL}		4.3		A	HG = BST or LG = VCC
Over Temperature Protection						
OTP Shutdown Rising Threshold(4)	T_{OTP}		165		°C	
OTP Shutdown Hysteresis(4)	$T_{OTP-HYS}$		20		°C	
GaN FETs						
Drain-to-Source Voltage	BV_{DSS}	100			V	PWML = 0V or PWMH = 0V, I_D =400μA
Drain-Source Leakage	I_{DSS}		4	28	μA	PWML = 0V or PWMH = 0V, V_{DS} = 80V
Drain-Source On Resistance	$R_{DS(ON)}$		2.4	3.2	mΩ	PWML = 5V or PWMH = 5V, I_D = 25A
Source-Drain Forward Voltage	V_{SD}		1.5		V	PWML = 0V or PWMH = 0V,

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
						I_S = 0.5A
Output Capacitance(4)	C_{OSS}		460		pF	PWML = 0V or PWMH = 0V, V_{DS} = 50V
Reverse Transfer Capacitance(4)	C_{RSS}		8.2			PWML = 0V or PWMH = 0V, V_{DS} = 50V
Energy Related C_{OSS}(4)	$C_{OSS(ER)}$		700			PWML = 0V or PWMH = 0V, V_{DS} = 0V to 50V
Time Related C_{OSS}(4)	$C_{OSS(TR)}$		1020			PWML = 0V or PWMH = 0V, V_{DS} = 0V to 50V
Output Charge(4)	Q_{OSS}		50		nC	PWML = 0V or PWMH = 0V, V_{DS} = 0V to 50V

12. Switching Characteristics

T_J = 25°C, VCC = BST = 5V, SW = PGND = 0V, unless otherwise noted.

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Minimum Input Pulse Width that Changes the Output(4)	T_{IPW}		10		ns	
Minimum Gate Output Pulse Width(4)	T_{OPW}		12		ns	
HGP Rise Time (0.5V-4.5V)(4)	T_{R_SW}		10		ns	
HG Fall Time (4.5V-0.5V)(4)	T_{F_SW}		3		ns	
LGP Rise Time (0.5V-4.5V)(4)	T_{R_LS}		10		ns	
LG Fall Time (4.5V-0.5V)(4)	T_{F_LS}		3		ns	
Dead time – LG off to HGP on (4)	T_{DTH}		1		ns	
Dead time – HG off to LGP on (4)	T_{DTL}		1		ns	
HG Turn-Off Propagation Delay(4)	T_{HPHL}		20		ns	PWMH falling to HG falling
HGP Turn-On Propagation Delay(4)	T_{HPLH}		20		ns	PWMH rising to HGP rising
LG Turn-Off Propagation Delay(4)	T_{LPHL}		20		ns	PWML falling to LG falling
LGP Turn-On Propagation Delay(4)	T_{LPLH}		20		ns	PWML rising to LGP rising
Delay Matching LGP On and HG Off(4)	T_{MON}		1		ns	
Delay Matching LG Off and HGP On(4)	T_{MOFF}		1		ns	

(4) Not 100% tested and guaranteed by design.

13. Typical Characteristics

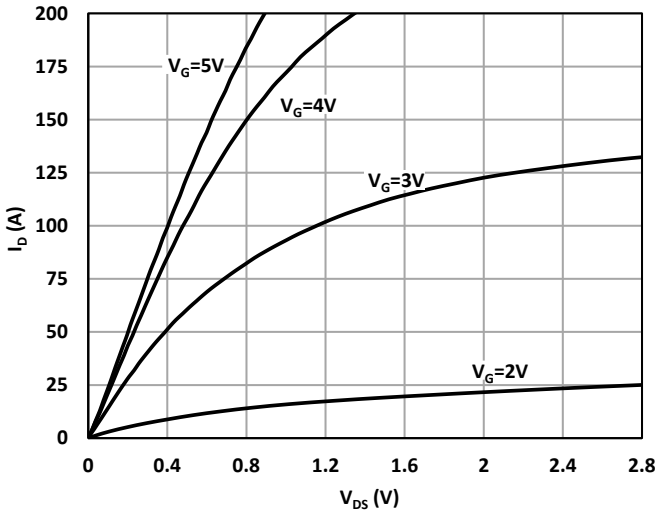


Figure 1. Pulsed Drain Current vs. Drain Voltage (25°C)

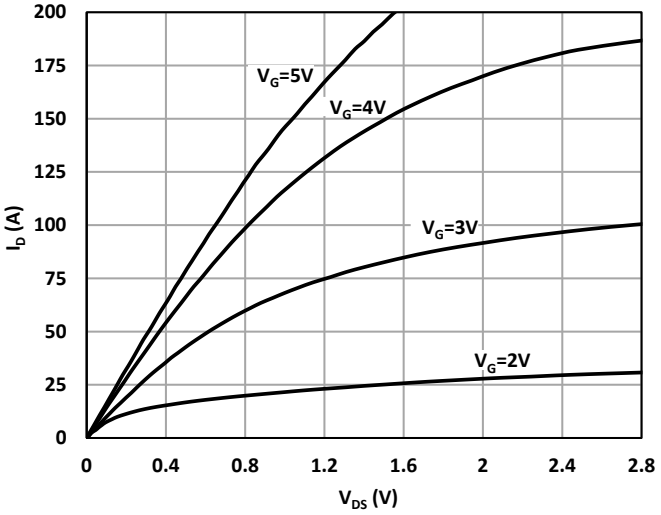


Figure 2. Pulsed Drain Current vs. Drain Voltage (125°C)

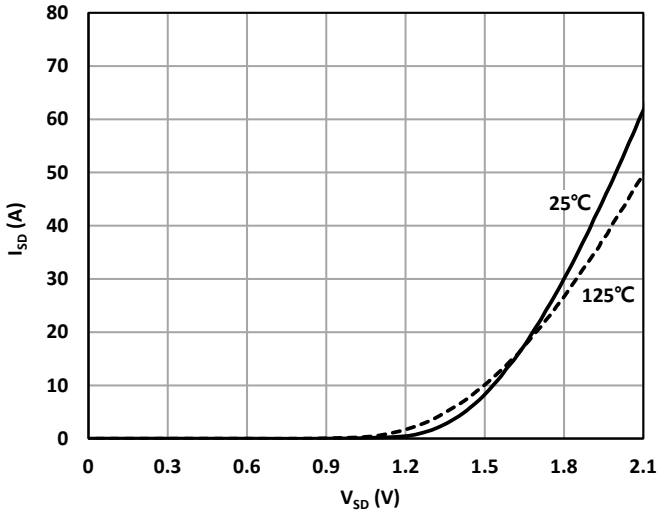


Figure 3. Source-Drain Reverse Conduction Voltage

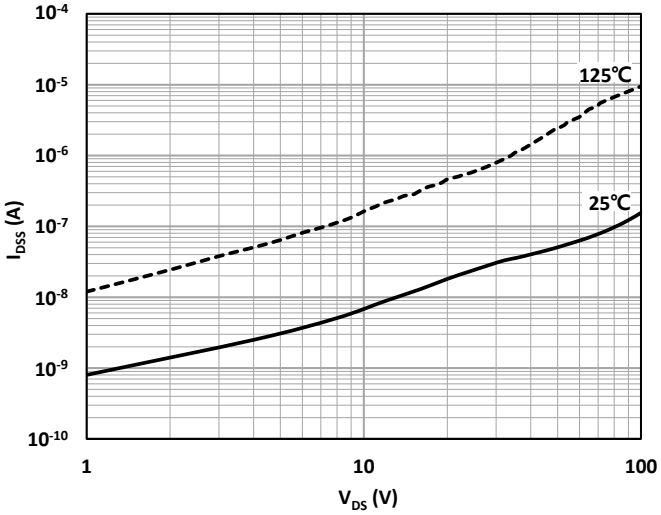


Figure 4. Drain Leakage Current vs Drain Voltage

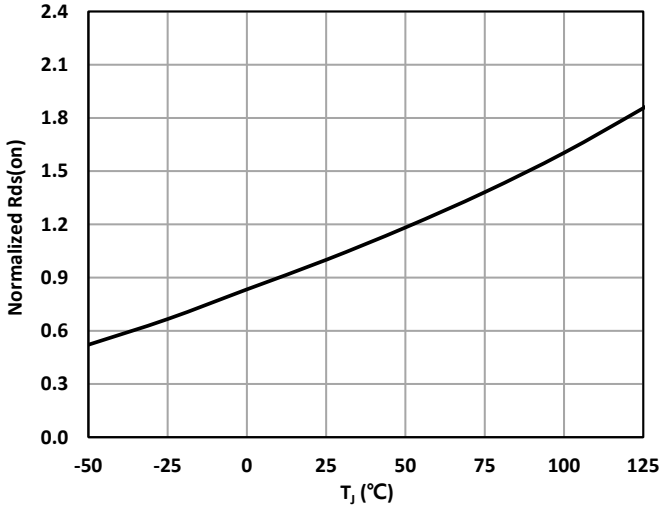


Figure 5. Normalized $R_{DS(ON)}$ vs Temperature

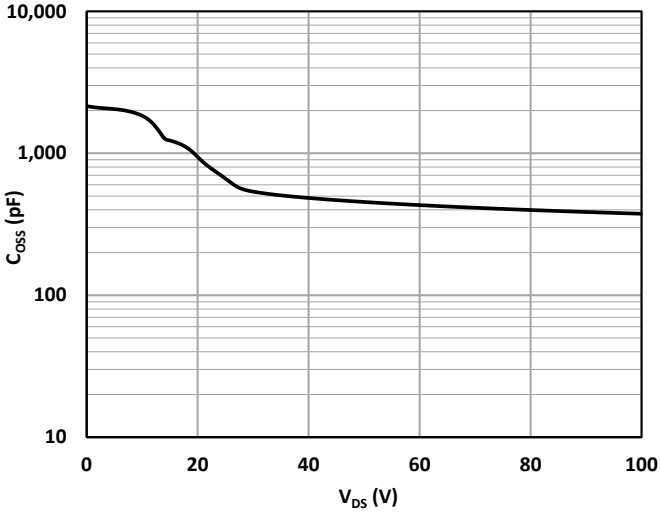


Figure 6. Output Capacitance vs Drain Voltage

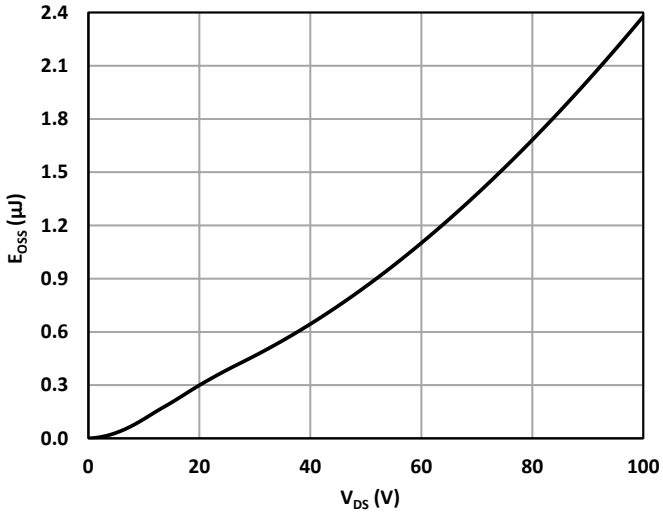


Figure 7. Output Capacitance Stored Energy vs Drain Voltage

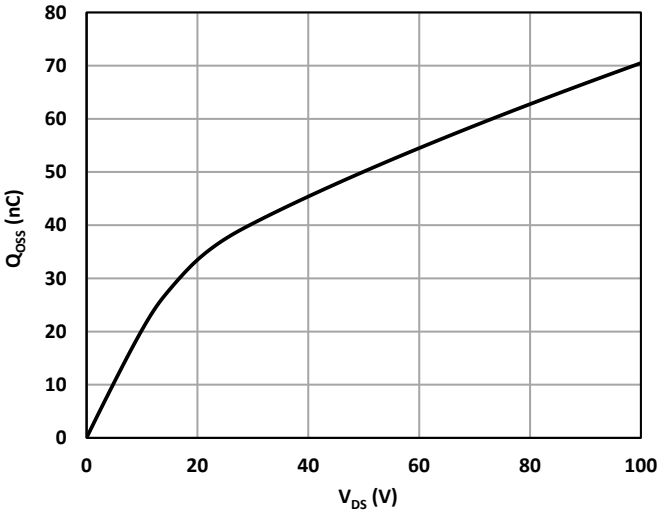


Figure 8. Output Charge vs Drain Voltage

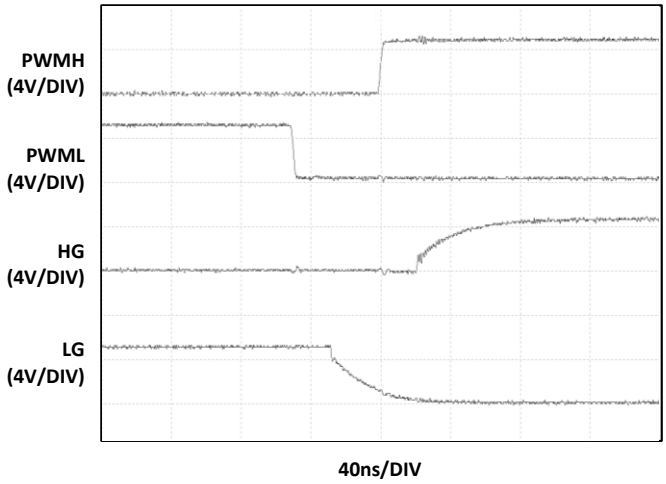


Figure 9. HG Turn-On and LG Turn-Off Waveform
with 20Ω external gate resistors

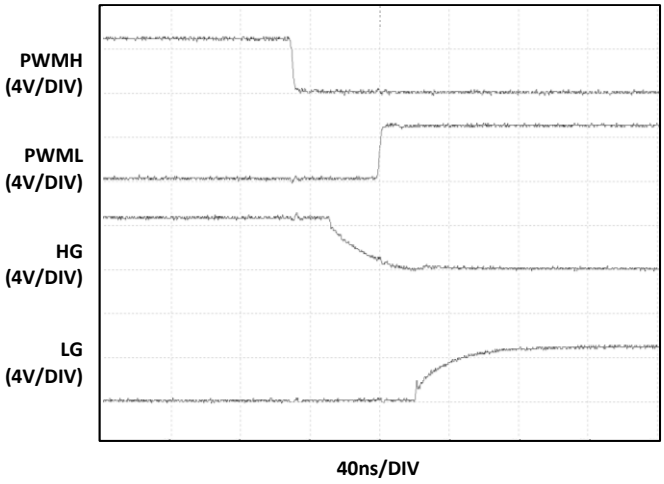


Figure 10. HG Turn-Off and LG Turn-On Waveform
with 20Ω external gate resistors

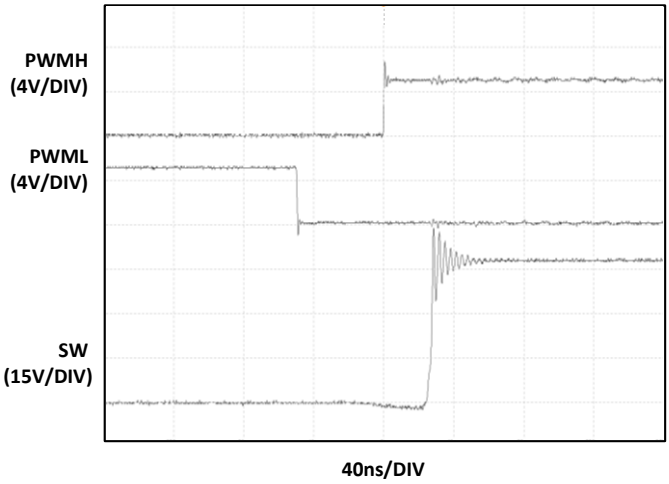


Figure 11. SW Rising Waveform at V_{IN}=48V and I_{OUT}=20A

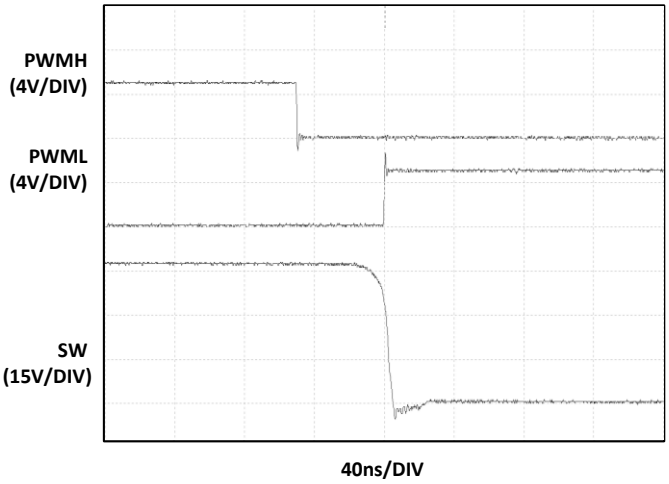


Figure 12. SW Falling Waveform at V_{IN}=48V and I_{OUT}=20A

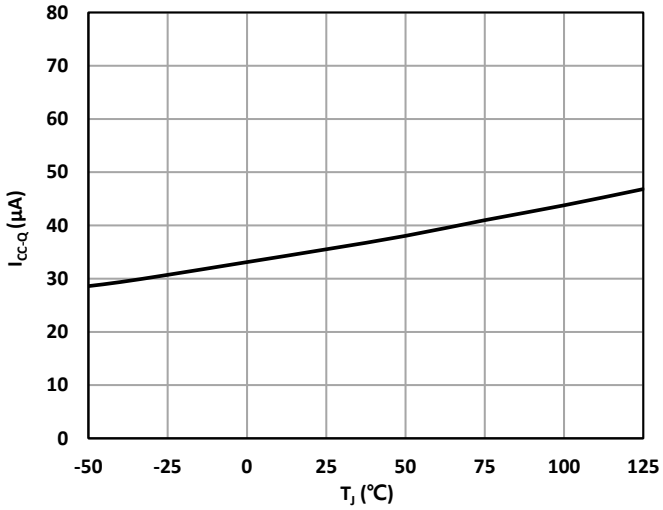


Figure 13. VCC Quiescent Current vs Temperature

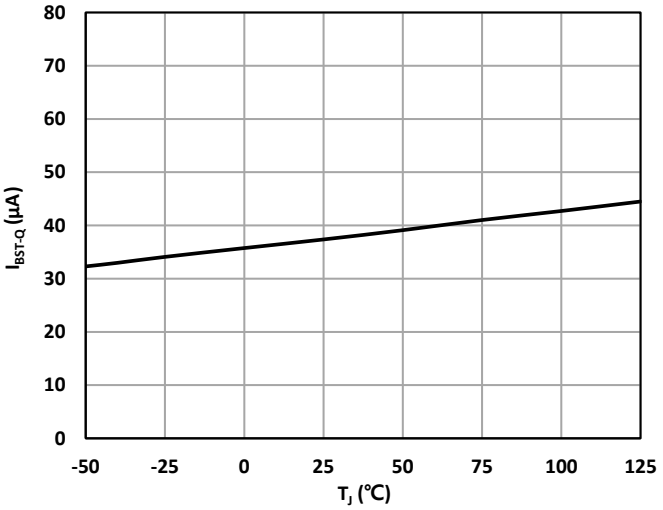


Figure 14. BST Quiescent Current vs Temperature

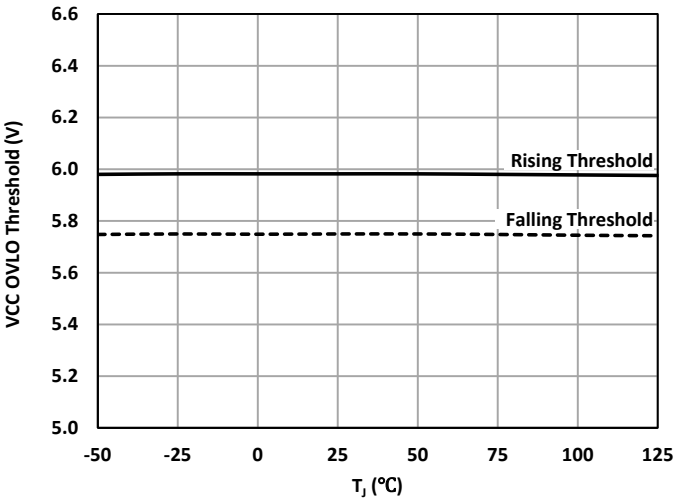


Figure 15. VCC OVLO Threshold vs Temperature

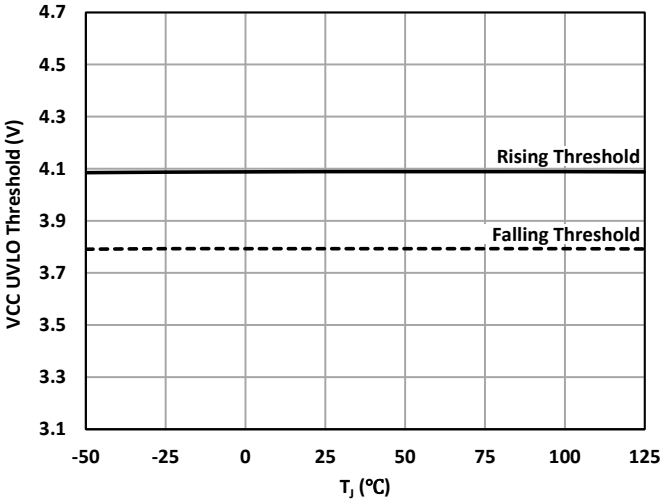


Figure 16. VCC UVLO Threshold vs Temperature

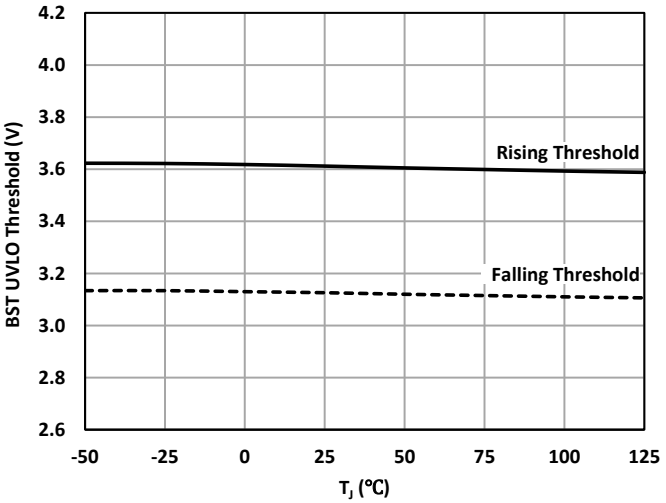


Figure 17. BST UVLO Threshold vs Temperature

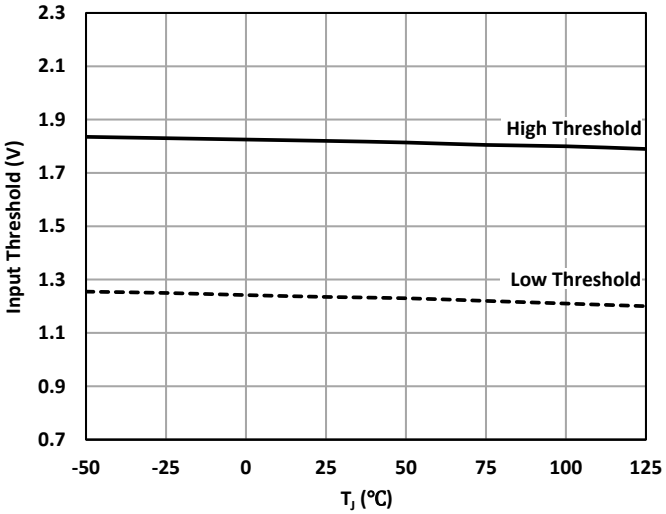


Figure 18. PWM Input Threshold vs Temperature

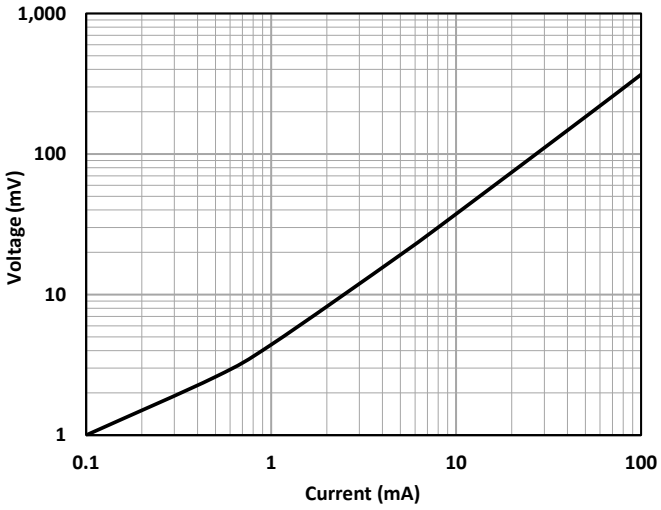


Figure 19. Bootstrap Forward Voltage vs Current

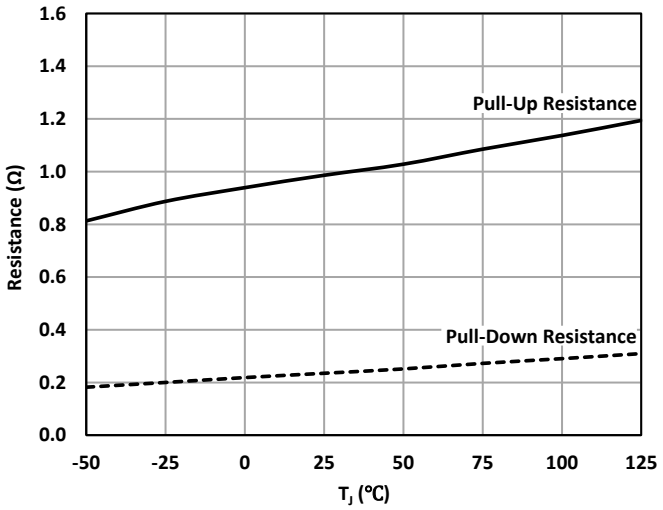


Figure 20. Output Pull-Down/Pull-Up Resistance vs Temperature

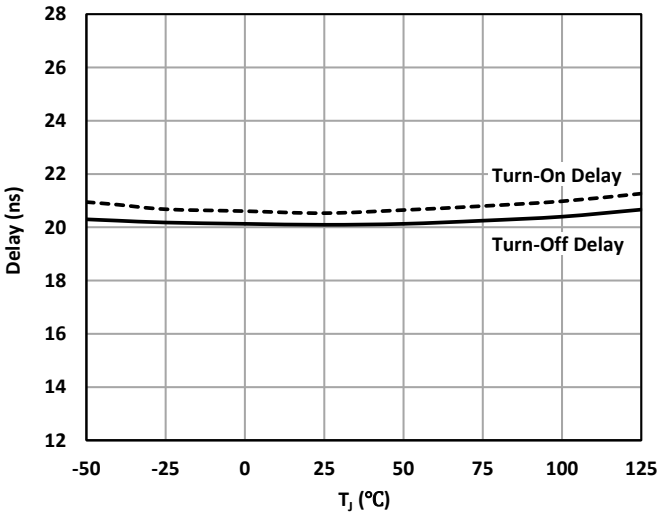


Figure 21. Low-Side Propagation Delay vs Temperature

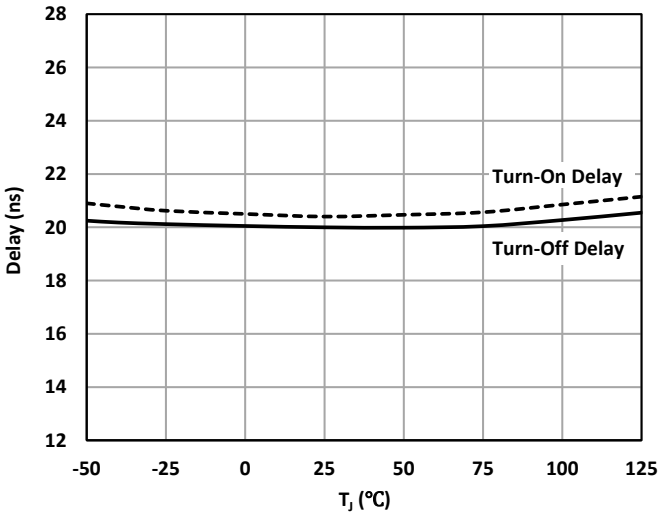


Figure 22. High-Side Propagation Delay vs Temperature

14. Block Diagram

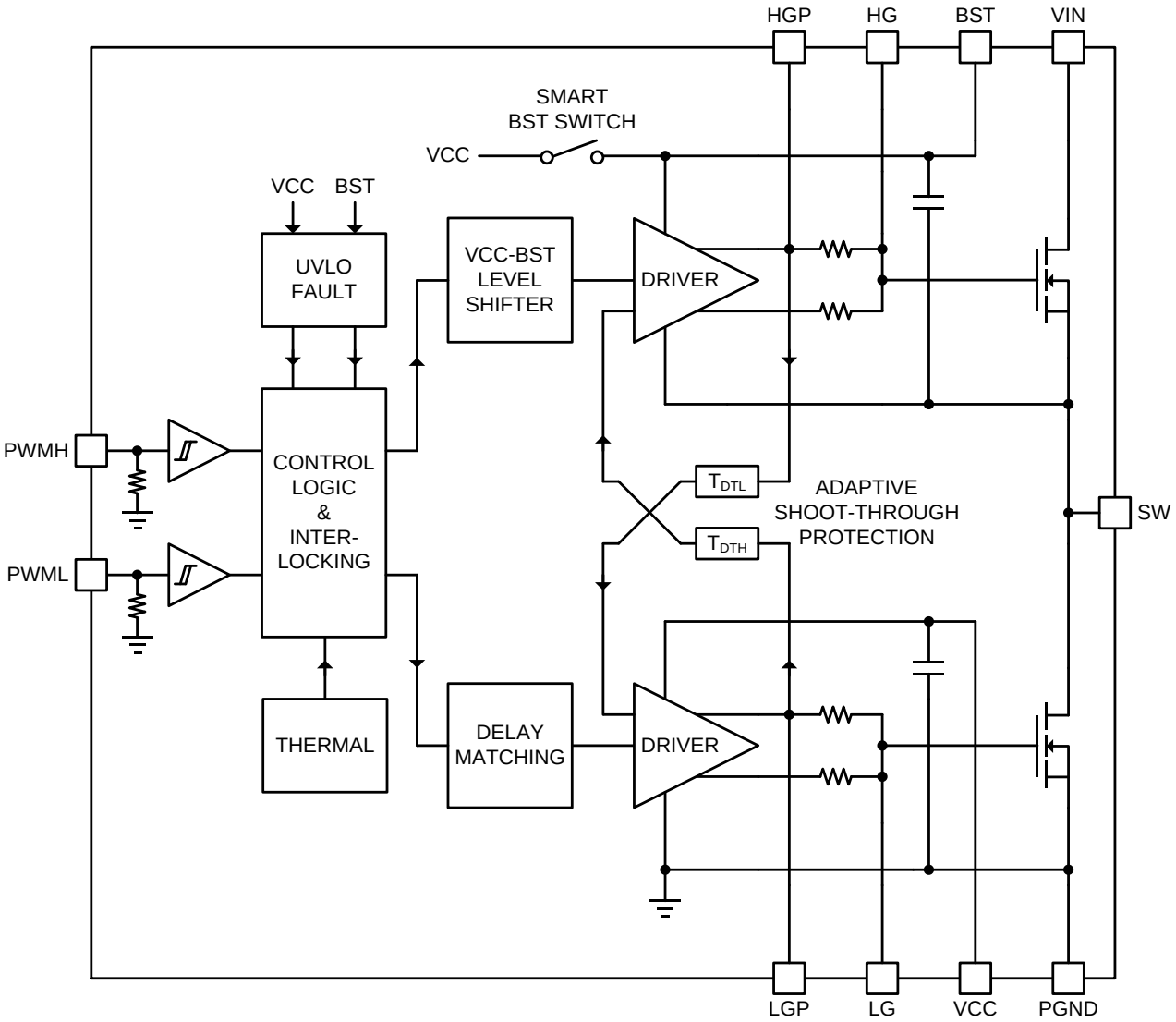


Figure 23. Functional Block Diagram

15. Function Description

The ISG3204 is a 100V SolidGaN half-bridge module in a compact 5mm x 6.5mm LGA package. Within that tiny package, it integrates two high-performance enhancement-mode GaN FETs, gate drivers, gate resistors, and VCC and BST supply capacitors, offering the smallest, most efficient, and easy-to-use GaN power stage solution.

The ISG3204 features two independent and TTL logic compatible inputs to offer control flexibility. It provides split gate driver outputs for the independent control of turn-on and turn-off speeds of both high-side and low-side GaN FETs by adding external gate resistors. The ISG3204's PWM input interlocking function with integrated adaptive shoot-through protection ensures neither output conducts simultaneously, even under near zero dead time delay conditions. Active bootstrap (BST) voltage control in ISG3204 prevents overcharging of the BST supply during dead times, protecting the gate of the GaN FET. Additionally, rich fault protection is provided including independent VCC and BST undervoltage lockout (UVLO), VCC overvoltage lockout (OVLO), and over temperature protection (OTP). Highly integrated with ultra-low inductance, fast propagation delay, and superior dV/dt immunity, the ISG3204 drives next-generation high-frequency, high-power-density applications across diverse topologies including buck, boost, and buck-boost.

Input and Output

The ISG3204 input pins, PWMH and PWML, are independent and TTL logic compatible with the ability to withstand input voltages up to 5.5V regardless of VCC voltage. The ISG3204 offers fast propagation delay (20ns typical) with excellent delay matching (1ns typical) between the high-side and low-side driver channels, making it ideal for high-frequency applications. Both inputs feature a 10ns (typical) input deglitch filter to remove any unwanted pulses from a PWM input. A narrow input pulse exceeding this deglitch delay time will be extended to a minimum output pulse of 12ns (typical) to ensure proper gate turn-on and turn-off transients. Figure 24 shows the switching characteristics of the input and output. The ISG3204 features the interlocking function to prevent shoot-through condition. When both input pins, PWMH and PWML, are high, the internal logic turns off both output pins, HG and LG, as illustrated in Figure 25. Both input pins have an internal pull-down resistor of 200kΩ. Table 1 shows the truth table of input and output.

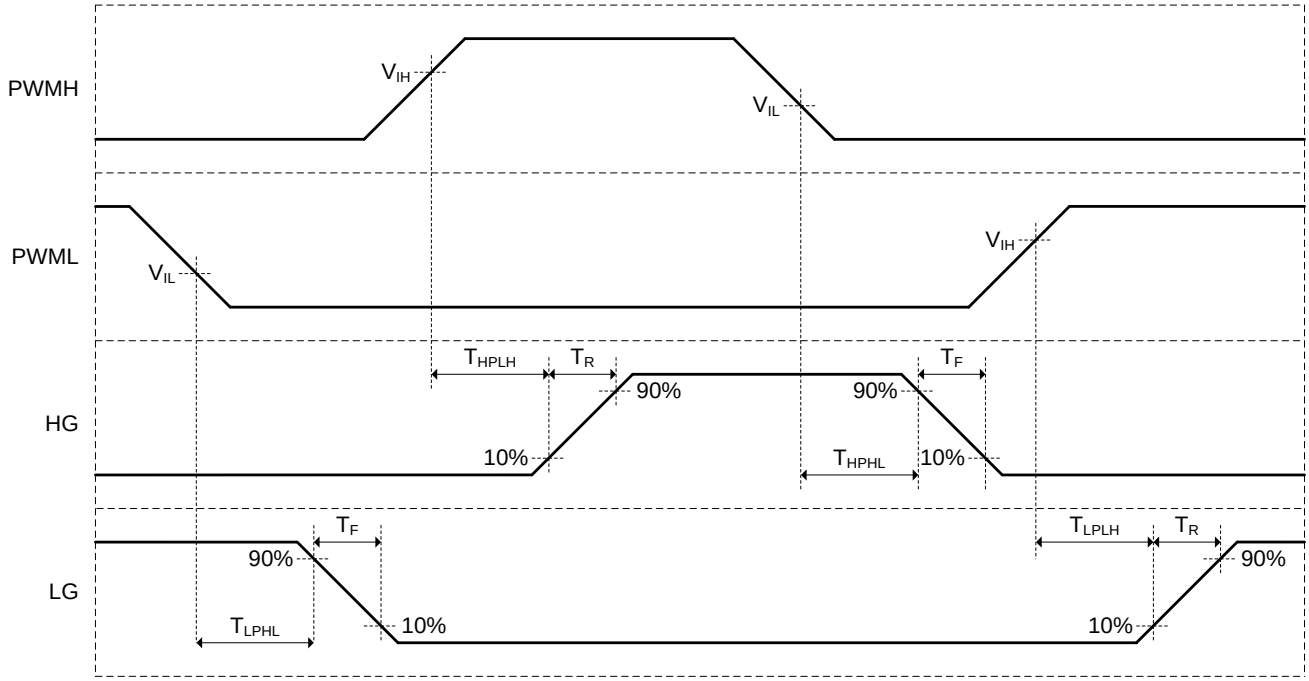


Figure 24. Timing Diagram of Input and Output

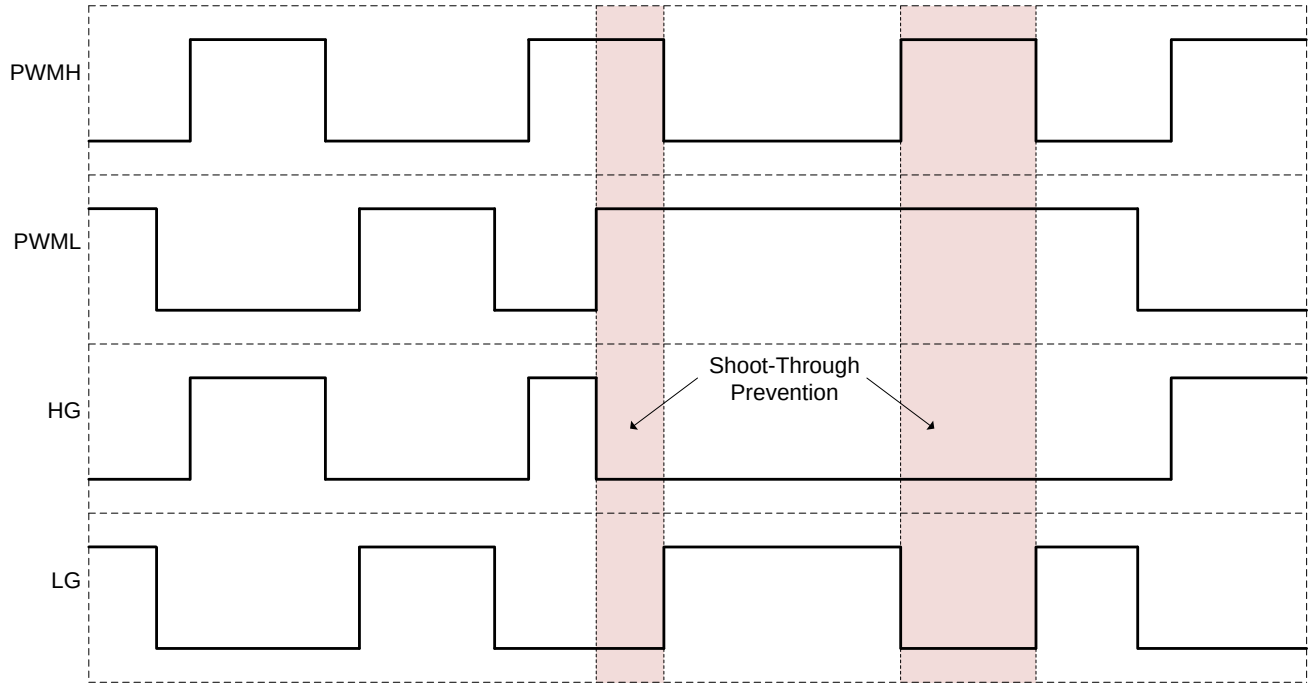


Figure 25. Timing Diagram of Interlocking Function

Table 1. Input and Output Truth Table

PWMH	PWML	HG	LG	Comment
H	L	H	L	High-Side GaN FET On
L	H	L	H	Low-Side GaN FET On
L	L	L	L	Both GaN FETs Off
H	H	L	L	Both GaN FETs Off

Adaptive Shoot-Through Protection

The ISG3204 features an internal shoot-through protection circuit, leveraging shunt sensing of the true gate voltage of GaN FETs through its split outputs structure. It offers precise switching timing control for immediate turn-on after complete turn-off of the opposite side to ensure that they do not conduct simultaneously in any situation. This is processed within a 1ns (typical) to achieve that near-zero dead time delay enhancing efficiency and enabling high-frequency operation.

Half-Bridge Output Stage

The ISG3204 integrates 2.4mΩ, 100V, enhancement-mode GaN FETs with drivers in a half-bridge configuration. It offers increased flexibility by providing split gate driver outputs for both high-side and low-side GaN FETs. As depicted in Figure 26, the internal gate drive output provides a default 20Ω internal pull-up resistor and a 10Ω internal pull-down resistor. Designers can further fine-tune turn-on strength by adding an external resistor in parallel between designated pins of HGP/HG and/or LGP/LG. While turning-off the GaN FET, the integrated strong 0.2Ω pull-down FET offers a robust, low impedance path necessary for eliminating high dv/dt induced gate turn-on. Additionally, the ISG3204 integrates the 0.2μF BST and VCC supplies capacitors within the package, thereby significantly reducing parasitic inductance loop paths and effectively minimizing voltage spikes at the gates of the GaN FETs. HG and LG pins have internal 50kΩ pull-down resistors to SW and PGND, respectively.

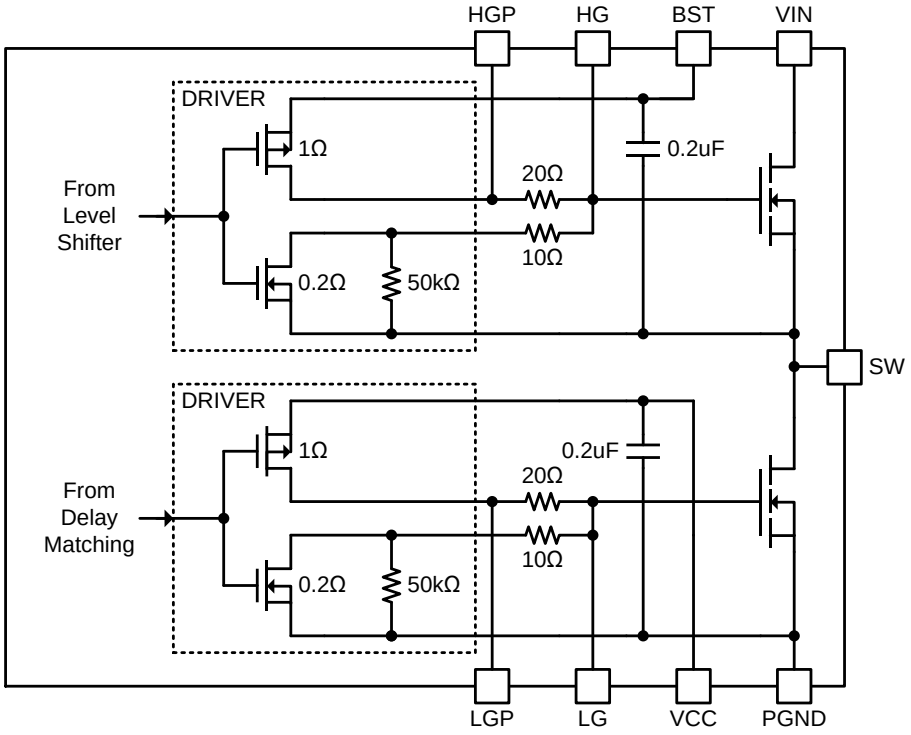


Figure 26. Simplified Output-Stage Block Diagram

VCC UVLO/OVLO Protections

The ISG3204 features UVLO and OVLO for VCC, providing the operation under the safe conditions of devices. When the VCC voltage falls below its UVLO threshold of 3.8V (typical) or exceeds above its OVLO threshold of 6.0V (typical), the ISG3204 turns off both the high-side and low-side GaN FETs and ignores the PWMH and PWML inputs.

High dv/dt Rate GaN FET Switching

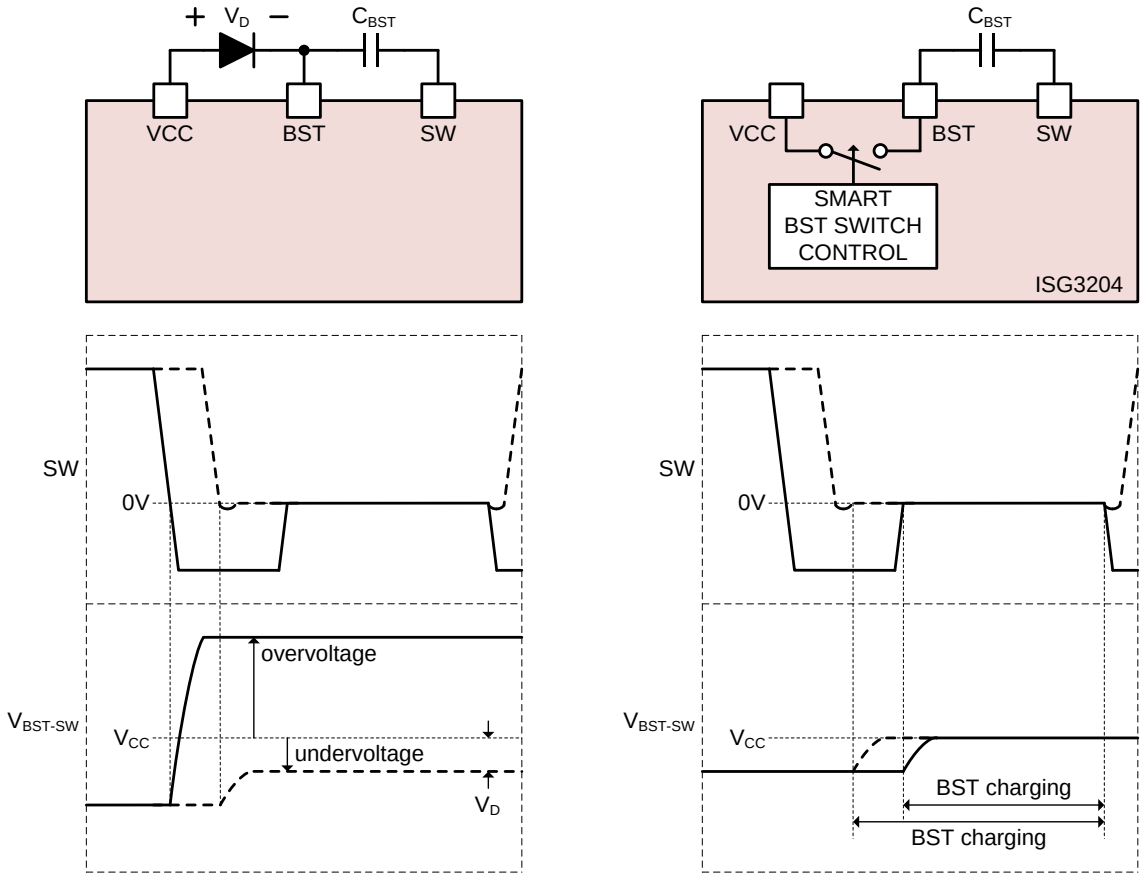
GaN FETs can switch much faster than traditional silicon based MOSFETs, requiring gate drivers capable of delivering precise and fast switching signals to fully leverage their potential. Managing high dv/dt rates during switching is important for stable gate driver circuitry, ensuring reliable and efficient operation. The ISG3204 features an advanced level-shifting technology circuit designed to overcome these challenges associated with driving GaN FETs. Its advanced noise rejection mechanism ensures precise and accurate signal transmission between the control logic to driver outputs even in extreme high dv/dt environments up to 50V/ns.

Another challenge in driving GaN FETs is the issue of high reverse conduction voltage. When the SW node drops below 0V due to this reverse conduction, it can temporarily lower the level shifter's supply rail, causing a disruption in the level shifter's output signals. This disruption can appear as a delay mismatch between signals transmitted to each side of the driver, resulting in timing inaccuracies and potential performance degradation. The proposed level shifter in the ISG3204 is designed to prevent such conditions, ensuring that delay variation is kept to a minimum (1ns typical) even when the SW node fluctuates by up to -4V. Furthermore, the ISG3204 features an additional delay matching circuit that parallels the proposed level shifter circuit, matching its process and temperature variation characteristic. This additional feature further improves delay matching to 1ns (typical).

High-Side Gate-Driver Supply

Despite GaN devices offering advantages with their superior figure of merit ($Q_G \times R_{DSON}$) compared to silicon based MOSFET counterparts, their sensitivity to gate driving voltage levels presents a challenging concern. GaN devices are more vulnerable to both over-voltage and under-voltage conditions at the gate, which can have negative effects on their reliability and performance. The concern over gate over-voltage is more significant for GaN FETs, given that they are considerably more fragile compared to their silicon counterparts. Conversely, Insufficient gate voltage, or gate under-voltage, can result in increased switching losses and reduced efficiency.

To mitigate these challenges, the ISG3204 features a smart BST switch that allows precise control for BST charging and blocking. Figure 27 illustrates the operation principle of the smart BST switch. Unlike silicon MOSFETs, GaN FETs typically lack an intrinsic body diode, resulting in higher reverse conduction voltages, (typically 2V to 3V or even higher at high current) during dead time. This can lead to overcharging of the BST capacitor, potentially causing permanent damage to the gate of the high-side GaN FET. In the ISG3204, the BST switch's turning on and off are precisely controlled so that it allows charging of the BST capacitor only during SW node is fully reached at PGND voltage when the low-side power switch is being turned on. Moreover, the BST switch exhibits a low on-impedance of 4Ω (typical), ensuring minimal dropout voltage. Accordingly, the ISG3204 always maintains a well-balanced BST rail voltage close to VCC, achieving excellent delay matching and balanced gate driving strength between the high-side and low-side drivers.



(a) Conventional Bootstrap Diode (b) Smart Bootstrap Switch

Figure 27. Operation Principle of Bootstrap Supply

Additionally, the ISG3204 provides a BST UVLO protection with a falling threshold of 3.1V (typical) and a rising

threshold of 3.6V (typical). When BST-SW falls below BST UVLO threshold, the ISG3204 enters BST UVLO mode, turns off the high-side GaN FET, but the low-side driver and GaN FET remain activated.

Over Temperature Protection (OTP)

The ISG3204 employs OTP. If the internal junction temperature, T_j, exceeds 165°C (typical), The PWMH and PWML inputs are ignored, and both the high-side and low-side GaN FETs are turned off. When the temperature drops below 145°C (typical), the ISG3204 will resume normal operation.

Layout Recommendation

Due to the small input capacitance of the GaN FET, the ISG3204 can support a high-frequency operation but it causes high dv/dt and high di/dt in power loop. To avoid the voltage and current spike caused by high dv/dt and high di/dt, the parasitic of the gate driving loop and power loop must be reduced by proper layout technique.

The ISG3204 employs an excellent layout on internal substrate to reduce the gate driving loop and power loop: (1) The driver has been placed very close to the GaN FETs to minimize the loops of parasitic inductance and reduce the noise on the gate loop. (2) The bootstrap capacitor is integrated in the module and the distance between BST and VCC to the driver has been minimized to minimize power loop impedance. (3) The distance between high-side GaN FET and low-side GaN FET has been minimized to avoid excessive voltage spike to the driver caused by the parasitic inductance between high-side GaN FET and low-side GaN FET.

Although the optimized pinout of the ISG3204 simplifies the power stage layout significantly, a proper layout of PCB board is required to fully utilize the benefit of the ISG3204. The layout guidelines are as follows:

1. The optional resistor between HGP(LGP) pin and HG(LG) pin to adjust the turn-on speed of the GaN FETs should be placed close to ISG3204.

2. The optional VCC decoupling capacitor should be placed close to ISG3204.

3. Use planes for VIN and PGND to minimize power losses and ensure effective voltage filtering. The power input decoupling capacitors should be placed close to ISG3204.

A 4-layer PCB layout example is shown in Figure 28. A two-layer board design is also possible due to the optimized pinout.

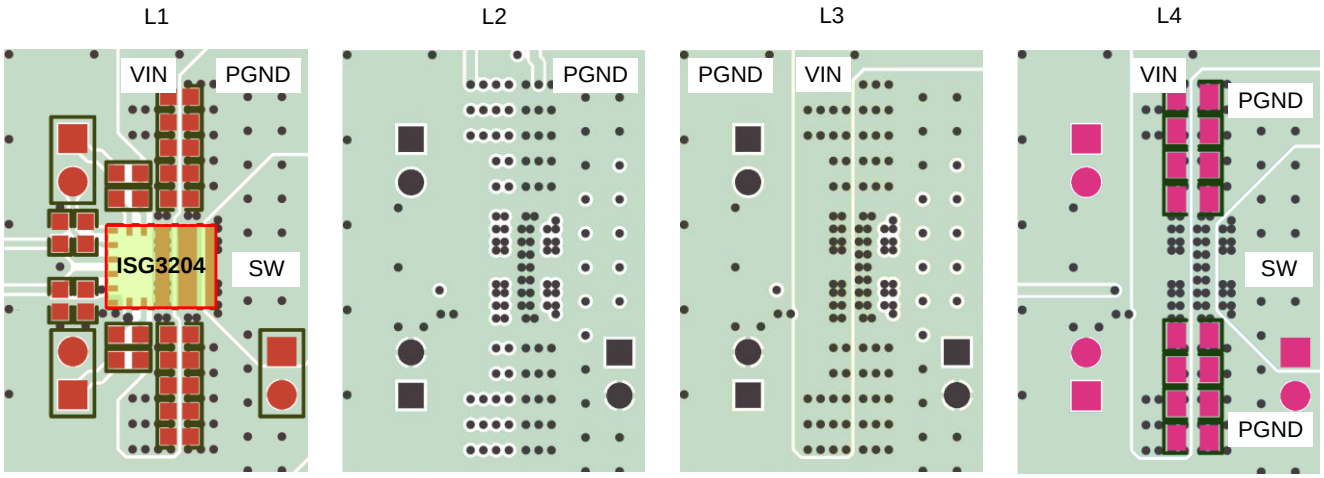


Figure 28. Four-Layer Layout Example

Typical Applications

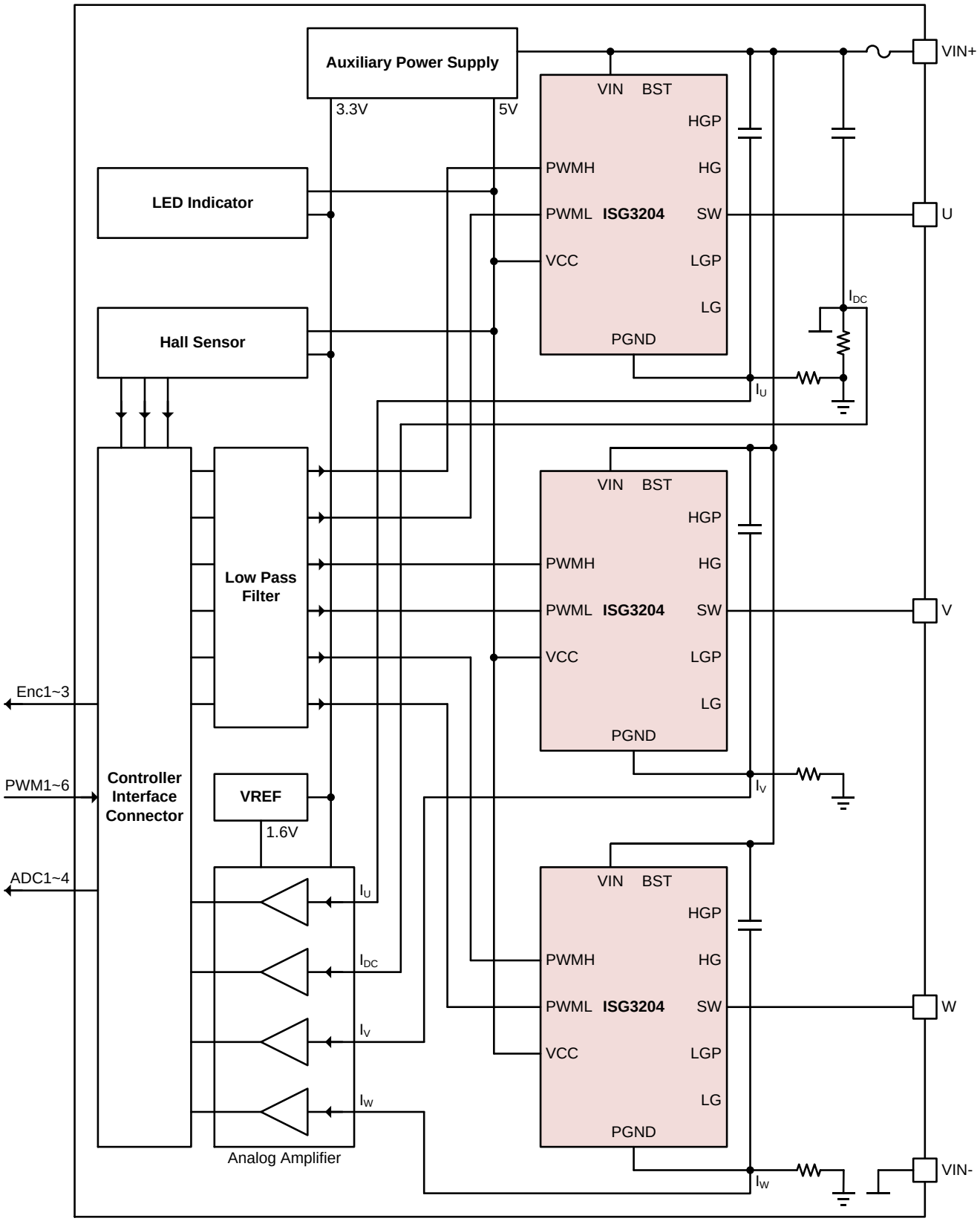
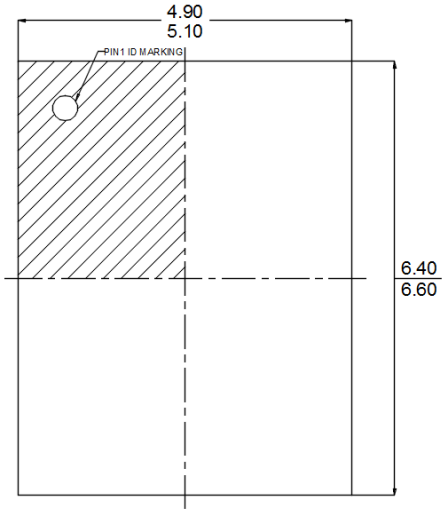


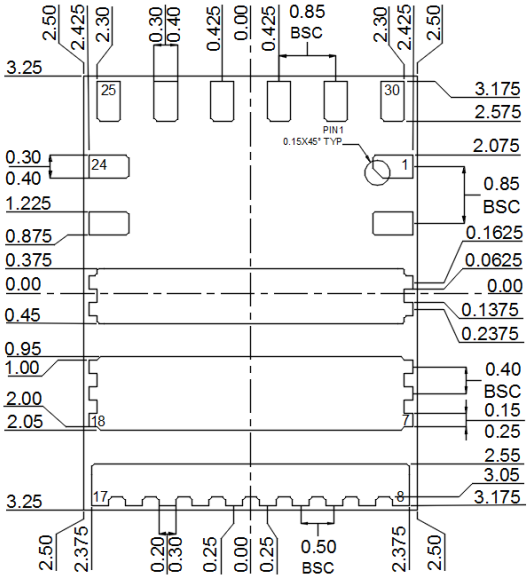
Figure 29. 500W Continuous / 1000W Pulse Power Capability Motor Driver: Refer to INNDDA500A1 Demo Board

16. Package Information

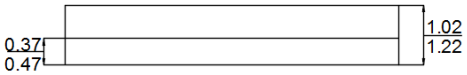
LGA5X6.5 Package:



TOP VIEW

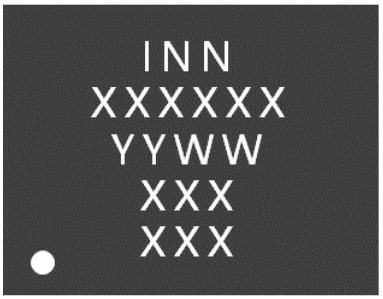


BOT VIEW



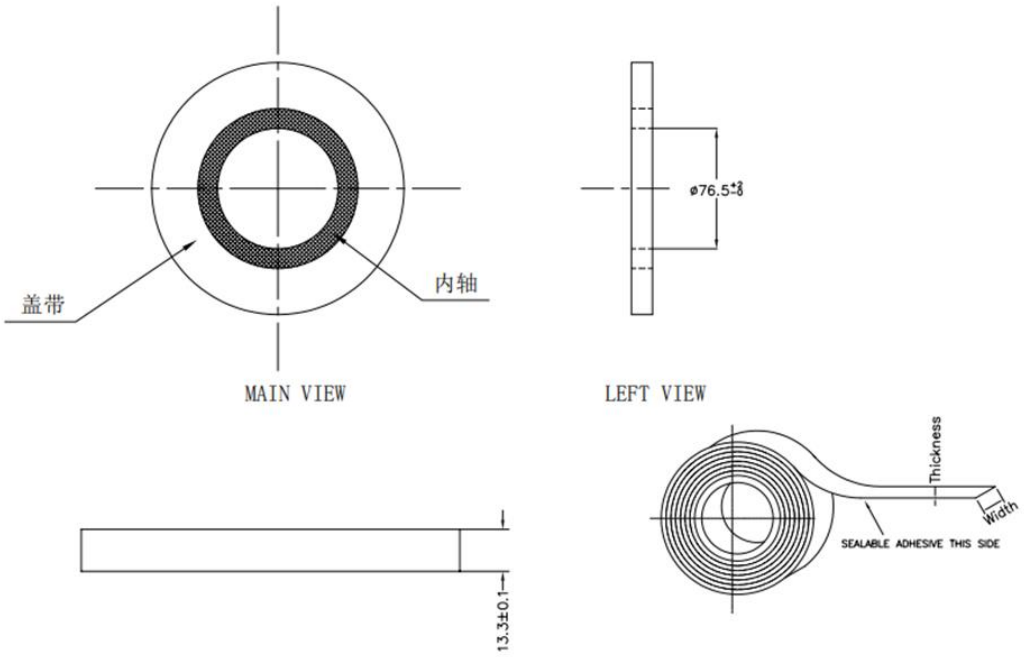
SIDE VIEW

NOTE:
1)ALL DIMENSION ARE IN MILLIMETERS.
2)BOTTOM VIEW IS FT TESTER SIDE VIEW.
3)LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4)COMPLIES WITH JEDEC MO-303.
5)DRAWING IS NOT TO SCALE.



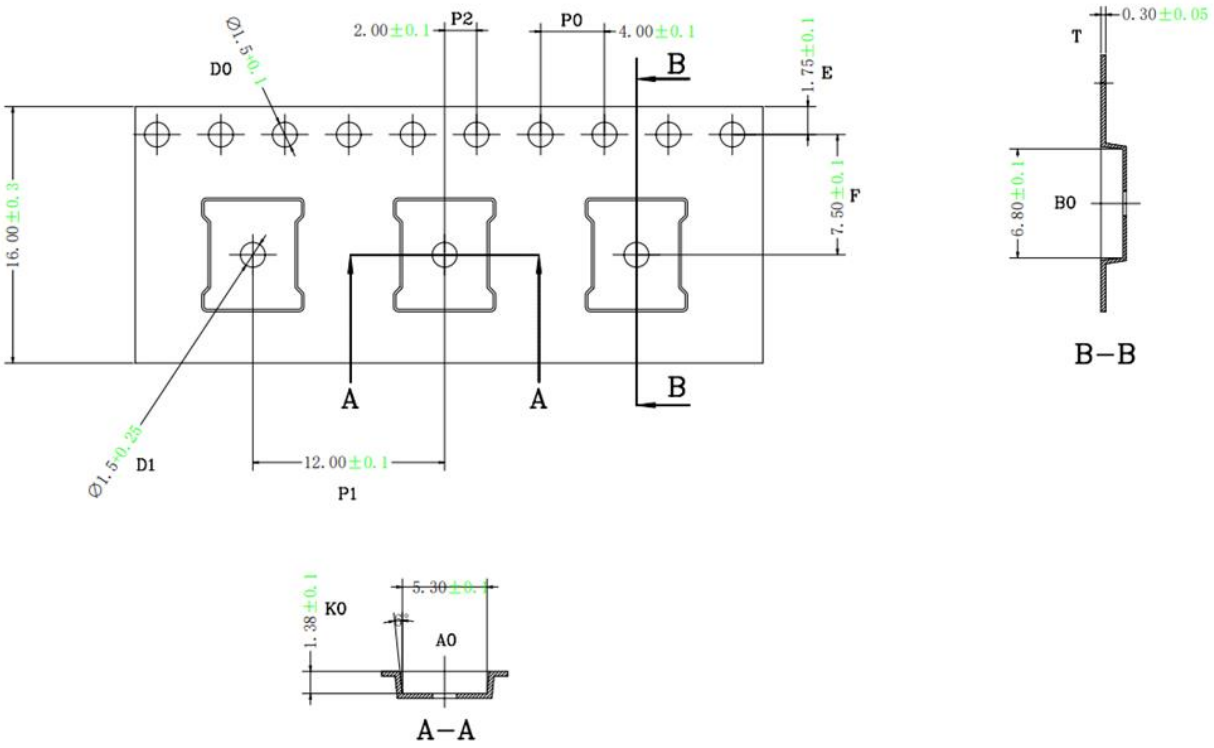
ROW	Description	Example
Row 1	Company Name	INN
Row 2	Product Code	XXXXXX
Row 3	Date Code	YYWW
Row 4	Lot Code	XXX
Row 5		XXX

17. Tape and Reel Information



TECHNOLOGY SPECIFICATION[技术要求]

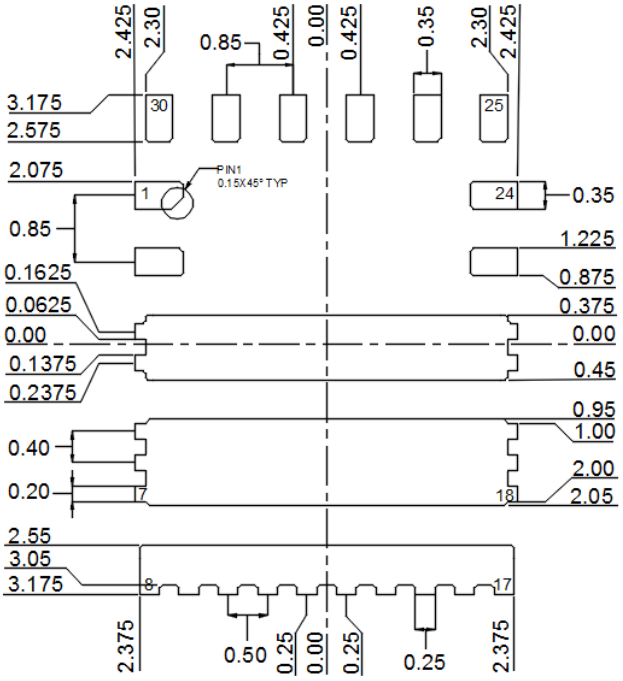
1. COVER TAPE COLOR:TRANSPARENT.[盖带颜色：透明]
2. COVER TAPE THICKNESS: 48±5um.[盖带厚度：48±5微米]
3. THE MATERIAL:PS[材质：聚乙烯]
4. SURFACE RESISTANCE: $1\times10^{5}\sim1\times10^{11}\Omega$.[表面电阻：$1\times10^{5}\sim1\times10^{11}\Omega$]
5. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING.
   [禁止使用长电科技规定的一级环境管理物质]



TECHNOLOGY SPECIFICATION[技术要求]
1. CARRIER TAPE COLOR:BLACK.[载带颜色为黑色]
2. THE MATERIAL:PS [材质：聚苯乙烯]
3. SURFACE RESISTANCE $1X10^4$～$1X10^9$OHMS.[表面电阻为$1X10^4$～$1X10^9\Omega$]
4. MOLD# LGA（5×6.5）.[载带规格LGA（5×6.5）]
5. COVER TAPE WIDTH:13.3±0.1mm. [配套13.3±0.1mm宽盖带]
6. TOLERANCE:X.X ±0.20 X.XX±0.10 [未注明公差参考：X.X±0.2 X.XX±0.10]
7. COVER TAPE COLOR:TRANSPARENT [盖带颜色无色透明]
8. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING.
[禁止使用长电科技规定的一级环境管理物质]

18. Recommended Land Pattern

LGA5X6.5-30L Package:



Unit: mm

19. Order Information

Ordering Code	Package	Product Code	MSL	Packing (Tape & Reel)
ISG3204LA	LGA5x6.5-30L	3204LA	MSL3	13” 2500PCS/reel