SGM41290
Bias and Monitoring Management Circuit

GENERAL DESCRIPTION

The SGM41290 is a highly bias and monitoring management circuit for silicon optical control applications. There are twelve channels of 12-bit programmable current/voltage output DACs with a maximum output current of 40mA and four channels of 12-bit 300mA high-current output DACs. The IC also has twelve MULTI_IO pins (MULTI_IOx) to monitor the current or DAC output signal. The functions of the twelve pins are configurable respectively through the I^2C interface or SPI.

The SGM41290 is available in a Green WLCSP-3.98×3.89-56B package. It operates over an ambient temperature range of -40℃ to +105℃.

APPLICATIONS

Silicon Optical Control

FEATURES

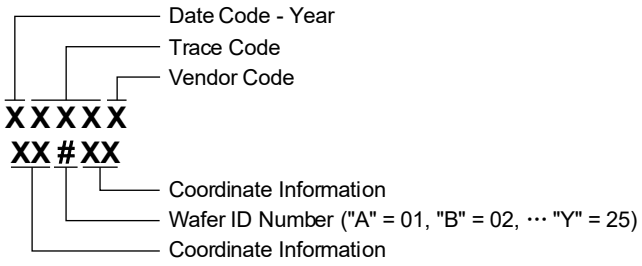
- **Twelve Channels 12-bit VDAC/IDAC (HEATERx)**
  - **Supports Current and Voltage Output Modes**
  - **Voltage Mode: 0V to 2.5V/5V, Maximum 40mA Load Current**
  - **Current Mode: 0mA to 30mA**
  - **Power Supply (VDRIVE) : 2.7V to V_{DD}**
- **Four Channels 12-bit 200mA IDAC (IBIAS)**
  - **Maximum Current: 200mA/300mA**
  - **EN_IBIASx Enable**
  - **EN_IBIASx Fast Turn-Off Control**
  - **Power Supply Range (PVDD): 1.5V to V_{DD}**
- **Twelve Channels Configurable MULTI_IOx**
  - **Support Current Monitoring**
  - **Support Voltage Monitoring**
  - **Support Digital General IO Function**
- **I^2C Interface Supports a Maximum of 1MHz**
- **SPI Interface Supports a Maximum of 20MHz**
- **Integrated Over-Temperature Alarm Function**
- **Available in a Green WLCSP-3.98×3.89-56B Package**

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM41290	WLCSP-3.98×3.89-56B	-40℃ to +105℃	SGM41290GG/TR	SGM 41290 XXXXX XX#XX	Tape and Reel, 7000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code. XX#XX = Coordinate Information and Wafer ID Number.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

VDD ..... -0.3V to 6V
PVDD ..... -0.3V to 6V
VDRIVE ..... -0.3V to 6V
IBIASx ..... -0.3V to 6V
HEATER0 ~ HEATER11 ..... -0.3V to 6V
MULTI_IOx ..... -0.3V to 6V
Sink Current Flowing into Any IO Pin, I_{SINK} .....25mA (MAX)
Source Current Flowing Out of Any IO Pin, I_{SOURCE} .....-25mA (MIN)
Total Sink Current Flowing into All IO Pins, I_{SINK_Tot} .....80mA (MAX)
Total Source Current Flowing Out of All IO Pins, I_{SOURCE_Tot} .....-80mA (MIN)
Junction Temperature .....+150℃
Storage Temperature Range .....-65℃ to +150℃
Lead Temperature (Soldering, 10s) .....+260℃

RECOMMENDED OPERATING CONDITIONS

VDD .....2.7V to 5.5V
PVDD ..... 1.5V to V_{DD}
VDRIVE ..... 2.7V to V_{DD}
TVDD-POR .....2.5V (TYP)
TVDD-Fall .....2.4V (TYP)
$t_{STARYUP}$ ..... 32ms (TYP)
Operating Ambient Temperature Range.....-40℃ to +105℃
Operating Junction Temperature Range.....-40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

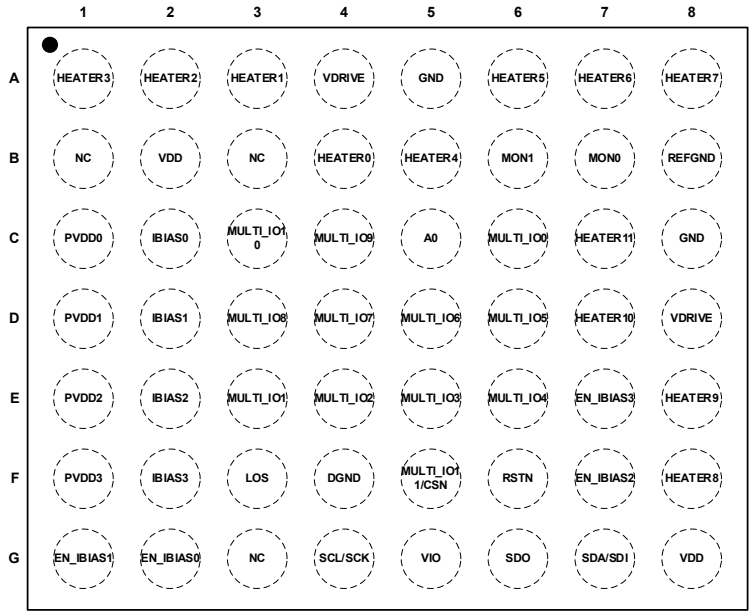
This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

PIN CONFIGURATION

(TOP VIEW)



WLCSP-3.98×3.89-56B

PIN DESCRIPTION

PIN	NAME	TYPE	FUNCTION
A1	HEATER3	AO	12-bit VDAC3/IDAC3 Output.
A2	HEATER2	AO	12-bit VDAC2/IDAC2 Output.
A3	HEATER1	AO	12-bit VDAC1/IDAC1 Output.
A4, D8	VDRIVE	P	Heater Power Supply.
A5, C8	GND	G	Ground.
A6	HEATER5	AO	12-bit VDAC5/IDAC5 Output.
A7	HEATER6	AO	12-bit VDAC6/IDAC6 Output.
A8	HEATER7	AO	12-bit VDAC7/IDAC7 Output.
B1, B3, G3	NC	—	No Connection.
B2	VDD	P	3.3V Power Supply.
B4	HEATER0	AO	12-bit VDAC0/IDAC0 Output.
B5	HEATER4	AO	12-bit VDAC4/IDAC4 Output.
B6	MON1	AO	Multiplexed Monitoring Output. Compliance voltage: 0V to 2.5V.
B7	MON0	AO	Multiplexed Monitoring Output. Compliance voltage: 0V to 2.5V.
B8	REFGND	G	Reference Ground.
C1	PVDD0	P	200mA 12-bit IDAC0 Power Supply.
C2	IBIAS0	AO	200mA 12-bit IDAC0 Output.
C3	MULTI_IO10	I/O	Same as MULTI_IO0.
C4	MULTI_IO9	I/O	Same as MULTI_IO0.
C5	A0	I	I^2C Address Pin/I^2C-SPI Selection.
C6	MULTI_IO0	I/O	Support Current Source Input, Current Sink Input, GPIO.
C7	HEATER11	AO	12-bit VDAC11/IDAC11 Output.

PIN DESCRIPTION (continued)

PIN	NAME	TYPE	FUNCTION
D1	PVDD1	P	200mA 12-bit IDAC1 Power Supply.
D2	IBIAS1	AO	200mA 12-bit IDAC1 Output.
D3	MULTI_IO8	I/O	Same as MULTI_IO0.
D4	MULTI_IO7	I/O	Same as MULTI_IO0.
D5	MULTI_IO6	I/O	Same as MULTI_IO0.
D6	MULTI_IO5	I/O	Same as MULTI_IO0.
D7	HEATER10	AO	12-bit VDAC10/IDAC10 Output.
E1	PVDD2	P	200mA 12-bit IDAC2 Power Supply.
E2	IBIAS2	AO	200mA 12-bit IDAC2 Output.
E3	MULTI_IO1	I/O	Same as MULTI_IO0.
E4	MULTI_IO2	I/O	Same as MULTI_IO0.
E5	MULTI_IO3	I/O	Same as MULTI_IO0.
E6	MULTI_IO4	I/O	Same as MULTI_IO0.
E7	EN_IBIAS3	I	IBIAS3 Enable Control.
E8	HEATER9	AO	12-bit VDAC9/IDAC9 Output.
F1	PVDD3	P	200mA 12-bit IDAC3 Power Supply.
F2	IBIAS3	AO	200mA 12-bit IDAC3 Output.
F3	LOS	O	Fault Interrupt of Heater Current Source Open, Heater Voltage Output Short, IBIAS Open and Short and Over-Temperature Events.
F4	DGND	P	Digital Ground.
F5	MULTI_IO11CSN	I/O	Same as MULTI_IO0/SPI Interface Chip Selection Signal.
F6	RSTN	I	Reset Pin. External reset, low effectiveness.
F7	EN_IBIAS2	I	IBIAS2 Enable Control.
F8	HEATER8	AO	12-bit VDAC8/IDAC8 Output.
G1	EN_IBIAS1	I	IBIAS1 Enable Control.
G2	EN_IBIAS0	I	IBIAS0 Enable Control.
G4	SCL/SCK	I	I^2C Clock/SPI Clock.
G5	VIO	P	IO Power Supply.
G6	SDO	O	SPI Data Output.
G7	SDA/SDI	I/O	I^2C Data Port /SPI Data Input.
G8	VDD	P	3.3V Power Supply.

NOTE: I: input, O: output, I/O: input or output, AO: analog output, G: ground, P: power for the circuit.

TYPICAL APPLICATION

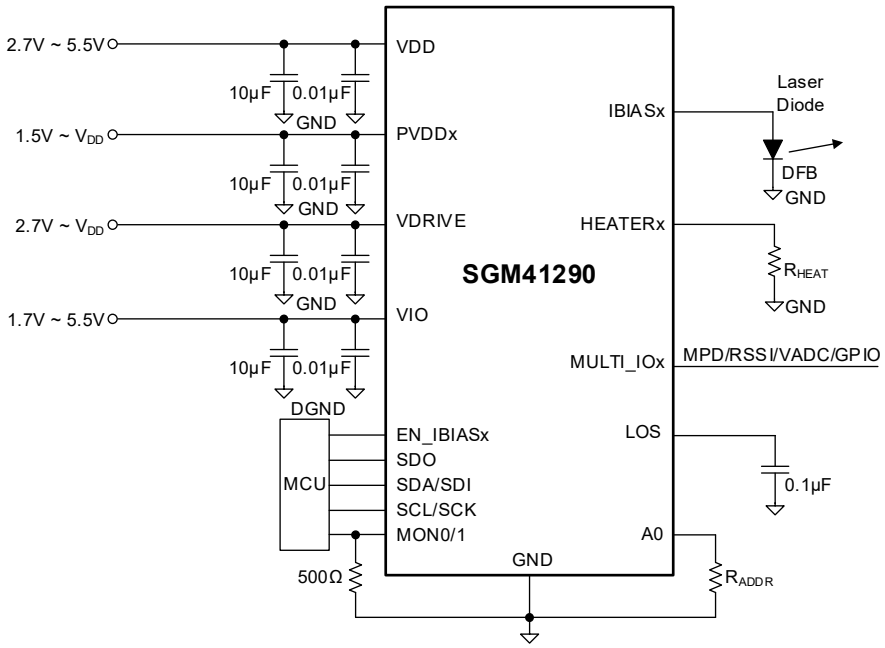


Figure 1. Typical Application Circuit

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, V_{PVDD} = 1.8V, V_{DRIVE} = 3.3V, T_J = -40℃ to +105℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IBIAS Current Source (12-Bit DAC)						
Output Current	I_{IBIAS}	IBIAS GAIN = 1	0		200	mA
		IBIAS GAIN = 1.5			300	mA
Resolution				12		Bit
PVDD Voltage			1.5		V_{DD}	V
Dropout Voltage				0.15		V
IBIAS Accuracy		I_{BIAS} = 100mA, V_{IBIAS} = 1.55V		±2		%
Integral Nonlinearity (1)				±1.5		LSB
Differential Nonlinearity (1)				±0.5		LSB
IBIAS Noise	I_{NOISE}	V_{PVDD} = 1.6V, I_{BIAS} = 100mA, 10Hz to 10kHz		20		μA_{RMS}
IBIAS Full Temperature Drift	V_{IBIAS_DRIFT}	I_{BIAS} = 100mA		40		ppm/℃
Pull-Down Resistor	R_{PD}			10		Ω
IBias Open Detection Threshold		V_{PVDD}-V_{IBIAS} falling		55		mV
IBias short Detection Threshold		V_{IBIAS} falling		600		mV
Heater (12-Bit DAC)						
Current Output Mode						
VDRIVE Voltage Range			2.7		V_{DD}	V
Resolution				12		Bit
Heater Current Source Full Scale Range			0		30	mA
Heater Voltage Tolerance			0		V_{DRIVE} - 0.1	V
Heater Current Source Accuracy		I_{HEATER} = 20mA		±2		%
Integral Nonlinearity				±1.5		LSB
Differential Nonlinearity				±0.5		LSB
Heater Noise		I_{HEATER} = 20mA		5		μARMS
Heater Full Temperature Drift		I_{HEATER} = 20mA		40		ppm/℃
Heater Current Source Open Detection Threshold		VDRV-VHEATER falling		45		mV
Voltage Output Mode						
VDRIVE Voltage Range		DAC normal operating voltage range	2.7		V_{DD}	V
VDAC Voltage Output Full Scale Range (12-Bit DAC)		VDAC gain = 1	0		2.5	V
		VDAC gain = 2 (2)	0		5	V
VDAC Voltage Sink or Source Current Over Full Scale Range					40	mA
Resolution				12		Bit
Integral Nonlinearity				±0.8		LSB
Differential Nonlinearity				±0.2		LSB
VDAC Voltage Accuracy		Code (3) = 4095 @ +25℃		0.5		%
VDAC Voltage Full Temperature Drift		T_J = -40℃ to +105℃		40		ppm/℃
VDAC Noise		V_{HEATER} = 2V		100		μV_{RMS}
VDAC Capacitive Load					500	pF
VDAC Output Short Current Detection Threshold				60		mA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, V_{PVDD} = 1.8V, V_{DRIVE} = 3.3V, T_J = -40℃ to +105℃, typical values are at T_J = +25℃, unless otherwise noted.)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Setup Time		1LSB change		10		μS
MUTI_IO						
Current Range			0		5	mA
Voltage Range		Type A Source	0		V_{DD} - 1.25	V
Monitor Output (MON)						
Current Accuracy		I_{MULTI_IOx} = 3mA		±3		%
		I_{MULTI_IOx} = 150μA (1:32)		±4		%
Current Temperature Drift		I_{MULTI_IOx} = 3mA		±0.5		%
		I_{MULTI_IOx} = 150μA (1:32)		±1.5		%
Current Noise		I_{MULTI_IOx} = 3mA		20		nA_{RMS}
Leakage Current		V_{MON} = 1V		10		nA
On-Resistance	R_{DS}	V_{MON} = 1V		12		Ω
Digital PIN Signals (RST_N, EN_IBIASX, SDA,SCL, MULTI_IOX)						
Input High Threshold			0.7 × V_{IO}			V
Input Low Threshold					0.3 × V_{IO}	V
Control Timing						
EN_IBias De-assert Time				2		us
EN_IBias Assert Time				260		us
Thermal Detection						
Thermal Alert Threshold				135		℃
Thermal Shutdown Threshold				155		℃
Thermal Shutdown Hysteresis				20		℃

NOTES:

1. PVDD: 1.55V to V_{DD}.
2. V_{DRIVE} ≥ 5.2V.
3. Code is the value of HEATERx_MSB<<8+HEATERx_LSB.

I²C COMPATIBLE INTERFACE TIMING CHARACTERISTICS (1)

PARAMETER	SYMBOL	TEMP	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	+25℃			1	MHz
LOW Period of the SCL Clock	t_{LOW}	+25℃	0.5			μs
HIGH Period of the SCL Clock	t_{HIGH}	+25℃	0.26			μs
Bus Free Time between a STOP and a START Conditions	t_{BUF}	+25℃	0.5			μs
Hold Time for a Repeated START Condition	$t_{hd;STA}$	+25℃	0.26			μs
Setup Time for a Repeated START Condition	$t_{su;STA}$	+25℃	0.26			μs
Data Setup Time	$t_{su;DAT}$	+25℃	50			ns
Data Hold Time	$t_{hd;DAT}$	+25℃	0		0.9	μs
Rise Time of SCL Signal after a Repeated START Condition and after an Acknowledge Bit	t_{RCL1}	+25℃	$20 + 0.1C_B$ (2)		120	ns
Rise Time of SCL Signal	t_{RCL}	+25℃	$20 + 0.1C_B$		120	ns
Fall Time of SCL Signal	t_{FCL}	+25℃	$20 + 0.1C_B$		120	ns
Rise Time of SDA Signal	t_{RDA}	+25℃	$20 + 0.1C_B$		120	ns
Fall Time of SDA Signal	t_{FDA}	+25℃	$20 + 0.1C_B$		120	ns
Setup Time for STOP Condition	$t_{su;STO}$	+25℃	0.26			μs
Capacitive Load for SDA and SCL	C_B (2)	+25℃			400	pF

NOTES:

1. The parameters are not production tested and guaranteed by design and characterization.
2. C_B is the total capacitance of one bus line. t_R and t_F are measured between $0.3V_{DD}$ and $0.7V_{DD}$.

I²C INTERFACE TIMING DIAGRAM

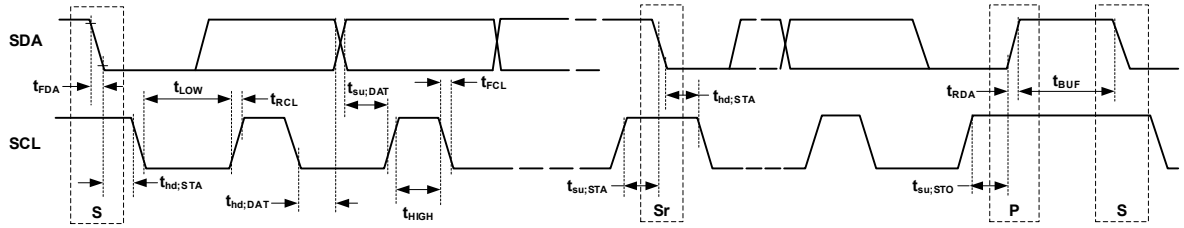


Figure 2. Serial Interface Timing for F/S-Mode

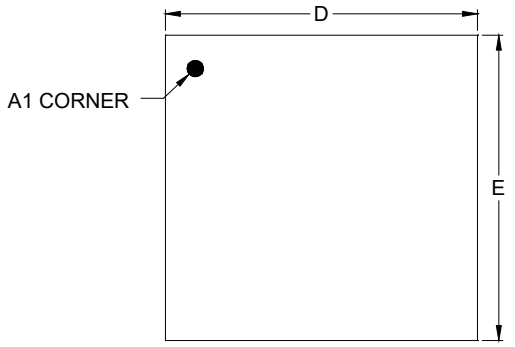
SPI TIMING CHARACTERISTICS

(V_{DD} = 3.3V, V_{PVDD} = 1.8V, V_{DRIVE} = 2.7V, T_J = -40℃ to +105℃, typical values are at T_J = +25℃, DOUT = 20pF || 100kΩ, unless otherwise noted.)

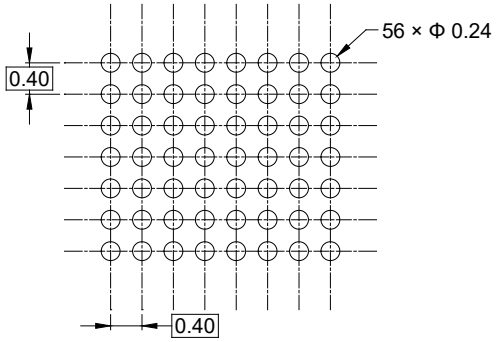
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
CSn Low Level to the First SCLK Setup Time	t_{CSSC}	6			ns
SCLK Cycle Time	t_{SCLK}	50			ns
SCLK High Time	t_{SPWH}	15			ns
SCLK Low Time	t_{SPWL}	15			ns
Data Setup Time	t_{DIST}	10			ns
Data Hold Time	t_{DIHD}	10			ns
CSn High Level Pulse	t_{CSH}	2			t_{CLK}
Last SCLK falling Edge to the CSn High Level	t_{SCCS}	4			t_{CLK}
Command Decoding Time	$t_{SDECODE}$	300			ns
SCLK Falling Edge to Invalid DOUT Holding Time	t_{DOHD}	10			ns
Effective Setup Time from SCLK Rising Edge to DOUT	t_{DOPD}			17	ns
CSn Low Level to DOUT Drive	t_{CSDOD}	10			ns
CS High Level to DOUT Hi-Z	t_{CSDOZ}			10	ns

PACKAGE OUTLINE DIMENSIONS

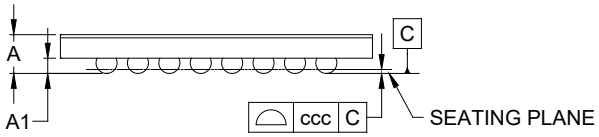
WLCSP-3.98×3.89-56B



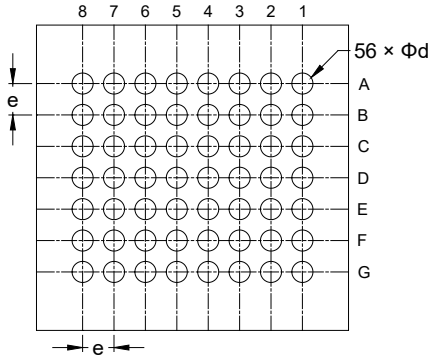
TOP VIEW



RECOMMENDED LAND PATTERN (Unit: mm)



SIDE VIEW



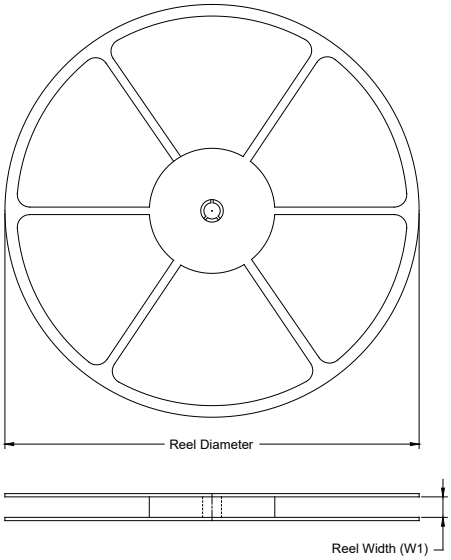
BOTTOM VIEW

Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A	-	-	0.532
A1	0.174	-	0.214
D	3.945	-	4.005
E	3.860	-	3.920
d	0.238	-	0.298
e	0.400 BSC		
ccc	0.050		

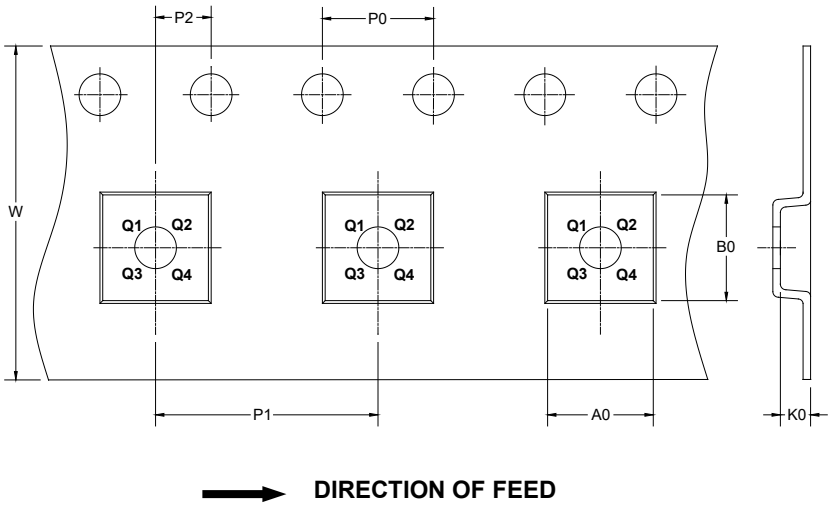
NOTE: This drawing is subject to change without notice.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



DIRECTION OF FEED

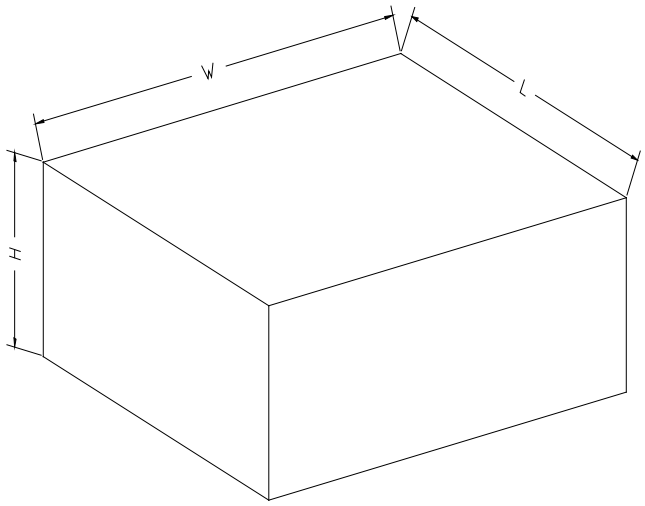
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
WLCSP-3.98×3.89-56B	13"	12.4	4.23	4.23	0.78	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002